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REVIEW ON ADDRESS GENERATION FOR WIMAX DE-INTERLEAVER

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Abstract: WiMAX (World Wide Interoperability for Microwave Access) technology brings a new ingredient in today's mobile community. Since it provides the ability for service providers to deploy new era Broadband service, a low complexity and new technique is proposed to efficiently implement the address generation circuitry for de-interleaver in WiMAX transceiver eliminating the floor function. Internal multiplier of FPGA(Field Programmable Gate Array) is made use of and resources are shared for supporting al modulation schemes with all possible code rates. Hardware structure of address generator is developed and is converted into a Verilog model using Xilinx ISE(Integrated Software Environment) exhibiting significant improvement in FPGA resources.
Index Terms: WiMAX, FPGA, Xilinx ISE, Verilog

I. INTRODUCTION

WiMAX technology is a wireless alternative to the cable modem, digital subscriber lines of any type, transmit/exchange circuits and optical carrier level circuits. It is a wireless communication standard designed to provide 30 to 40MB/s data rates and for fixed stations datarates are upto 1Gb/s. Interleaving plays an important role in wireless networks in combating burst errors. It spreads burst error among multiple code words, thus reduces erroneous bits per code word symbol which can be corrected by forward error correction (FEC) decoder[1]. here are limited works available in the literature related to hardware implementation of the De-Interleaver used in WiMAX transceiver. There are different techniques carried out by researchers to optimize the block interleaver design. Primarily the focus was on reduction in area usage of LUTs[3]. Secondly the permutations were reformed to be done row by row rather than bit by bit[5]. Despite these optimizations, the multimode block interleaver providing more than one interleaving sequence still need huge LUTs which is in contrast that the usage of LUTs must be minimal when the target design environment is FPGA. To accomplish low complexity, high speed, an optimized resource efficient address generator for the channel De-Interleaver is proposed. The floor function and modulo operator assocated with the complex mathematical steps is very difficult to implement in FPGA. In order to eliminate the modulo and floor functions, a simple algorithm along with mathematical background is developed. The organization of the rest of the paper is as follows:
Section II gives a comparative analysis of various address generation techniques and their limitations, Section III gives the principle of proposed work, Section IV gives applications and the conclusion of the paper is given in Section V.

II. COMPARITIVE ANALYSIS OF DIFFERENT ADDRESS GENERATION TECHNIQUES

A. LUT based technique:

This technique aims at fully improved FPGA implementation of LUT(Look Up Table) based design. It supports all possible modulation schemes. The Address generator used here involves two complex mathematical steps which includes modulo and floor functions associated with it. As FPGA implementation of these complex functions are not possible, MATLAB(Matrix Laboratory) is used for writing the address. Four LUTs are required to store the Interleaver's Addresses. Interleaver's action is modeled using Finite State Machine[2]. In order to generate proper address for the modulation type, another LUT has to be implemented. It performs better in terms of operating frequency and is found to be 141.63MHz

Limitation:

- This supports only three possible code rates, ½, 2/3, ¾ and four interleaver depths.
- In order to achieve better operating frequency and support all modulation schemes bulkier hardware is required.
- Bulkier hardware limits the paper in presenting the output for a single modulation technique.
- Due to complex mathematical functions MATLAB is used.
- Additionally, FSM is used.

Another modified LUT technique was proposed[6] in which improvement is seen in terms of memory blocks where the addresses were generated reducing the bulkier hardware and use of FSM(Finite State Machine) was avoided and the operating frequency was increased. But the Interleaving depth became fixed and LUTs had to be implemented for alternate modulation scheme and the task became tedious.

B. FSM Based Technique

The address generation in this method involves complex mathematical steps associated with modulo and floor functions. As this cannot be implemented on FPGA, FSM is made use of in order to ease this technique. This supports all the modulation schemes, varying Interleaver depths(ID) and code rates. Any change in the value of ID, modulation type, the interleaver follows a different path or else the FSM will follow the same route of transition and the same set of interleaver addresses will be continuously generated. When

the FSM at this level reaches to the terminal value of that iteration, it goes to the preset state in order to continue the process. Preset state/ Preset Logic is used to generate the correct beginning addresses. Now hardware is generated depending upon the FSM[9].

Limitation

- FSM is very difficult to maintain without a well thought out design and a larger system is difficult to manage and implement using FSM.
- It is not suited to all problem domains. It can be used only when states, conditions and transitions are well defined.
- It is a lengthy procedure and conditions must be fixed for developing FSM.

C. 2D Realization of Interleaver

Since the modulo and floor function's direct computation is hardware inefficient, it is necessary to consider the two steps as one step and find the correlation between input and output which should be hardware efficient. 1 Dimensional equation is realized into a joint 2 Dimensional expression. Transformation of both the set of equations to 2-D space is not required as they are the inverse of each other. Thus only one set of equations can be transformed for efficient hardware implementation and same can be used for other by just swapping the order of read and write of data into memory.

It suits for all modulation schemes and avoids the bulky hardware[7].

Limitation

- Due to 2D realization, number of mathematical steps associated with the interleaver function increases and due to presence of modulus and floor operators within the interleaver functions use of standard algebraic rules does not work always.
- Different code rates and interleaver depths are not supported.

D. Dual mode Deinterleaver

The address generation is done for two kinds of deinterleaver cases adopted by the IEEE 802.16e and DVB(Digital Video Broadcasting) standards. Both the designs are integrated. In error control circuits, both standards can share the same decoder modules. The 6 bits of output of each cycle are placed at separate memory addresses which necessitates the need of multiple ports resulting in overhead and limited throughput. This paper addressses low cost solution is provided by splitting the data into seperate memory banks, i.e., use of single port memory. The same design can be extended for various other interleaver designs. Convolutional interleaving scheme is also an equally important interleaving technique along with block interleaving. The DVB standards adopt the convolutional interleaving which composes of 12 data transmission branches, cyclically connected to the input byte-stream set by the switch. As each branch holds different input data with different delay, each branch can be simply regarded as a FIFO. Both DVB and IEEE 802.16e standards provides very high speed wireless data transmission[8].

Limitation:

- The direct implementation of FIFO(First In First Out) based on the shift registers not only occupies lots of area but also dissipates great switching energy.
- Transformation of FIFO suffers control overhead and cause low memory utilization of memory cell.
- Integration of IEEE 802.16e and DVB standards causes overhead

E. Multimode Block Interleaver

The paper[5] gives a comparative view about Traditional and newly proposed Interleaver architecture. First part addresses the Traditional block Interleaver where input bits are written sequentially and then read in the order defined by the LUT. For deinterleaving the bits are written according to the LUT and then read sequentially. The second part gives a description about the new novel Interleaver hardware efficient Interleaver. This is more suitable for operation as an accelerator unit for a programmable processor. The architecture is based on a special matrix memory block where words are written as rows but read as columns. A complete row can be written in one clock cycle and a complete column can be read. Intra-row and intra column permutations are carried out before reordering the bits. This architecture gives better performance, consumes less power and cost effective.

Limitation

- Traditional Block Interleaver can address only 1 bit at a time and complete interleaving sequence of every interleaving scheme has to be stored explicitly in the LUT, making it relatively large if many modes have to be supported.
- In the newly proposed interleaver addresses are generated only if the interleaver is compatible with the processor world length. It is not as general as traditional Interleaver because unlike the formal method changes cannot be made easily by changing the values in LUT.

F. Hardware Efficient Architecture for WiMAX

The paper[2] shows the implementation of interleaving in Hardware. Instead of using Traditional Block Interleaver where every bit has to read and written one at a time making the ROM take very large area consuming enormous power, the proposed architecture uses multi-bank 2D memory where a complete row or column can be read or written in single clock cycle. With efficient permutation logic and ROM less hardware, proposed hardware architecture realizes interleaving with low area and power. LUT ROM is completely avoided and address generation circuits are made very simple.

Limitation:

- Though the complete row can be written and entire column can be read in a single clock cycle, only a width 3 bit for row and 4 bit for column can be accessed.
- This technique neither addresses the issue of interleaving depths nor supports any code rate.

G. IEEE 802.16e Interleaver

The paper[4] proposes a new and different approach for address generation in IEEE(Institute of Electrical and Electronics Engineers). Basically three different techniques are designed to implement the interleaving addresses in the address generator. They are

- State machine implementation.
- Direct Implementation.
- Pattern tracking implementation.

First two methods have been implemented already and hence this paper follows the new third method. In this method, Patterns follow a certain set of rules like:

- Each pattern should begin with by zero, each group begins by start value of the previous group plus one.
- Each adjacent 16 numbers construct one group, within the group the successive numbers have a relation.

Limitation:

- Lack of mathematical calculations makes it difficult to analyse the pattern in which addresses are generated.
- Though the area consumed is less, patterns have to be generated everytime for each and every modulation technique and different code rates, so this becomes a time consuming task.

With the various methods mentioned, the following method gives an alternative, suitable, user friendly & innovative methodology as an improved version used in generation of address for WiMAX Deinterleaver.

III. PRINCIPLE OF WIMAX DEINTERLEAVER

Considering the limitations of various methods, this paper describes a simple algorithm for address generator with its mathematical background[10]. Here the number of rows, d is fixed, given by d=16 where as the number of columns are given by Ncbps/d. The mathematical foundation of the correlation between the addresses is represented in the following way given by (1)-(3), i.e.,

$$k_{n,\text{QPSK}} = \{\, d*i+j \quad \text{for } \forall\, j \text{ and } \forall\, i \tag{1}$$

$$k_{n,\text{16-QAM}} = \begin{cases} d*i+j & \text{for } j\%2 = 0 \text{ and for } \forall\, i \\ d*(i+1)+j & \text{for } j\%2 = 1 \text{ and} \\ & \text{for } i\%2 = 0 \\ d*(i-1)+j & \text{for } j\%2 = 1 \text{ and} \\ & \text{for } i\%2 = 1 \end{cases} \tag{2}$$

$$k_{n,\text{64-QAM}} = \begin{cases} d*i+j & \text{for } j\%3 = 0 \text{ and for } \forall\, i \\ d*(i-2)+j & \text{for } j\%3 = 1 \text{ and} \\ & \text{for } i\%3 = 2 \\ d*(i+1)+j & \text{for } j\%3 = 1 \text{ and} \\ & \text{for } i\%3 \neq 2 \\ d*(i+2)+j & \text{for } j\%3 = 2 \text{ and} \\ & \text{for } i\%3 = 0 \\ d*(i-1)+j & \text{for } j\%3 = 2 \text{ and} \\ & \text{for } i\%3 \neq 0 \end{cases} \tag{3}$$

where j=0,1,2….d-1 and i=0,1,2…..(N_{cbps}/d)-1 represents the row and column numbers. N_{cbps} is the number of coded bits per subcarrier, kn represents the deinterleaver addresses. The outcome of this analysis gives the final addresses for the Deinterleaver. The equations (1)-(3) play a vital role in establishing the formal mathematical foundation of the proposed algorithm. The toplevel structure of the Deinterleaver address generator address generator is shown in figure 1 which supports various modulation schemes like QPSK(Quadrature Phase Shift Keying), 16-QAM(Quadrature Amplitude Modulation) and 64 QAM for any possible code-rate. Logical circuits are developed for every modulation scheme and our design. The design is optimized in the sense that common logic circuits such as multiplier, adder, column counter and row counter are shared between the three modulation schemes while generating the addresses for them. The incrementer and decrementer blocks are shared between 16-QAM and 64 QAM.

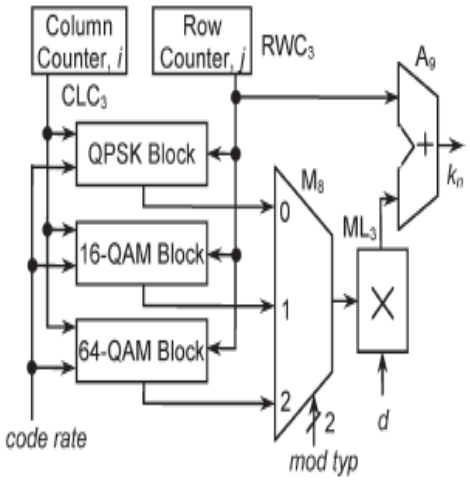

Fig 1 : Top Level view of complete De-interleaver Address generator

The programming is done in verilog in Xilinx ISE simulator and implemented on Spartan 3 FPGA. Since the implementation is on FPGA, the product can be easily upgraded by making changes in (Hardware Description Language)HDL[2]. FPGA is chosen for implementation because the TAT(Turn Around Time) of FPGA is less than that of ASIC(Application Specific Integrated Circuit).

IV. APPLICATIONS

- The most important application offered by WiMAX technology is business consumer connectivity and backhaul WiMAX technology.
- WiMAX is a major part of wireless broadband future because of the flexibility it promises [11].
- WiMAX technology can be used to present data, video, voice, mobile and internet enabling the users to get access to media, visitors and employees.
- The implementation is in FPGA, which offers internal embedded storage for potential applications like FIFO, Data buffers, stack.

V. CHALLENGES IN DEINTERLEAVER DESIGN

Deinterleavers used in different standards like WLAN, 802.11, LTE, HSPA, WiMAX have different structures and permutations. They have wide range of Interleaving block sizes and algorithms. It encounters high percentage of memory conflicts. It becomes difficult to converge to a single architecture supporting concurrent operations for multiple standards. Deinterleavers are very complexs it requires preprocessing with every change[12]. This preprocessing is associated with some extra cycle cost before starting actual deinterleaving. All these challenges have to be overcome to compute an efficient deinterleaver circuit for address generation.

VI. CONCLUSION

This paper shows the various techniques of address generation and an optimized method to overcome the limitation of the previous methods, a novel method employing a simple algorithm with its mathematical foundation has been proposed which shows the significance of our work. The address generation circuitry discussed supports all possible code rates and modulation techniques.

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