International Journal For Technological Research In Engineering
Volume 2, Issue 7, March-2015 *ISSN (Online): 2347 - 4718*

DESIGN AND IMPLEMENTATION OF A CASCADED H-BRIDGE MULTILEVEL INVERTER BY FPGA CONTROLLER FOR PHOTO VOLTAIC APPLICATION

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Abstract: Multilevel Inverters are emerging technology playing a vital role in power electronics, Electric drive systems and Power systems etc. Here new multilevel topology is discussed. Cascaded H- Bridge (CHB) 7 level inverter is designed using Simulink, finally it is simulated and inverter switching signals are controlled using FPGA controller. H-bridges are connected seriously to achieve 7 level output voltage, Sinusoidal Pulse Width Modulation (SPWM) scheme is employed to control the inverter switching signals. This topology is tested in Mat lab/Simulink environment. Total Harmonic Distortion (T.H.D) value is reduced to 19% compared with 3 level inverter (46%). Solar Photo Voltaic system employed to compete disadvantages of conventional sources and resulted in energy conservation system that reduces power consumption.

Keywords: Multilevel Inverter, Cascaded H- Bridge, Sinusoidal Pulse Width Modulation, Total Harmonic Distortion, FPGA controller, Photo Voltaic System, Xilinx System Generator Tool.

I. INTRODUCTION

The Inverter is a power electronic circuit that converts direct current (DC) to alternate current (AC) of desired magnitude and frequency. The inverter find their application in ac motor and uninterruptible power supplies. Multi level Inverter technology has emerged recently an alternative in area of high power medium voltage energy control. Multilevel inverters have grown better counterparts to conventional two-level inverters. Commonly employed multilevel inverter topologies are Diode clamped, Capacitor clamped and Cascaded Multilevel inverters. In all these topologies, output voltage is synthesised from several levels of input voltages obtained from several capacitors connected across the dc bus. The Multi level inverter is used for industrial applications as alternative in high power and medium voltage situations. The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. Figure 1 shows the circuit for a diode clamped inverter for a three-level inverter. The key difference between the two-level inverter and the three-level inverter are the diodes D1 and D2. These two devices clamp the switch voltage to half the level of the dc-bus voltage. In general the voltage across each capacitor for an N level diode clamped inverter at steady state is vdc/(n-1) Although each active switching device is only required to blockV, the clamping devices have different ratings. The diode-clamped inverter provides multiple voltage levels through connection of the phases to a series of capacitors. According to the original invention, the concept can be extended to any number of levels by increasing the number of capacitors. Early descriptions of this topology were limited to three-levels where two capacitors are connected across the dc bus resulting in one additional level. The additional level was the neutral point of the dc bus, so the terminology neutral point clamped (NPC) inverter was introduced. However, with an even number of voltage vdc / (n-1) levels, the neutral point is not accessible, and the term multiple point clamped (MPC) is sometimes applied . Due to capacitor voltage balancing issues, the diode-clamped inverter implementation has been limited to the three levels. Because of industrial developments over the past several years, the three level

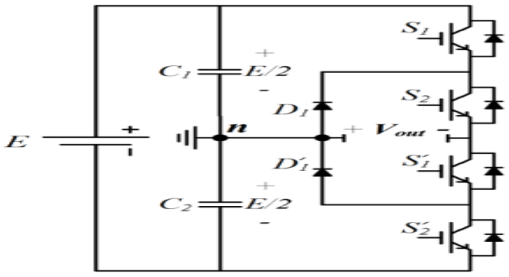

Figure: 1 Basic circuit of Diode clamped Multi Level Inverter

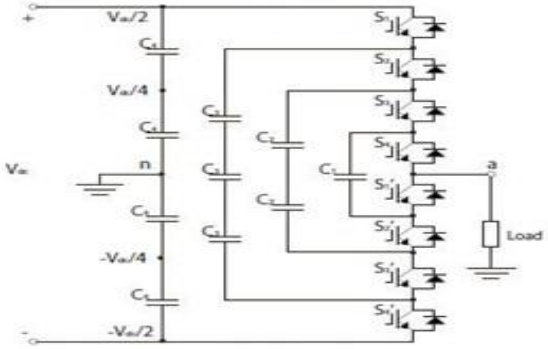

Figure: 2 Basic circuit diagram of flying capacitor Multi Level Inverter.

The cascaded-H- bridge inverter where a seven level H bridge cell is connected in series with a three-level cell. The complete topology involves three phases. This is a combinational topology in a couple of senses. First, the five-level cell is a combination of the diode-clamped and H-bridge topologies. Next, the five level cells are inserted into the series H-bridge inverter in place of a three-level cell. In general any number of cells having any number of levels is possible. The dc voltage ratio can be selected to maximize the number of voltage levels. However, the maximum case suffers from the disadvantage that negative dc currents in the lower voltage cell will distort the dc voltage if a transformer/rectifier source is used to supply vadc2. One solution to this problem is to use a ratio of vadc1 = 4vadc2 instead which reduces the number of voltage levels to eleven. The per-phase RSS can be used to avoid negative dc source currents. Also, per-phase RSS within the five-level cell can be used to ensure that each of the capacitors is charged to one-half of the supply voltage vadc1. In general, any number of cells can be placed in series and only one isolated dc source is needed per phase. If the number of voltage levels is lowered to nine. lt shows that both cells are switching at nearly the same frequency.

II. 7 LEVEL CASCADED H-BRIDGES MULTI LEVEL INVERTER

A solar panel is a set of solar photovoltaic (PV) modules electrically connected and mounted on a supporting structure. A PV module is a packaged, connected assembly of solar cells. Solar panels can be used as a component of a larger photovoltaic system to generate and supply electricity in commercial and residential applications. Each module is rated by its DC output power under standard test conditions (STC), and typically ranges from 100 to 320 watts. The efficiency of a module determines the area of a module given the same rated output - an 8% efficient 230 watt module will have twice the area of a 16% efficient 230 watt module. There are a few solar panels available that are exceeding 19% efficiency. A single solar module can produce only a limited amount of power; most installations contain multiple modules. A photovoltaic system typically includes a panel or an array of solar modules, an inverter, and sometimes a battery and/or solar tracker and interconnection wiring. Solar modules use light energy (photons) from the sun to generate electricity through the photovoltaic effect. The majority of modules use wafer-based crystalline silicon cells or thin-film cells based on cadmium telluride or silicon. The structural (load carrying) member of a module can either be the top layer or the back layer. Cells must also be protected from mechanical damage and moisture. Most solar modules are rigid, but semi-flexible ones are available, based on thin-film cells. These early solar modules were first used in space in 1958. Electrical connections are made in series to achieve a desired output voltage and/or in parallel to provide a desired current capability. The conducting wires that take the current off the modules may contain silver, copper or other non-magnetic conductive transition metals. The cells must be connected electrically to one another and to the rest of the system. Externally, popular terrestrial usage photovoltaic modules use MC3 (older) orMC4 connectors to facilitate easy weatherproof connections to the rest of the system. Bypass diodes may be incorporated or used externally, in case of partial module shading, to maximize the output of module sections still illuminated. Some recent solar module designs include concentrators in which light is focused by lenses or mirrors onto an array of smaller cells. This enables the use of cells with a high cost per unit area (such as gallium arsenide) in a cost-effective way.

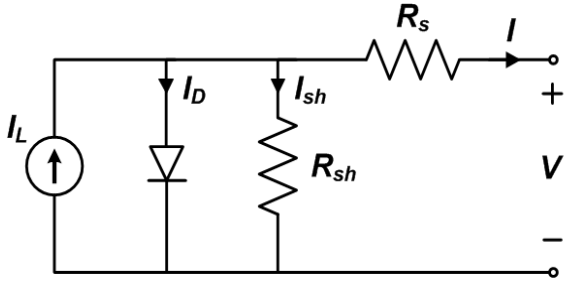

Figure: 3 Equivalent circuit diagram PV system

Photovoltaic cell consist of PN junction that when exposed to light releases electrons. The solar cell can be modeled as a current source parallel with a forward biased diode. The diode current Id is varies with the junction voltage Vd and the cell reversesaturation current Io. In practical , solar cell is not ideal diode so there is some losses .In real cells, the effect is degraded by the presence of series resistanceRs and parallel resistance Rsh . Series resistance Rs is very small, which arises from the ohmic contact between metal andsemiconductor internal resistance. But Shunt resistance Rsh is very large and represents the surface quality along the periphery.Leakage of current through the periphery represents Ish. Both the diode current Id and shunt current Ish given by the photocurrentIph. In ideal case Rs is 0 and Rsh is ∞. The resultant current relationships are in the following equation, as dictated by Kirchhoff'sCurrent Law [1]

$$I = Iph – Id – Ish \ldots\ldots\ldots (1)$$

III. CONTROLLING METHOD

Usually, the on- and off-states of the power switches in one inverter leg are always opposite. Therefore, the inverter circuit can be simplified into three 2-position switches. Either the positive or the negative dc bus voltage is applied to one of the motor phases for a short time. Pulse width modulation (PWM) is a method whereby the switched voltage pulses are produced for different output frequencies and voltages. A typical modulator produces an average voltage value, equal to the reference voltage within each PWM period. Considering a very short PWM period, the reference voltage is reflected by the fundamental of the switched pulse pattern.In regular sampling technique, the reference waveform is sampled at regularly spaced intervals. Normally, the sampling take places at the triangular waveform peaks. With one sample per carrier cycle the output is a double edge modulated waveform, which is symmetrical with respect to the centre point between the two

consecutive samples. The modulation process is termed symmetrical modulation because the intersection of adjacent sides of the triangular carrier waveform with the stepped sine wave, about the non-sampled carrier peak, is equidistant about the carrier peak. figure 1.3 illustrating the general features of symmetrical sampling PWM. A very popular method of controlling the voltage and frequency is by sinusoidal pulse width modulation. The amplitude and frequency of the output voltage are varied, respectively, by varying the amplitude and frequency of the reference sine waves. The ratio of the frequency of the sine wave to the frequency of the carrier wave is called the modulation index. The carrier and reference wave are mixed in a comparator. When sinusoidal wave has magnitude higher than the triangular wave, the comparator output is high, otherwise it is low.

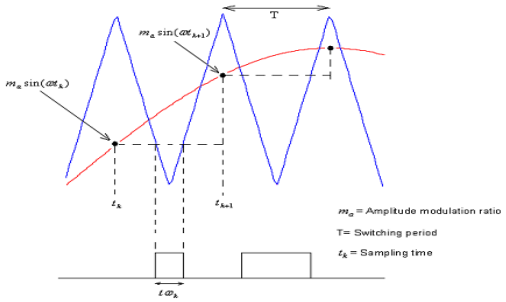

Figure: 4 Symmetrical regular PWM

IV. XILINX SYSTEM GENERATOR TOOL:

System Generator is a DSP design tool from Xilinx that enables the use of the Math Works model-based Simulink design environment for FPGA design. Designs are captured in the DSP friendly Simulink modelling environment using a Xilinx specific block set. System Generator is a system-level modelling tool that facilitates FPGA hardware design. It extends Simulink in many ways to provide a modelling environment that is well suited to hardware design. The tool provides high-level abstractions that are automatically compiled into an FPGA at the push of a button. The tool also provides access to underlying FPGA resources through low-level abstractions, allowing the construction of highly efficient FPGA designs. System Generator allows device-specific hardware designs to be constructed directly in a flexible high-level system modeling environment. In a System Generator design, signals are not just bits. They can be signed and unsigned fixed-point numbers, and changes to the design automatically translate into appropriate changes in signal types System Generator allows designs to be composed from a variety of ingredients. Data flow models, traditional hardware design languages (VHDL and Verilog), and functions derived from the MATLAB programming language, can be used side-by-side, simulated together, and synthesized into working hardware. System Generator simulation results are bit and cycle-accurate. System Generator simulations are considerably faster than those from traditional HDL simulators, and results are easier to analyze. A Simulink block set is a library of blocks that can be connected in the Simulink block editor to create functional models of a dynamical system. For system modelling, System Generator block sets are used like other Simulink block sets. The blocks provide abstractions o mathematical, logic, memory, and DSP functions that can be used to build sophisticated signal processing (and other) systems. There are also blocks that provide interfaces to other software tools (e.g., FDATool, ModelSim) as well as the System Generator code generation. The Xilinx Block set is a family of libraries that contain basic System Generator blocks. Some blocks are low-level, providing access to device-specific hardware. Others are high- level, implementing (for example) signal processing and advanced communications algorithms. Modelling Specifies the relationship between the Simulink-based simulation of a System Generator model and the behaviour of the hardware that can be generated from it. Timing and Clocking Describes how clocks are implemented in hardware, and how their implementation is controlled inside System Generator. Synchronization Mechanisms Describes mechanisms that can be used to synchronize data flow across the data path elements in a high-level System Generator design, and describes how control path functions can be implemented.System Generator provides direct support for MATLAB through the M Code block. The M Code block applies input values to an M-function for evaluation using Xilinx's fixed-point data type. The evaluation is done once for each sample period. The block is capable of keeping internal states with the use of persistent state variables. The input ports of the block are determined by the input arguments of the specified M-function and the output ports of the block are determined by the output arguments of the M-function. The block provides a convenient way to build finite state machines, control logic, and computation heavy systems. In order to construct an M Code block, an M-function must be written.

V. SIMULATION DESIGN AND RESULT ANALYSIS

Simulation is an effective tool by which we can experience the practical results through the software. There is a number of simulation software available, and the most efficient tool is the MATLAB. Here we have a number of parts of MATLAB. We employ the Simulink part of the MATLAB.MATLAB is a software package for computation in engineering, science, and applied mathematics. It offers a powerful programming language, excellent graphics, and a wide range of expert knowledge. MATLAB is published by and a trademark of The Math Works, Inc The focus in MATLAB is on computation, not mathematics: Symbolic expressions and manipulations are not possible (except through the optional Symbolic Toolbox, a clever interface to maple). All results are not only numerical but inexact, thanks to the rounding errors inherent in computer arithmetic. The limitation to numerical computation can be seen as a drawback, but it's a source of strength too: MATLAB is much preferred to Maple, Mathematical, and the like when it comes to numeric's.

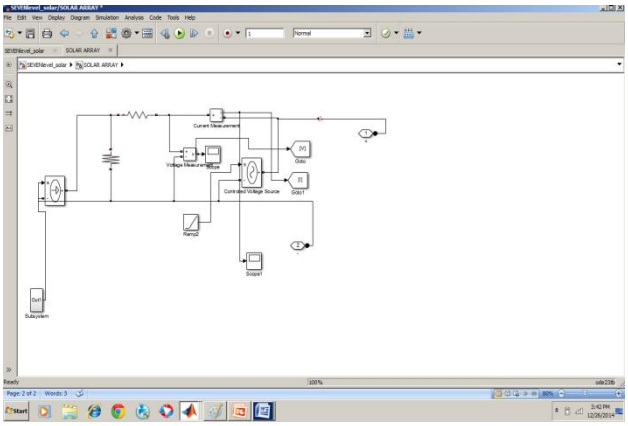

Figure: 5 Simulation diagram of PV module

Figure: 6 shows the complete simulation diagram of Cascaded H-bridge 7 level Multilevel inverter circuit. Actually these three H-bridges are developed in Sub system block in order to reduce the complexity of understand. Figure: 7 shows 7 level output voltage waveform which looks like a near sinusoidal voltage. The harmonics content in the proposed system is 19% which is very less compared with 3 level inverter where T.H.D will be 46%.

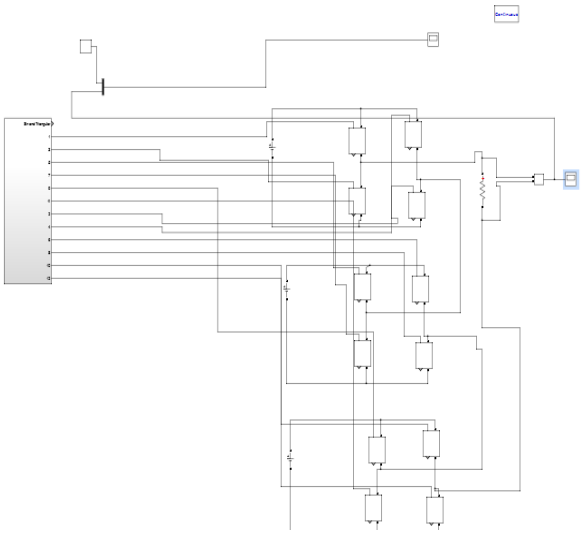

Figure: 6 Simulation diagram of Proposed C.H-B. 7 level inverter

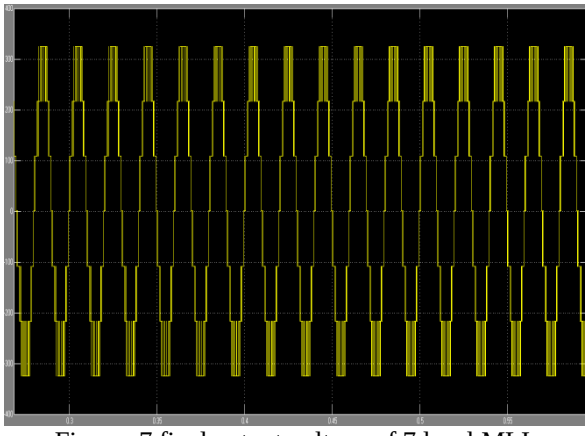

Figure: 7 final output voltage of 7 level MLI

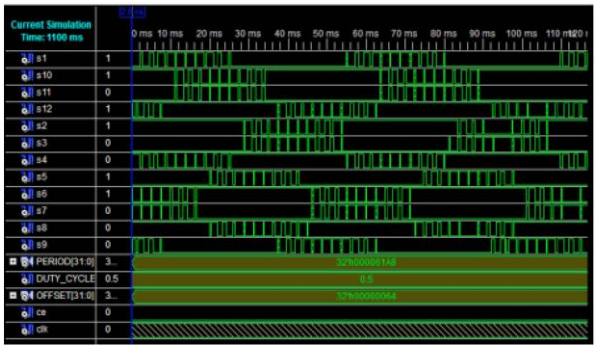

Figure: 8 Simulation diagram triggering pulse generated by Xilinx System Generator Tool

Table: 1
T.H.D comparison of different MLI toplogy

S.no	Type of MLI	T.H.D
1	Diode clamped MLI	23%
2	Flying capacitor MLI	22.5%
3	Proposed MLI	19.35

From table No 1 we can analyse the various MLI topologies and their T.H.D minimization percentage. Among three method proposed MLI has much reduced T.H.D.

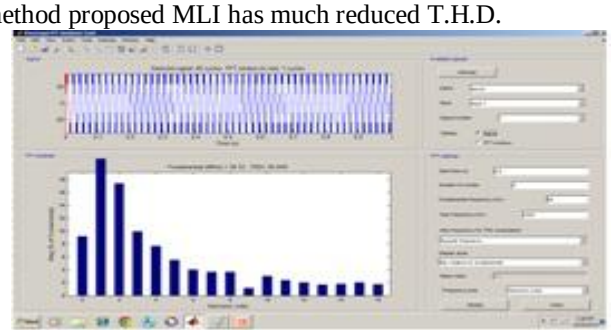

Figure: 9 FFT analysis of Line voltage of proposed MLI topology

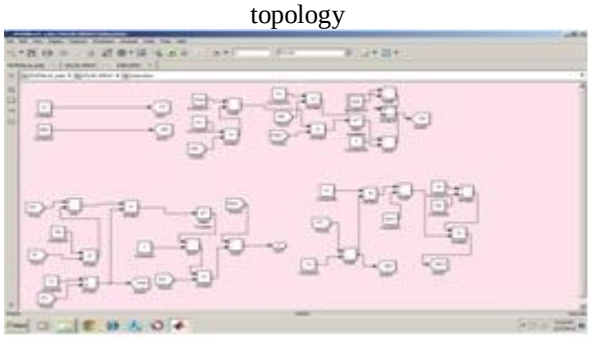

Figure: 10 Simulation diagram of PV sub module

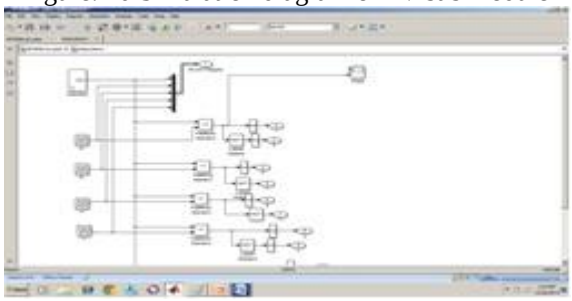

Figure: 11 Simulation diagram PWM Scheme

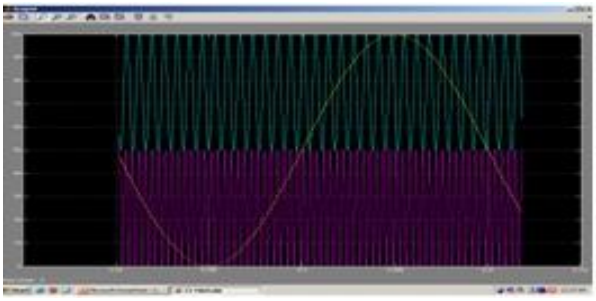

Figure: 12 Simulation Diagram of Modulation Scheme

Figure: 12 Sinusoidal Pulse Width Modulation Scheme

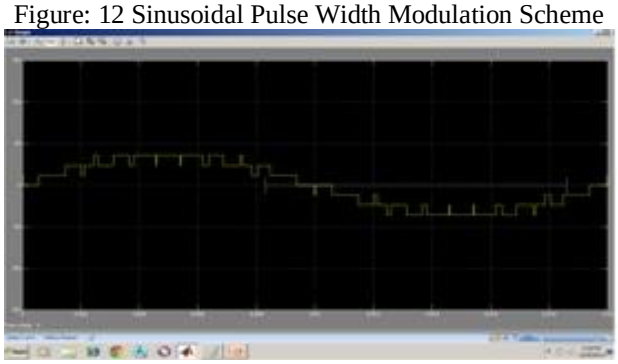

Figure: 13 Triggering Pulse Generated By FPGA

VI. CONCLUSION

Thus photo voltaic submodule to control inverter switches of multilevel inverter and results are verified in simulation. T.H.D comparison of various MLI are performed and found proposed system gives better results.

REFERENCES

[1] J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galvan, R. C. P. Guisado, Ma. A. M. Prats, J. I. Leon, N. Moreno-Alfonso, "Power- Electronic Systems for the Grid Integration of Renewable Energy Sources: A Survey," IEEE Transactions on Industrial Electronics, vol. 53, no. 4, pp. 1002-1016, June 2006.

[2] A. J. Morrison, "Global Demand Projections for Renewable Energy Resources," IEEE Canada Electrical Power Conference, 25-26 Oct. 2007, pp 537

[3] J. Rodriguez, S. Bernet, Bin Wu, J. O. Pontt, S. Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives, " IEEE Transactions on Industrial Electronics, vol. 54, no. 6, pp. 2930-2945, Dec. 2007.

[4] L. M. Tolbert, F. Z. Peng, "Multilevel Converters as a Utility Interface for Renewable Energy Systems," IEEE Power Engineering Society Summer Meeting, Seattle, Washington, July 15-20, 2000, pp. 1271

[5] S. Khomfoi, L. M. Tolbert, "Multilevel Power Converters," Power Electronics Handbook, 2nd Edition Elsevier, 2007, ISBN 978-0-12- 088479-7, Chapter 17, pp. 451-482.

