

A REVIEW ON MULTIPLE BIT ERROR CORRECTION USING BCH CODES

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Abstract: *In the present Digital Communication systems, it is highly possible that the data or message get corrupted during transmission and reception through a noisy channel medium. The environmental interference and the physical defects in the medium are the main causes of the data or message corruption in the communication medium, which leads to the injection of random bits into the original message and corrupt the original message. To overcome these problems during data transmission a high-speed BCH (Bose-Chaudhuri-Hocquenghem) decoder is used that corrects double-adjacent and single-bit errors in parallel, and serially corrects multiple-bit errors other than double-adjacent errors.*

Index Terms: *Error correcting code (ECC), double-adjacent error correction (DAEC), BCH codes, parallel decoder.*

I. INTRODUCTION

ERROR control codes (also known as error correcting codes, ECCs) have been frequently used to improve the dependability of a memory system [1], [2]. The error correction is based on mathematical formulas, which are used by Error correcting codes (ECC). Error correction is done by adding parity bits to the original message bits during transmission of the data. However, the dependability of a memory system still remains a concern due to neutron induced single event upsets (SEUs) [3] and the occurrence of multiple-bit. Jose Maiz, Scott Hareland, Kevin Zhang and Patrick Armstrong [4] stated that Single Event Upsets (SEU) and Soft Errors (SE) generated by ionizing particles or neutron interactions with semiconductor devices have been identified as a critical and possibly dominant failure mechanism in modern CMOS circuits. Error detection and correction schemes in memories and microprocessor caches are common and drastically reduce the externally observable error rate. A key consideration for these protection schemes is the treatment of multiple bit errors that can be generated when adjacent bits fail as a result of a single strike. These events can prevent the detection of an error in a parity protected, or make an uncorrectable error in spite of the use of Error Correction Codes (ECC). Bit interleaving is commonly used to minimize the error rate contribution of multi-bit errors. Song-Chul Jang, Je-Hoon Lee, Won-Chul Lee and Kyoung-Rok Cho [5] stated that BCH (Bose-Chaudhuri-Hocquenghem) coding is very useful to correct a small bit error. But the code length n is longer as in a game program stored in a MLC (multi-level cell) flash memory, for which the decoding circuits takes a lot of computation time. The error patterns of flash memories are almost random

error. Long BCH code can correct the random error. While a conventional binary BCH decoder is operating at very high frequency, it suffers from the serial-in and serial-out limitation. The parallel decoding architecture of BCH code speeded up the 2-bit error correction. Multiple -bit error correction of a BCH code needs a low-speed serial decoding process. BCH codes can be decoded faster by parallelizing the serial operations [6], [7], but parallelization incurs a large hardware overhead, particularly for long information bit length. Moreover, it is well known that the BCH code is less efficient for short information bit lengths [8]. There are few multiple-bit error correcting codes that can be decoded in parallel, e.g., product codes and some low-density parity-check (LDPC) codes, such as orthogonal Latin square (OLS) codes [1], Euclidean geometry LDPC (EG-LDPC) codes [9] and difference -set cyclic codes (DSCC) [10]. However, they require longer check bits than BCH codes. To resolve these issues, Wilkerson et al. [8] have proposed a high speed decoding scheme for the BCH code. This scheme utilizes parallel decoding when no error or a single-bit error occurs, and serial decoding when multiple-bit errors occur. As single-bit errors occur more often, this scheme achieves high-speed decoding for most errors.

II. BCHCODES

BCH (Bose, Chaudhuri, Hocquenghem) codes are one of the most well-known binary multiple-error detecting and correcting codes. The error correction is based on mathematical formulas, which are used by Error correcting codes (ECC). Error correction is takes place by adding parity bits to the original message bits during transmission of the data. Because of the addition of parity bits to message bits makes the size of the original message bits longer. Now this longer message bits is called "Codeword". This codeword is received by the receiver at destination, and could be decoded to retrieve the original message bits. Error correcting codes (ECCs) have been frequently used to improve the dependability of a memory system. ECCs dealing with multiple -bit errors are becoming more and more important. The BCH code is one of the best-known and widely used multiple-bit error correcting codes. Multiple -bit error correction of a BCH code needs a low-speed serial decoding process. The BCH code is a cyclic code, and can be decoded serially. However, the high-speed parallel decoding of a BCH code incurs a large hardware overhead. Jang et al. [6] have proposed a BCH decoding scheme in which only some operations are partially parallelized, and overall, it is slower than fully parallelized decoders. Chen et al. [7] have shown a fully parallelized BCH decoder. However, the parallelization

of BCH decoders for long information bit length requires a significant overhead in hardware.

III. DECODING ALGORITHM

Wilkerson et al. [8] have presented a high speed BCH decoding scheme in which code words are decoded in parallel if no error or a single bit error occurs and they are decoded serially only if multiple-bit errors occur. As the probability of occurrence of a multiple-bit error is lower than a single-bit error, this decoding scheme represents a good compromise, because it achieves high-speed operation for the most likely cases of error occurrence.

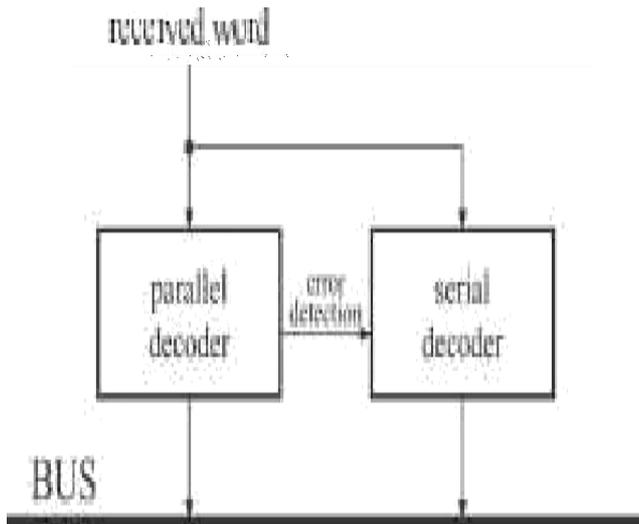


Fig. 1. Diagram of the Wilkerson's BCH decoder.

Fig. 1 shows the block diagram of Wilkerson's BCH decoder. It consists of a parallel decoder and a serial decoder. The parallel decoder decodes the received word. When the parallel decoder detects multiple-bit errors, it generates an error signal that starts the operation of the serial decoder. The parallel decoder detects multiple-bit errors in a single clock cycle, and the serial decoder requires n iterations for an (n, k) BCH code to find the error location (when using the Berlekamp-Massey algorithm). David Hart [11] said that the implemented logic BCH for $(n=63, k=56)$ is capable of correcting 1 bit error and detecting up to 2 bit errors. If the received command is not correctable, then erroneous authentication is prevented providing high probability of correct command execution. Communication system in satellites falls under Telemetry Tracking and Command System (TTC). Telemetry refers to remotely retrieving information from satellites. The data may be either the payload information or housekeeping data. Likewise, telecommand refers to commanding the satellite remotely for aiding it to accomplish its purpose by providing vital uplink. Since satellite link is normally noisy, error control is necessary for significant increase in communication efficiency. Errors normally occur in the physical or the channel layer. Numerous error control techniques have been tested on such noisy links. They are Forward-Error-Correction (FEC) and Automatic-Repeat-Request (ARQ).

FEC adds redundant bits in the message causing bandwidth of message to increase whereas ARQ is set of feedback protocols that notify the transmitter about reception in case FEC fails [11]. The importance of BCH codes is that they are capable of correcting multiple errors over the span of codeword length by a decoding algorithm that is simple and can be realized by reasonable amount of equipment. With respect to satellite communication BCH codes are well suited because:

- Well understood algebraic structure.
- Good hamming distance for given information and code length.
- Easy to implement in hardware.

But this BCH code is capable of correcting 1 bit error and detecting up to 2 bit errors. It is not well suited for work on 3 bit error detection and correction in BCH $(63, 56)$ which involves different algorithm for syndrome generation and error correction.

N. Andreadou, C. Assimakopoulos, and F.-N. Pavlidou [12] implement Bose-Chaudhuri-Hocquenghen (BCH) coding to study the performance of Power Line Channel (PLC) impaired by impulsive noise and AWGN. Quadrature amplitude modulation (QAM) is employed and orthogonal frequency division multiplexing (OFDM) is used as a transmission scheme. Block truncation coding (BTC) is used for the compression of the image. A comparison is made between uncoded system and BCH coding system. To obtain a satisfactory performance of the system, coded OFDM systems like RS (Reed-Solomon), convolutional codes, and turbo codes are adopted. Orthogonal Frequency Division Multiplexing (OFDM) is used for PLC and for high data rate transmission. This is due to its robustness against frequency selective multi-path channels and its error correction ability of channel codes [12]. Consequently, they motivated to implement Bose-Chaudhuri-Hocquenghen (BCH) coding to examine its effect on the performance of PLC channel in the presence of AWGN and impulsive noise. They obtained the results that BCH codes can achieve around additional 0.6 dB coding gain over AWGN channel compared to RS codes. However, when using encoder size of $[63, 16]$, the quality of the image is higher with a degradation in the efficiency of the system. To have a higher quality of the image one may have to sacrifice in the bandwidth depending on the application used. Michelle Effros, Andrea Goldsmith, and Yifan Liang [13] said that Error Correcting Codes are required to have a reliable communication through a medium that has an unacceptable bit error rate and low signal to noise ratio. In Wireless Body Area Network (WBAN), data gets corrupted during the transmission and reception due to noises and interferences. Hence simple block codes like BCH $(n=63, k=51, t=2)$ can be employed in the transceiver design. Claude Shannon proposed the theorem of Channel capacity stating that, "Channel capacity is the maximum rate at which bits can be sent over the channel with arbitrarily good reliability" [13]. According to Channel Coding theorem, "The error rate of data transmitted over a band-limited noisy channel can be reduced to an arbitrarily small amount if the information rate is lower than the channel capacity". Error correcting codes are used in satellite communication, cellular

telephone networks, body area networks and in most of the digital applications. The decoder uses Berlekamp algorithm and Chien Search algorithm. But if they use parallel approach methods, the performance can be improved. It can detect and correct Only up to 2 random errors. G. Smietanka and J. Goetze [14], said that Radio Frequency Identification (RFID) is a wireless communication method mostly used in rough indoor environments. In such environments Forward Error Correction (FEC) is a popular method to improve the transmission quality. However, the common RFID protocol (EPCglobal) only provides error detection based on Cyclic Redundancy Check (CRC) codes. The replacement of this code with an arithmetically similar FEC code improves the transmission and requires only minor changes to the protocol structure. A BCH code fulfills this requirement. They explained BCH decoding using the Chase algorithm which also takes the soft information of the received sequence into account. It is shown that a coding gain of 1 dB is achievable in an RFID transmission application, compared to a transmission with a common BCH code. Also an estimation of the computational complexity when using the Chase algorithm is given as this complexity generally increases with this modification. The EPCglobal uses a CRC code [14] which allows a very reliable error detection but no error correction. Replacing this code with an error correcting BCH code increases the performance of the transmission system. A disadvantage of this BCH code is that it uses only hard-coded bit values for the decoding process. Also it does not explain about different concepts regarding a computational efficient decoding and Codes with iterative decoding like Low-Density-Parity-Check (LDPC) provides an additional coding gain compared BCH codes [14] shown.

IV. CONCLUSION

David Hart[11] said that the implemented logic BCH codes for ($n=63$, $k=56$) is capable of correcting 1 bit error and detecting up to 2 bit errors. But it is not well suited for work on 3 bit error detection and correction. N. Andreadou, C. Assimakopoulos, and F.-N. Pavlidou [12] obtained the results that BCH codes can achieve around additional 0.6 dB coding gain over AWGN channel compared to RS codes. However to have a higher quality of the image one may have to sacrifice in the bandwidth depending on the application used. Michelle Effros, Andrea Goldsmith, and Yifan Liang[13] said that simple block codes like BCH codes for ($n=63$, $k=51$, $t=2$) can be used to reduce error rate of data transmitted over a band-limited noisy channel. But it can detect and correct only up to 2 random errors. G. Smietanka and J. Goetze [14], said that Replacing CRC code with an error correcting BCH code increases the performance of the transmission system. A disadvantage of a this BCH code is that it uses only hard-coded bit values for the decoding process. C.Wilkerson [8] stated that high-speed BCH decoder presents a error correction scheme for correcting double-adjacent as well as single-bit errors in parallel. The decoder resembles Wilkerson's parallel BCH decoder [8] that can correct only single-bit errors. The decoding scheme of [8] operates serially (and hence at low speed) when a multiple-bit error

occurs (including a double-adjacent error).This decoder is fully parallelized BCH decoders capable of correcting any double-bit errors in parallel. The decoder received the data including two bit error. The decoder detects the exact error location and corrects the error. Then it outputs the data without error.

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