

IMPLEMENTATION OF 4-BIT TWO STEP FLASH ADC USING 180nm TECHNOLOGY

Muruges H M¹, Dr Nagesh K N²

¹M.Tech VLSI Design and Embedded Systems, ECE Dept., ²Prof. and HOD ECE Dept. NCET, Bengaluru, India.

Abstract: Analog-to-Digital converters (ADCs) are essential in approximately all communication and signal processing application. In the current paper, it has been shown that a 4-bit Two Step Flash Analog-to-Digital (ADC) which has Flash ADC, Resistor String DAC along with Sample and Hold, all the sub-blocks are implemented using Cadence Virtuoso 180nm technology at an operating voltage of 2V. The simulated results shows a power dissipation of 0.75mw having the input frequency of 1 KHz and input voltage of 2V. The proposed design achieves low power consumption; Conversion time and delay are minimized. This occupation also includes the comparison among One Step Flash ADC and the projected Two Step Flash ADC.

Keywords: Sample and Hold; Flash ADC; Residue Amplifier; Comparatore.

I. INTRODUCTION

A current wireless communication device asks for high data rates with low power consumption and high speed. The important components in the wireless receivers is the analog to digital converter, it is a boundary between analog and digital design. For a System-On-Chip (SOC) application, needed or require a less voltage, less power and more accurate analog -to -digital converters, high speed, less power are most requirements in many wireless applications. A Two Step Flash converter or Parallel Feed-Forward ADC is a type of ADC. The converter of Two Step Flash ADC is separated into two complete Flash ADC's with Feed-Forward circuitry to obtain a better and improved result. In this paper, Flash ADC or Parallel ADC are used because of their speed of converting an analog signal to digital signal is fastest their requirements are suitable for implementation. However Flash converters use a lot of power, have comparatively low resolution, and can be moderately costly. This confines them to high frequency applications that cannot be address in any other technique. Examples contain Data gaining, satellite communications, radar processing, sampling oscilloscope and high concentration disk drives. Two Step Flash ADC approach is the favored design as it reduces area as well as power. High resolution with low area is reachable however at the expense of speed. The speed of the analog -to -digital and digital -to -analog interface must balance with the speed of the digital circuits in organize to fully make use of the advantages of the advanced technologies. Recently low power, compact size and high resolution analog -to -digital interface circuits have been in large demand for convenient system such as camcorders, cellular phones and personal digital support etc. High integration analog -to -digital

interface for portable battery mechanical system require analog -to -digital converters and other interface essentials that dissolve the lowest possible power and operate on supply voltages friendly with the digital parts of the system. Also the rate and performance make it attractive to attain high level of incorporation on a single chip for varied signal processing system. In the earlier time a few of the high speed ADC's have been calculated using bipolar technology, but the manufacture of these devices turn into very complex and large chip area and power. The idea for CMOS is that advanced level of combination and low power are possible then in the bipolar implementation [2].

II. FLASH ADC ARCHITECTURE WITH TWO STEP FLASH ADC APPROACH

On the other hand, we have different architectures of Flash ADC's as confirmed in the literature, but to complete our main goal that is high speed and low power. Two-Step Flash ADC architecture is used. Initially, this architecture improve the speed of our ADC, may be a small bit, but the optimized components enhance the speed to a significant level. In many applications it is essential to have a lesser conversion time ADC. ADC's considered for such application are the high speed ADC's that use the equivalent techniques to reach the shorter conversion period. One way of achieving this is to amplify the speed of the individual components, which will increase the speed of the entire system. The prospective of Two Step Flash architectures for realizing fast, high resolution analog -to -digital converters are established in a number of design in [4,5]&[6].With the alteration rates approaching half those of fully parallel (Flash ADC).

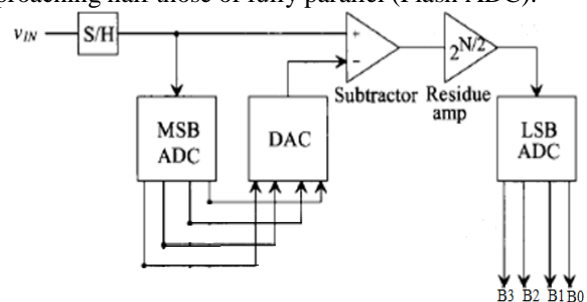


Fig.1 Block diagram 4-bit Two-Step Flash ADC

The fundamental structure of the Two Step Flash converter is shown in Fig.1. The initial converter generates a rough estimation of the value of the input, and the second converter performs a very well conversion. The benefit of this architecture is that the amount of comparators is very much reduced from that of the flash converter from $2^N - 1$

comparators to $2(2^{N/2} - 1)$ comparators. For example, an 8 bit flash converter require 255 comparators, while the step require only 30. The transaction is that the exchange process takes two steps as an alternative of one, with the speed inadequate by bandwidth and settle time necessary by the residue amp and the summer.

III. DESIGN OF SUB-BLOCKS OF TWO STEP FLASH ADC

To get better the speed we optimize the different mechanism of the ADC on your own and by you. The design of the different mechanism of ADC is selected so that when they are cascade together they improve the speed considerably.

Comparator

Comparator is a significant circuit in analog and mixed signal design. The Two Step Flash ADC consists of Flash and Resistor String DAC structural design, in which comparator is used as significant blocks to calculate the result. The two stage operational amp is used as a comparator. The Fig. 2 shows the planned schematic of comparator circuit [2]. The primary stage of the designed comparator consists of two parts, one is biasing circuit to bias the present mirror and another part is differential amp. The second stage is gain stage to get better the gain of operational amp.

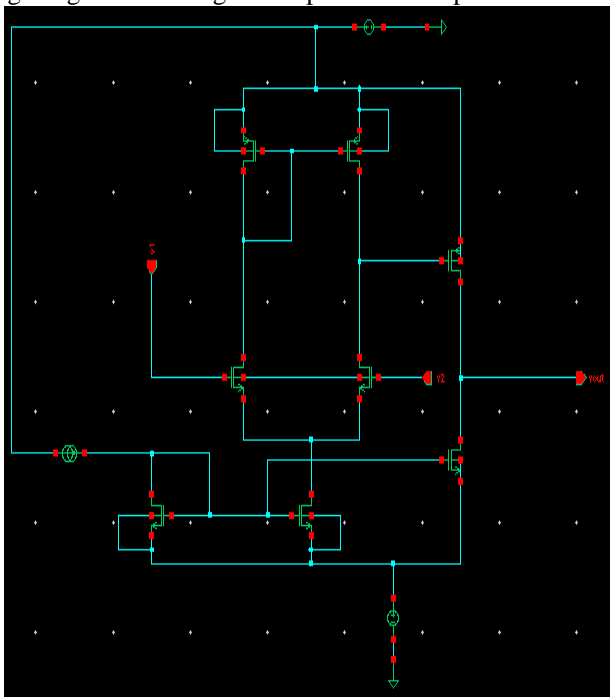


Fig. 2 Schematic of Comparator Circuit.

Flash ADC

Fig.3. shows a classic Flash analog –to -digital Converter schematic diagram. On behalf of an "N" bit converter, the circuit employs $2^N - 1$ comparators. Resistive dividers with 2^N resistors provide the reference voltage. The reference voltage for each one comparator is one least significant bit (LSB) bigger than the reference voltage for the comparators instantly lower it. All comparator produce a "1" while its analog input voltage is higher than the reference voltage

applied to it. Or else, the comparator in Fig.1.output is "0". As shown in Fig. 3, the Flash ADC is composed of three most important components: resistors string, comparators and priority encoder. The analog input voltage is at the same time as compare to the reference voltage levels generated from resistors string and the speed of A/D conversion is consequently maximize. The outputs of comparators appearance a thermometer code (TC) which is a mixture of a sequence of zeros and a sequence of ones, e.g., 0000...0011...1111. Since binary code is typically wanted for digital signal processing, a thermometer code is then altered to a binary code encoder. The rate of such a conventional encoder increases exponentially with the resolution. Optimizations on area rate, circuit latencies and power consumption are very much projected. In this paper we have low power Comparator used in the implementation all through a Comparator Circuit & implementation Specification.

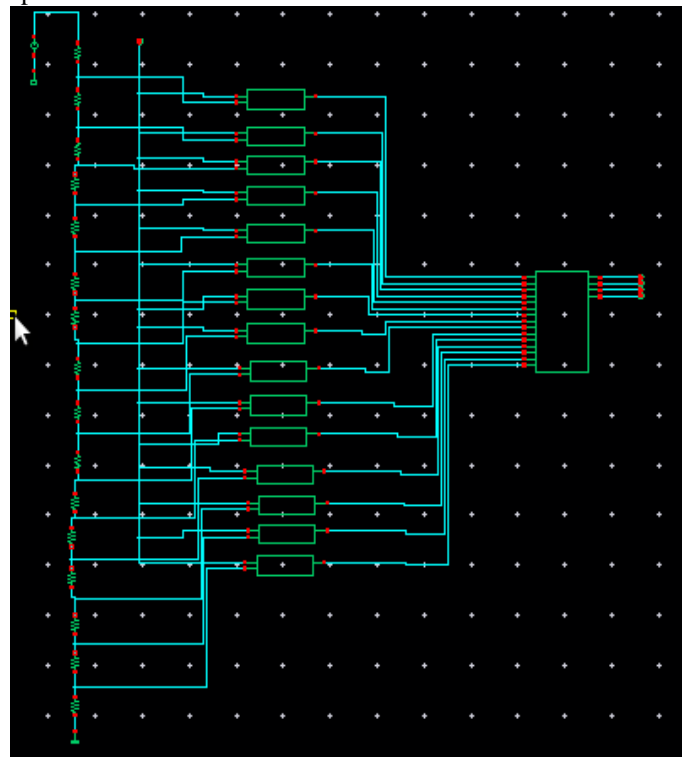


Fig. 3 Schematic of 4-bit Flash ADC with Thermometer code to binary code converter.

Integration of Flash ADC and DAC Circuit

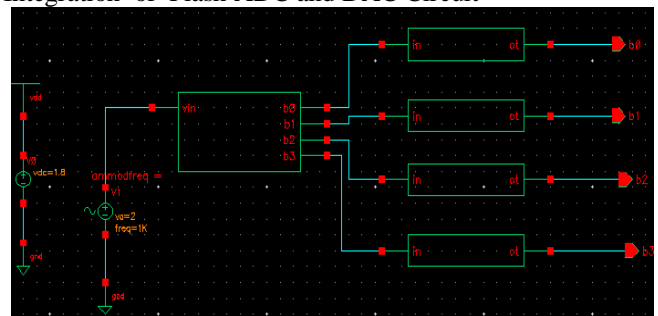


Fig.4 Schematic of Two-Step 4-bit Flash ADC

The Fig. 4 shows the schematic sketch of a 4-bit Two-Step Flash ADC circuit. It consists of inner sub-blocks of Sample and Hold circuit, subtract or with gain stage of residue amplifier, Resistor String DAC, Flash ADC.

IV. RESULTS & DISCUSSIONS

The major reason of our design is to get high speed with low power. The output waveforms obtain for Flash ADC and Two Step Flash ADC are shown in Fig.5, Fig. 6. Reference voltage is in use constant. The simulation has been run on Cadence Virtuoso analog design phase and the implementation was done with 180nm technology. A supply voltage of 2V has been used and the comparisons of the architectures are shown in Table I.

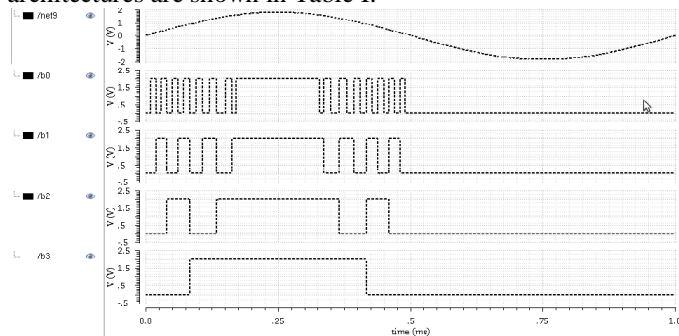


Fig. 5 Simulation result of the 4-bit Flash ADC

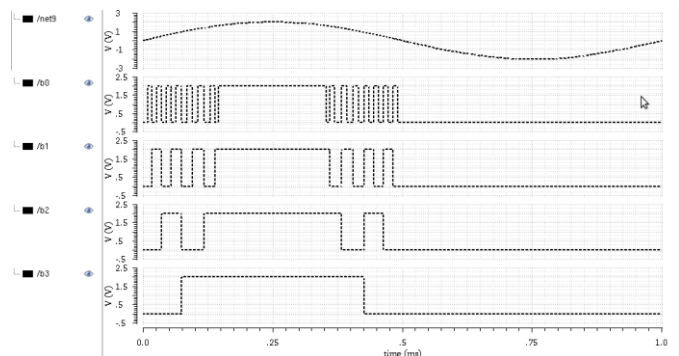


Fig.6 Simulation result of the proposed 4-bit Two Step Flash ADC

Table 1 Comparison Of Flash Adc Vs Two Step Flash Adc

Parameters	Types of ADC	
	Flash ADC	Two Step ADC
Input Voltage	2V	2V
Frequency	1KHz	1KHz
Technology	180nm	180nm
Delay	6.14mw	5.6102mw
Conversion Time	41.014ms	9.012ms
Power Dissipation	4417µw (44.17mw)	750µw (0.75mw)

Table 1, shows the comparison of Two Step Flash ADC with One Step Flash ADC result. From this, it reveals that the proposed Two Step ADC has much better than Flash ADC. It has improved in power dissipation, delay and speed. The power dissipation of implemented Two Step Flash ADC has been calculated as 0.75mw where as existing work dissipation as 44.17mw the conversion time of proposed

work as 9.01ms where as existing work as 41.014ms.

V. CONCLUSION

The work obtainable in this document is to design and examine the performance individuality of the Two Step Flash ADC mechanism. For this propose method are developed for individual mechanism of the analog –to –digital converter. Base on the method developed W/L ratio for all the transistors are considered using the representation parameter of the 180nm CMOS technology. Individual mechanisms are implemented separately. The chosen technology as with the scale of operating voltages to low values down to 2 V, it ensures a high performance circuit. The considered mechanisms are best suitable for a whole Flash ADC. The table I crates a comparison between delay, conversion time and power dissipation with different ADC.

Acknowledgment

The author would like to acknowledge the assist of Dr. Nagesh K N Prof. and HOD Dept of ECE for their support with this development. The author is also thankful of Department of Electronic & communication Engineering, NCET. The mechanism was implemented using cadence tool which is made obtainable by department.

REFERENCES

- [1] Indhudhara Gowda T G, Manasa A, „Design and VLSI Implementation of 8-Bit Pipelined ADC Using Cadence 180nm Technology”. Volume 3 Issue IX, September 2015 ISSN: 2321-9653.
- [2] Ashish Mishra, Dr. V.K Pandey and Kapil Chaudhary, “Designing High Speed Flash ADC by Optimizing its Components”, Volume 1, Issue 2 , July- August 2012 ISSN 2278-6856.
- [3] Arunkumar. P. Chavan, Rekha. G, P. Narashimaraja “Design of a 1.5-V, 4-bit Flash ADC using 90nm Technology”. ISSN: 2249-8958, Volume-2, Issue-2, December 2012.
- [4] K. Lokesh Krishna, T.Ramashri, “VLSI Design Of 12-bit ADC With 1gsps In 180nm Cmos Integrating With SAR And Two-step Flash ADC”. Journal of Theoretical and Applied Information Technology ISSN . 1992-8645 October 2014.
- [5] Panchal S.D, Dr. S.S Gajre, Prof. V .P Ghanwat, “Design and implementation of 4-bit Flash ADC using folding technique in cadance tool” International Journal of Advanced Research in Computer and Communication Engineering Vol. 1, Issue 4, June 2012 ISSN: 2278-1021.
- [6] Pradeep Kumar, Amith Kolhe, “Design & implementation of low Power 3-bit Flash ADC in 0.18um CMOS” International Journal of Soft Computing and Engineering(IJSCE) ISSN: 2231-2307, Volume-1, Issue-5, November 2011.
- [7] Suman Biswas, Jitendra Kumar Das, Rajendra Prasad, “Design and implementation of 4-bit Flash ADC using low power low offset dynamic comparator” 978-1-4799-7678-2/15/31.00 2015

IEEE.

- [8] Manju Devi, Arunkumar P. Chavan, K.N Muralidhara, "A1.5V, 10-bit, 200-MS/s CMOS Pipeline Analog –to –Digital Converter" International Journal of Computer Applications (0975-8887) Volume-88 No.7, February 2014.
- [9] Jorge Guilherme, Joao Vital, Jose E. Franca, "New logarithmic Two-Step Flash ADC with Digital Error Correction for MOS Technology" IST Center for Microsystems, Inegrated Circuis and Systems Group.
- [10] R.Jacob Baker, "CMOS Circuit Design, Layout, and Simulation" Third Edition IEEE series on Microelectronics Systems.
- [11] Channakka lakkannavar, Shrikanth K. Shirakol, Kalmeshwar N. Hosur, "Design, implementation and analysis of Flash ADC architecture with differential amplifier as comparator using custom design approach " International Journal of Electronics Signals and Systems (IJESS) ISSN: 2231- 5969, Vol-1 Iss-3, 2012.
- [12] L. Roi,cado, "A 65nm CMOS 1.2V 6b 1GS/s Two-Step Sub ranging ADC for Ultra Wideband" IST - Technical University of Lisbon ChipIdea Microelectronica, Lisboa, Portugal