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A SINGLE PHASE UNIFIED POWER QUALITY CONDITIONER (UPQC)

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Abstract: This paper proposes a straightforward power circuit topology for single stage bound together power quality conditioner (UPQC). The quantity of force circuit switches of traditional single-stage UPQC is lessened to half and thus it has brought about significant diminishment of cost, weight, volume, security circuits, control misfortunes and control circuit intricacy. The proposed framework adjusts for the utility voltage music, voltage hang and voltage swell. Interim, the proposed circuit could make up for the present music and responsive force of single-stage non-direct loads. A straightforward and quick technique is proposed for the era of remuneration reference voltage of arrangement dynamic channel (SAF) and reference pay current of the parallel dynamic channel (PAF). The said strategy could direct the voltage of DC side capacitors, as well. The notable hysteresis control technique is utilized for exchanging procedure of PAF. An approximated hysteresis control technique is proposed for exchanging methodology of SAF that makes zero voltage exchanging (ZVS) of its switches conceivable amid turn ON. A circuit demonstrate has been reenacted utilizing MATLAB programming to confirm the logical investigation and to demonstrate the capacity and profitable element reaction of the proposed framework in the power quality molding of single-stage utility and non-straight loads.
Index Terms: Unified Power quality conditioner, UPQC, Active filter, Single-phase

I. INTRODUCTION

POWER quality compensators have attracted lots of attention during the last decades, and they have become one of the most important fields of the electrical industry and economy. Power electronic apparatus due to their rapid response, continuous decreasing of their size and price and increasing of their rated voltage and current have been the primary candidate for power quality compensation. Some of the most popular power electronic devices to compensate for power quality in distribution systems are as follows [1-5]:

- Static Var Compensators (SVCs)
- Active Filters (AFs)
- Solid State circuit Breaker (SSB) or Static Transfer Switch (STS)
- Dynamic Voltage Restorer (DVR)
- Distribution Static Converter (D-STATCOM)
- Unified Power Quality Conditioner (UPQC)

Among the mentioned apparatuses, the UPQC is highlighted due to its unique ability in simultaneous compensation for utility voltage and load current. The UPQC in its usual configuration is an integration of a parallel active filter (PAF) and a series active filter (SAF) with a common DC bus. Usually, the PAF compensates for load current, and it regulates the DC bus voltage while the SAF compensates for poor voltage quality of utility [6-11]. This paper proposes a simple single phase power circuit topology for UPQC that is used in single-phase utility with non-linear single-phase loads. The power circuit of UPQC consists of only one single-phase full-bridge inverter, while the conventional single-phase UPQC structure need two single-phase full-bridge inverters with a common DC link [12]. Reduction of switching devices to half would result in considerable reduction of cost, weight, volume, protection circuits, power losses, control circuit complexity and electromagnetic noises. There are two capacitors in the DC side which their middle point is connected to the neutral of utility. A simple control strategy regulates the voltage of capacitors. There are not any mathematical computation blocks or DSP processors. A circuit model has been simulated with MATLAB software. The results show the considerable performance of the proposed circuit in power quality improvement of single-phase utility with non-linear single-phase loads.

II. POWER CIRCUIT CONFIGURATION

Fig. 1 shows the power circuit of proposed UPQC. It consists of a single phase full bridge structure with two DC side capacitors. The middle point of capacitors C_1 and C_2 is connected to the neutral of utility and is considered as the reference point of voltages in the inverter circuit. The two arms of inverter could operate independently. The pair of transistors Q_1 and Q_2 is used for voltage compensation via isolation transformer TR, coupling inductance L_d and filter capacitance C_d for canceling out the undesired voltage harmonics, voltage sag, and swell. Indeed, this part of the power circuit is equivalent with SAF in conventional UPQC topology. The voltage across capacitor C_d, should follow the compensation reference voltage. Using L_d makes it possible to get a smooth voltage variation through C_d. The output capacitor C_d is large enough to have a constant voltage during each switching interval so, the current of inductor L_d varies smoothly and in almost linear form.

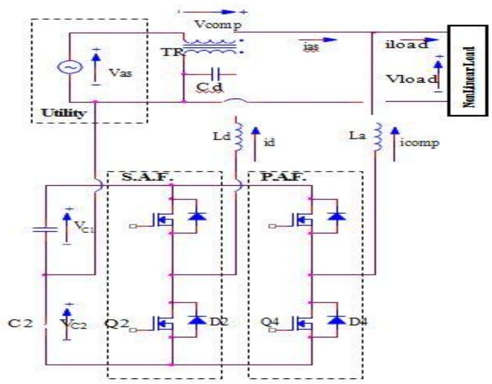

Fig.1.Proposed UPQC circuit diagram

The pair of the transistors Q3 and Q4 act as PAF of conventional UPQC and compensates for current harmonics and reactive power of the non-linear load. Using coupling inductor, La makes it possible to charge the capacitors C1 and C2 like a boost converter and it also smooth the compensation current icomp(t). Fig. 2 shows a general power circuit topology for the single-phase UPQC. It consists of two H-bridge back to back inverters. One of the inverters operates as a normal series active filter and compensates for the voltage supply voltage quality and the next one operates as a shunt active filter for non-linear load harmonics and/or reactive power. Comparison of Fig. 1 and Fig. 2 shows that the switches number of Fig. 1 is half of the power circuit of Fig. 2. Also, the split capacitors in the DC side of Fig.1, provides a neutral point which might be used as zero potential for the control circuit.

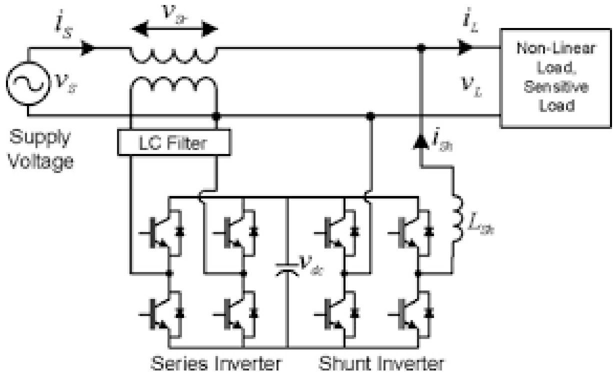

Fig. 2. General power circuit topology of single-phase UPQC

III. DETERMINATION OF COMPENSATION REFERENCE VOLTAGE AND CURRENT

Fig. 3 shows the block diagram of proposed control strategy for determination of compensation reference voltage of SAF $v_{Comp,Ref}$ (t), and reference compensation current of PAF $i_{Comp,Ref}$ (t).

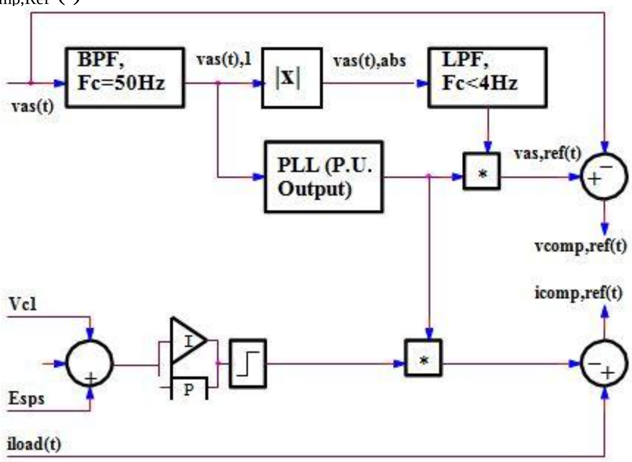

Fig. 3. The Reference compensation voltage and current generation control block diagram

Utility voltage vs (t) that may be harmonic polluted and it could have voltage sag or swell passes through a band pass filter (BPF) for filtering out the undesired harmonics and the determination of fundamental frequency vs1 (t). An absolute control block, a low pass filter (LPF) with a big time constant and a correction factor block Kc, generates the reference voltage magnitude of vs1(t) as vs1m(t). A phase lock loop (PLL) circuit uses vs1(t) for generation of a unit sinusoidal waveform with the same frequency and phase angle of vs1(t). The output of PLL multiplies to vs1m(t) for generation of reference voltage waveform in load side. By subtraction of vs(t) from the reference voltage waveform of load side, it is possible to generate the reference compensation voltage waveform of SAF, vComp,Ref(t). The reference compensation current of PAF should be in such a way that it compensates for current harmonics and reactive power of load, and it regulates the voltage of DC side capacitors. The output of PLL is a unity magnitude sinusoidal waveform that is in-phase with load-side voltage. By choosing the suitable magnitude for mentioning current, it could be used as the reference current in source side that is shown in Fig. 2 by iS,Ref(t). On the other hand, the magnitude of iS,Ref(t) determines the sum of the absorbed active power of UPQC and load from the utility. The absorbed active power by UPQC would increase the voltage of DC side capacitors and vice versa. In this way, it is possible using DC side capacitor voltage for regulating the magnitude of iS,Ref(t). If the voltages of DC side capacitors decrease from a pre-specified value, the magnitude of iS,Ref(t) should increase and vice versa. A “DC side voltage regulator” circuit that compares the sum of the voltages of VC1 and VC2 with a pre-specified DC voltage Vsp, is used for regulating the magnitude of iS,Ref(t) where VC1 and VC2 stand for the average voltage of C1 and C2, espectively. API controller regulates the magnitude of iS,Ref(t). Subtraction of iS (t) from the load side current iS,Ref(t) can be used for generation of reference compensation current of PAF, iComp,Ref(t).

IV. GENERATION OF SWITCHING STRATEGY OF PAF AND SAF

The well-known Hysteresis band control method is used for generation of switching pattern of PAF. Fig. 4 shows the reference compensation current of PAF iComp,Ref (t), the current through La, iComp(t) and upper and lower bands around iComp,Ref(t). The bandwidth is considered to be 2ε in this figure. Decreasing the band width results in better quality of iComp(t) in tracking of iComp,Ref (t) but it increases the switching frequency and vice versa. This figure shows the switching pattern of pair switches S3 and S4 where S3 comprises of Q3 and D3 and S4 comprises of Q4 and D4, respectively. For proper operation of PAF the following conditions should be satisfied:

$$v_{C1}(t) > V_m \quad (1)$$

$$v_{C2}(t) > V_m \quad (2)$$

Where vC1(t) and vC2(t) are voltage across capacitors C1 and C2, respectively. The Vm stands for the maximum expected voltage of the utility. Considering above equations show that switching ON the S3 results in increasing of iComp(t) while switching ON the S4 results in decreasing of iComp(t). Table 1 shows the conducting semiconductors of each switch considering the polarity of iComp(t) and its derivative.

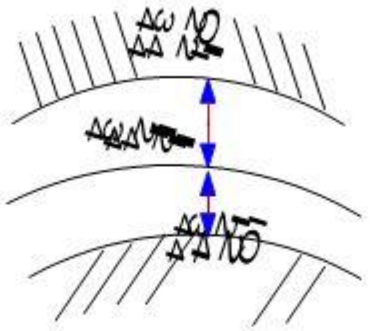

Fig. 4. Hysteresis band control of PAF switches of and its derivative

$i_{Comp}(t)>0$		$i_{Comp}(t)<0$	
$di_{Comp}(t)/dt>0$	$di_{Comp}(t)/dt<0$	$di_{Comp}(t)/dt>0$	$di_{Comp}(t)/dt<0$
Q_3	D_4	D_3	Q_4

Considering Fig. 1 shows that positive values of id(t) results in charg of Cd and thereby vComp(t) increases. On the other hand, the negative value of the id(t) discharges the Cd and vComp(t) decreases. For suitable operation of SAF the following conditions should be satisfied:

$$v_{C1}(t) > V_{Cd,M} \quad (3)$$

$$v_{C2}(t) > V_{Cd,M} \quad (4)$$

Where, VCd,M stands for the maximum possible voltage value across Cd that could be obtained considering the maximum possible voltage magnitude of vComp(t) and the turns ratio of coupling transformer TR, easily. Turning ON of Q1 results in a positive value of id(t), so vComp(t) increases. Q1 turns OFF when vComp(t) reaches the upper limit, and a commutation occurs between Q1 and D2. D2 conducts until the current of Ld reaches zero and Q2 turn ON in zero voltage switching (ZVS) condition. Q2 conducts until the vComp(t) reaches to lower limit of the hysteresis band where a commutation occurs between Q2 and D1. By conducting of D1, id(t) increases to zero where Q1 turns ON in ZVS condition. Indeed, the proposed switching strategy for SAF is an approximate hysteresis band control, and it makes it possible tracking of vComp,Ref(t) by vComp(t) in addition to ZVS of Q1 and Q2 during their turning ON.

V. SIMULATION RESULTS

The following values are selected for simulation of the proposed circuit. Switching frequency is considered about 25 [KHz], Vs =220 [V], C1=C2=10000 [μF], La=Ld=100 [mH], ESPS=700 [V] and a non-linear load with an active power consumption about 400 [W]. The optimum values of the PI controller obtained from try and error and experimental results. Grid, load, and compensated voltages have been illustrated in Fig. 5. In this figure, normal case occurs between 4.7<t<4.75, voltage sag condition is between 4.75 < t < 4.8 where the utility side voltage has decreased to 170 (v), voltage swell happens between 4.8 < t < 4.87 that the utility side voltage has increased to 270 (v) and between 4.87 < t < 4.92 a 250 Hz harmonic with 30 (v) is added to the utility voltage.

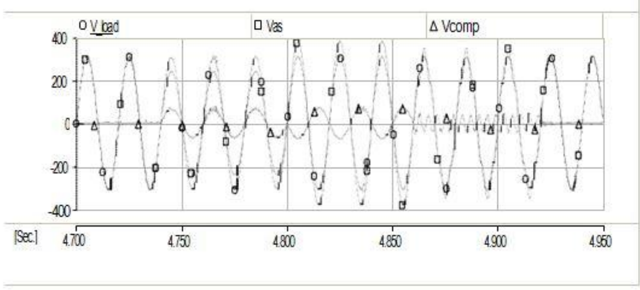

Fig.5. Utility, load and compensated voltages

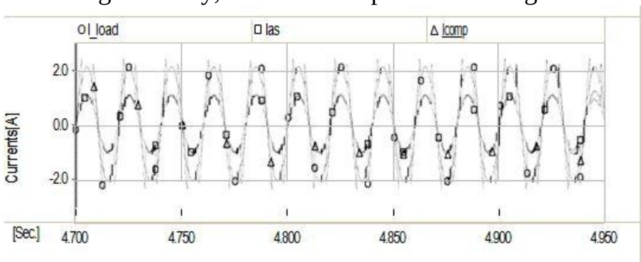

Fig 6 Utility, load and compensated currents

As it can be seen in Fig. 5, the UPQC has managed to compensate the difference between load and utility voltages with SAF function. Fig. 6 shows the grid and load currents that UPQC's PAF function has compensated their differences. In Table II, shows a comparison of Total Harmonic Distortion (THD) percentage between the utility voltage and currents without and with UPQC compensation.

TABLE II

COMPARING RESULTS

THD %			
Without Compensation		With Compensation	
$THD[i_{as}(t)]$	$THD[v_{load}(t)]$	$THD[i_{as}(t)]$	$THD[v_{load}(t)]$
28	14	17	10

VI. CONCLUSION

In this paper a single phase power circuit topology for UPQC that is used in single-phase utility with non-linear single-phase loads has been proposed. This UPQC can act as SAF and PAF with ZVS function. As it has been shown in simulation results the proposed UPQC can compensate for different power quality problems such as voltage sag, voltage swell, voltage harmonics, current harmonics and reactive power compensation successfully. The proposed UPQC uses only one single-phase full-bridge inverter instead of two single-phase full-bridge inverters that lead to its cost, weight, volume, protection circuits, power losses and control circuit complexity reduction. The analytical analysis presented and the simulation results show fast response with high power quality for proposed circuit.

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