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PERFORMANCE ANALYSIS OF MODIFIED SEPIC CONVERTER WITH LOW INPUT VOLTAGE

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Abstract: ***The paper presents performance analysis of modified SEPIC dc-dc converter with low input voltage and wide output voltage range. The operational analysis and the design is done for the 380W power output of the modified converter. The simulation results of modified SEPIC converter are obtained with PI controller for the output voltage. The results obtained with the modified converter are compared with the basic SEPIC converter topology for the rise time, peak time, settling time and steady state error of the output response for open loop. Voltage tracking curve is also shown for wide output voltage range.***
Keywords: Dc-dc Power Conversion, SEPIC Converter.

I. INTRODUCTION

Dc-dc converters are widely used in regulated switched mode dc power supplies and in dc motor drive applications. The input to these converters is often an unregulated dc voltage, which is obtained by rectifying the line voltage and it will therefore fluctuate due to variations of the line voltages. Switched mode dc-dc converters are used to convert this unregulated dc input into a controlled dc output at a desired voltage level. The recent growth of battery powered applications and low voltage storage elements are increasing the demand of efficient step-up dc–dc converters. Typical applications are in adjustable speed drives, switch-mode power supplies, uninterrupted power supplies, and utility interface with nonconventional energy sources, battery energy storage systems, battery charging for electric vehicles, and power supplies for telecommunication systems etc.. These applications demand high step-up static gain, high efficiency and reduced weight, volume and cost. The step-up stage normally is the critical point for the design of high efficiency converters due to the operation with high input current and high output voltage [1]. The boost converter topology is highly effective in these applications but at low line voltage in boost converter, the switching losses are high because the input current has the maximum value and the highest step-up conversion is required. The inductor has to be oversized for the large current at low line input. As a result, a boost converter designed for universal-input applications is heavily oversized compared to a converter designed for a narrow range of input ac line voltage [2]. However, recently new non-isolated dc–dc converter topologies with basic boost are proposed, showing that it is possible to obtain high static gain, low voltage stress and low losses, improving the performance with respect to the classical topologies. Some single stage high power factor rectifiers are presented in [3-6]. A new alternative for the implementation of high step-up structures is proposed in this paper with the use of the voltage multiplier cells integrated with basic non-isolated dc–dc converters. The uses of the voltage multiplier in the basic dc–dc converters add new operation characteristics, becoming the resultant structure well suited to implement high-static gain step-up converters [7]. The use of high static gain and low-switch voltage topologies can improve the efficiency operating with low input voltage, as presented in [8-10].

II. OVERVIEW OF CIRCUIT AND OPERATION

The modified SEPIC converter is accomplished by including of the diode DM and the capacitor CM in basic SEPIC converter. The voltage multiplier technique is used to increase the static gain of single-phase boost dc–dc converters. An adaptation of the voltage multiplier technique with the SEPIC converter is presented in fig.1. Many operational characteristics of the basic SEPIC converter are changed with the proposed modification.

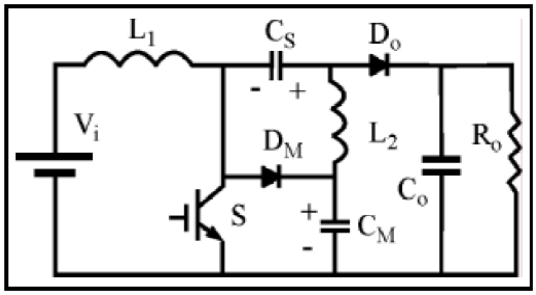


Fig. 1: Circuit of the Modified SEPIC

The capacitor C_M is charged with the output voltage of the basic boost converter. Therefore, the voltage applied to the inductor L_2 during the conduction of the power switch S is higher than that in the basic sepic converter, thereby increasing the static gain. The principle of operation of the modified SEPIC converter presents the following two operation stages. First stage (switch is off)
Second stage (switch is on)
The principle of operation of first stage is shown in the fig. 2.

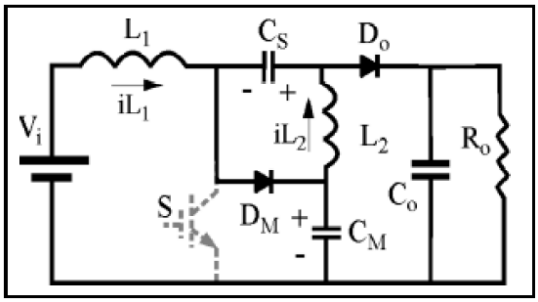


Fig 2 First stage (Switch is off)

The first stage of operation varies from time t_0 to t_1. At the instant t_0, the switch S is turned-off and the energy stored

in the input inductor L_1 is transferred to the output through the capacitor C_S and output diode D_O, and also to the capacitor C_M through the diode D_M. Therefore, the switch voltage is equal to the capacitor C_M voltage. The energy stored in the inductor L_2 is transferred to the output through the diode D_O.

The principle of operation of second stage is shown in the fig.3.

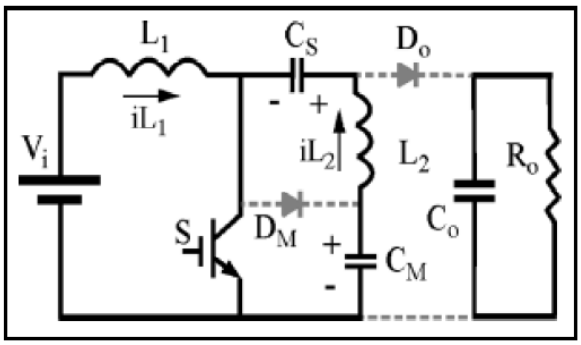


Fig. 3: Second Stage (Switch is On)

The second stage operation varies from time t_1 to t_2. At the instant t_1, the switch S is turned-on and the diodes D_M and D_o are blocked, and the inductors L_1 and L_2 store energy. The input voltage is applied to the input inductor L_1 and the voltage $V_{CS} - V_{CM}$ is applied to the inductor L_2. The voltage V_{CM} is higher than the voltage V_{CS}.

The operating waveforms of modified SEPIC converter are presented in fig. 4.

The voltage in all diodes and the power switch is equal to the capacitor C_M voltage. The output voltage is equal to the sum of the voltages across capacitors C_S and C_M respectively. The average L_1 inductor current is equal to the input current and the average L_2 inductor current is equal to the output current [11].

III. ANALYSIS AND DESIGN OF THE MODIFIED SEPIC

Static gain is a measure of the ability of a circuit to increase the power from the input to the output. It is usually defined as the ratio of the output to the input of a system. At the steady state for the inductor L_1, the relation presented in (1) occurs:

$$V_1(t_{on} + t_{off}) = V_{CM} t_{off} \quad 1$$

$$V_1 D = (V_{CM} - V_1)(1 - D) \quad 2$$

Therefore, the Cm capacitor voltage is defined by (3), which is the same equation of the classical boost static gain given by

$$\frac{V_{CM}}{V_i} = \frac{1}{1-D} \quad 3$$

During the period where the power switch is turned-off (t_{off}), the diodes D_M and D_0 are in conduction state, and the following relation can be defined:

$$V_o = V_{CS} + V_{CM} \quad 4$$

$$V_{CM} = V_O - V_{CM} \quad 5$$

The L_2 average voltage is zero at the steady state, and the following relations can be considered.

$$(v_{cm} - V_{CS}) t_{on} = (V_o - V_{CM}) t_{on} \quad 6$$

$$(v_{cm} - V_{CS}) D = (V_o - V_{CM})(1 - D) \quad 7$$

From equations (3), (5) and (6) the static gain of the proposed converter is obtained and presented in (8)

$$\frac{V_0}{V_i} = \frac{1+D}{1-D} \quad 8$$

The voltage of the series capacitor $V_{CS}$is defined by substituting (3) and (8) in (7), resulting the following equation.

$$\frac{V_{CS}}{V_i} = \frac{D}{1-D} \quad 9$$

For a basic SEPIC converter the static gain is given by as follows which is equal to the same as the equation (9) because the output Where, f is the switching frequency. voltage is equal to the capacitor C_S voltage. Thus the static gain of the basic SEPIC converter is given by,

$$\frac{V_o}{V_i} = \frac{D}{1-D} \quad 10$$

The operation with a higher static gain results in an improvement in the operation with the lower input voltage.

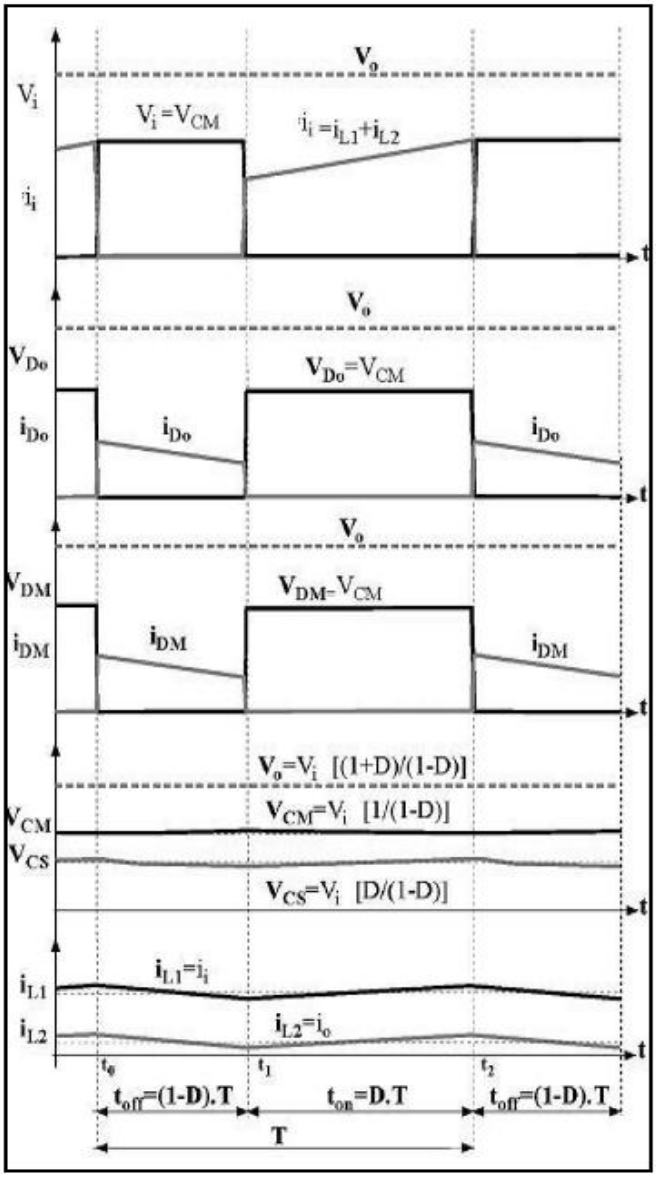


Fig 4: Steady State operation Waveforms

A. Input current ripple and L_1-L_2 Inductances

As the basic sepic, boost and the modified sepic converters present the same input stage, the equation for the determination of the input current ripple is the same for all converters. the input current ripple (Δi_{L1}) during the conduction of the power switch is defined by the following equation.

$$\Delta i_{L1} = \frac{V_i D}{f L_1} \quad 11$$

Where f is the switching frequency.

The input current ripple Δi_{L1} considered is 18% of the peak input current (i_{inpk}). Therefore, the input current ripple is calculated as follows:

$$\Delta i_{L1} = i_{inpk} X 0.18 = 6.5 X 0.18 = 1.17A$$

The input inductance is calculated from the equation (12). The input inductance value utilized in the simulation is equal to L_1 = 1mH. As the average input current is higher than the average output current for a step-up converter, the L_2 inductor volume is lower than the L_1 inductor volume.

The L_2 inductance utilized in the simulation is half of the L_1 inductance. The L_2 inductance value utilized in the simulation is half of the L_1inductance i.e. L_2= 500µH.

B. Series Capacitor Cs and multiplier Capacitor Cm

During the power switch turn on period, the current in the Cs and Cm capcitances is equal to the L2 inductor current. the capacitor charge variation ΔQ is calculated as

$$\Delta Q = i_{L2} DT \text{v} \quad 13$$

The high frequency capacitor voltage ripple ΔV_ccan be defined by (14), as a function of the capacitor charge variation

$$\Delta V_C = \frac{i_{L2} DT}{C} \quad 14$$

Therefore, the Cs and CM capacitances can be defined as follows.

$$C = \frac{i_{L2} D}{f \Delta V_C} \quad 15$$

Where f is the switching frequcny and C=Cs=Cm.

for an inpurt voltage equal to Vi=115V and a maximum capacitor voltage ripple equal to 7% of the output voltage $\Delta V_c = 24.15V$), and the maximum inductor current L2 is assumed to 1.5A. the capacitors Cs and CM can be determined from equation (15).

$$C = 647nF$$

The capacitors utilized in the analysis of the proposed converter are,

C=CS=CM=660nF.

C. Output capacitor C_0

The output filter capacitance is defined by a function of the output power Po the supply i.e. grid frequency fG and the low frequency output voltage ripple ΔV_0. the output voltage ripple is considered equal to 1% of the output voltage in calculation. The output capacitance is calculated as given bellow:

$$C_0 = \frac{P_0}{2\pi f_G X 2 V_0 \Delta V_0} \quad 16$$

the output voltage is calculated from equation 8

V0=345V

Considering an output voltage ripple equal to 1% of the output voltage for the output power 380W, the output capacitor value is calculated from equation (16)

$$C_0 = 500\mu F$$

IV. SIMULATION RESULTS

The designed parameters of the modified SEPIC system is given in table1 the closed loop simulink model for the modified SEPIC converter is shown in fig. 5 The single phase 115V, 50Hz ac voltage is the input of the SEPIC. The input voltage waveform is shown in fig. 6. The input ac current is in phase with the input voltage waveform having almost unity power factor as shown in fig. 7. The low order harmonics are also absent in the input current, i.e., less current harmonics are injected into the utility. Fig. 8 and fig. 9, are the rectified input voltage and current waveforms respectively. Open loop output voltage waveforms of Basic SEPIC and Modified SEPIC are shown in fig. 10 and fig. 11, respectively. Different open loop parameters of the Basic and Modified SEPIC are given Table 2. Fig. 12, shows the output voltage stabilization at 345V, 500V and 600V step voltage references at time t=0, t=0.55 and t=0.8s respectively.

Table 1: Parameters of the Modified SEPIC.

Model parameters	VALUE
Input voltage v1	115V
output voltage Vo	345V
inductor L1	1mH
Inductor L2	$500\mu F$
Series Capacitor Cm	660nF
Multiplier Capacitor Cm	660nF
Output Capacitor C0	$500\mu F$
Switching frequency Fs	48kHz
Grid frequency F_G	50Hz

Table 2: Comparison of Parameters of the Basic and modified SEPIC

Parameters	Basic SEPIC	Modified SEPIC
Input voltage	115V	115V
Output Voltage	366V	430V
Output Current	0.46A	0.54A
Rise Time (Sec)	0.186	0.056
Settling Time(Sec)	0.42	0.22
Steady State Error(%)	2.19	1.16

During the power switch turn-on period, the current in the C_S and C_M capacitances is equal to the L_2 inductor current. The capacitor charge variation ΔQ is calculated as The high-frequency capacitor voltage ripple ΔV_C can be defined by (14), as a function of the capacitor charge variation Therefore, the and capacitances can be defined as follows.

Output Capacitor C

The output filter capacitance is defined by a function of the output power P_o, the supply i.e. grid frequency f_G, and

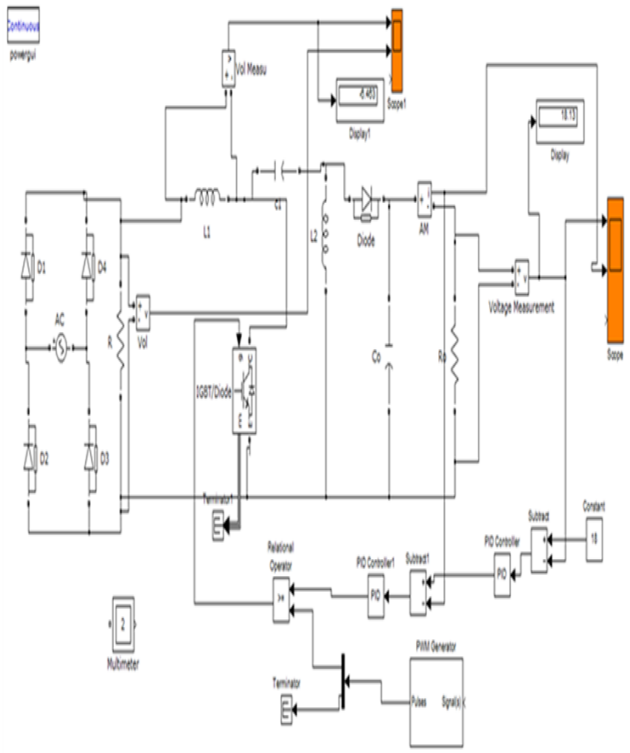
the low- frequency output voltage ripple ΔV_o. The output voltage ripple is considered equal to 1% of the output voltage in calculation. The output capacitance is calculated as given below: The output voltage is calculated from equation (8). Considering an output voltage ripple equal to 1% of the output voltage for the output power 380W, the output capacitor value is calculated from equation (16). C_o = 500 µF

V. SIMULATION RESULTS

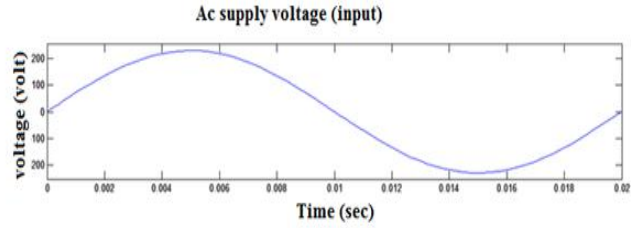
During the simulation time the input voltage was varied from 40V ac - 500V ac, Resulting multiple output ranges from 18V DC – 470V DC .In others words we can select a constant DC output voltage of 18V (tolerance band of ±10% to ±15%) while input voltage is varies from 40V ac -500V ac. During simulation, switching frequency has been set to 12kHz.The PI Controller has been used in the feedback loop and the value of Kp= 0.0455 and Ki= 0.95.

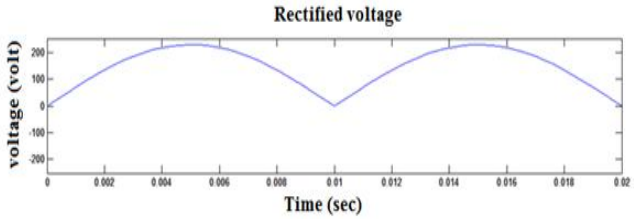
VI. CONCLUSIONS

A modified SEPIC converter is analyzed and designed. The converter model is simulated on Simulink for open loop as well as closed loop. The PI controller is used to control the output voltage of the modified SEPIC which gives the controlled variation of output voltage from 250V to 650V with input voltage 115V. Although the proposed structure presents a higher circuit complexity than the basic converter but we obtain the higher static gain for the operation with the low input voltage, low switch voltage operation and controlled output voltage variation between 250V and 650V with input voltage 115V with duty ratio 50% with 25kHz switching frequency.

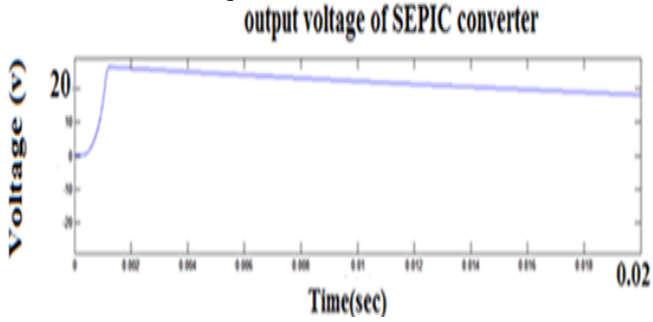


Simulink Model of SEPIC converter

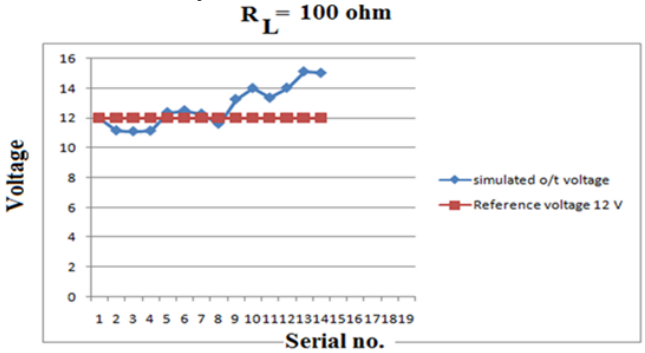




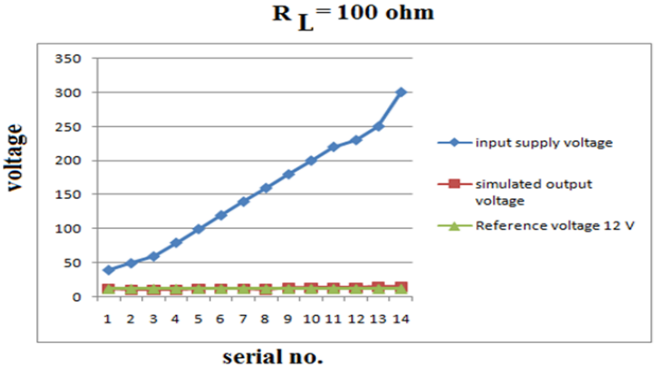
Input supply given to the SEPIC (upper and rectified voltage obtained from the rectifier section (lower) of the SEPIC converter i.e. at the input section of SEPIC



Output voltage obtained from SEPIC converter when input supply was set to 230 V ac and controlle input at 18.
The above plot showing that, the output voltage attend the value that was set by controller.



Simulated result versus Reference voltage Plot



Plots Among supply, Reference and Simulated voltages

Table 6.1: output response of SEPIC converter for resistive load for IGBT switch.

Vin	V_{out} For V_{ref}=12V R_l=100Ω	V_{out} For V_{ref}=12V R_l=120Ω
40	12	10.63
50	11.16	10.52
60	11.1	11.84
80	11.14	11.86
100	12.38	12.97
120	12.51	13.33
140	12.28	13.08
160	11.61	15.21
180	13.26	14.13
200	14.01	15.23
220	13.36	14.23
230	14.03	14.95
250	15.13	13.88
300	15.03	13.56

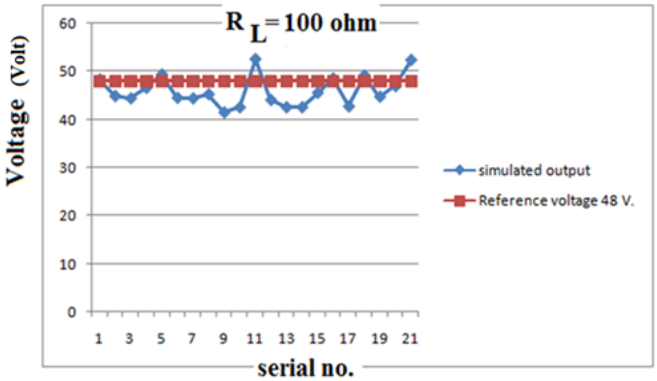
The data given in tabular form as in Table no. (6.1).It showing response for two different set of values, the first one is Vref=12V and 100Ω load and second set is Vref = 12V and 120Ω load. The graph ploting against Reference value, actual output corresponding to this reference value while input was varied from 40V ac to 300V ac during this period. It is clear from graph in figure (6.7) that actual output response of the converter is almost equal to the reference value while there is wide variation in input side and in the load. The data in tabular form as in Table no. (6.3) representing response for two different set of values, the first one is Vref=48V and 100Ω load and second set is Vref = 80V and 100Ω load. The graph has been plotted against Reference value, actual output corresponding to this reference value while input has been varied from 40V ac to 500V ac during this period. It is clear from graph in figure (6.9) that actual output response of the converter is almost equal to the reference value while there is wide variation in input side and in the load.

Table 6.2: Simulation Result of close-loop SEPIC for IGBT switch when load was resistive.

SL. No.	V_{in} Ac supply(volt)	$V_{out}(V)$ forV_{ref}=18V	V_{out}(V) for V_{ref}=120V
1	40	17.13	114.4
2	60	18.71	129.8
3	80	19.96	121.0
4	100	15.81	114.1
5	120	14.48	110.1
6	140	14.58	108.8
7	160	16.92	107.6
8	180	16.15	108.7
9	200	18.13	110.1
10	230	17.48	107.6
11	250	19.15	107.5
12	270	20.81	117.8
13	290	18.40	116.9
14	320	19.09	115.7
15	340	21.85	115.0
16	400	21.08	110.0
17	430	22.77	109.5
18	450	23.91	106.3
19	500	21.51	118.8

Table 6.3-Simulation Result of SEPIC for IGBT switch.

V_{in}(V)	V_{out}(V) For V_{ref}=48vR_l=100Ω	V_{out} (V) For V_{ref}=80vR_l=100Ω
40	48.28	90.7
60	44.85	81.76
80	44.38	76.14
100	46.53	75.44
120	49.32	74.25
140	44.48	77.46
160	44.37	76.94
180	45.22	73.6
200	41.47	80.84
230	42.52	85.47
250	52.47	72.72
270	44.04	78.18
290	42.54	72.67
300	42.54	83.74
320	45.52	86.09
340	48.49	92.09
350	42.72	103.3
400	49.11	109.3
430	44.71	71.41
450	46.88	74.83
500	52.29	72.28



Reference voltage (48V) versus Simulated Result plot

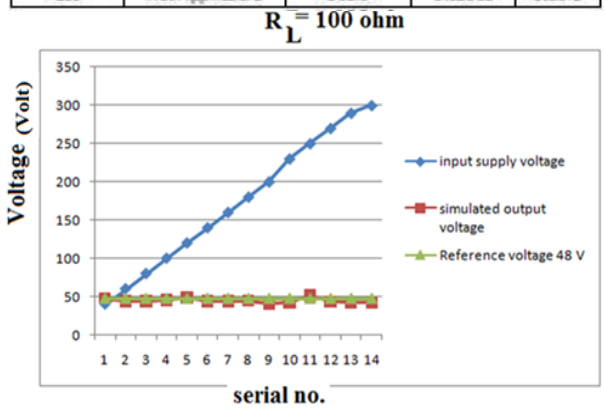
TABLE NO. (6.5)- SIMULATION RESULT OF SEPIC.

INPUT-OUTPUT RESPONSE TABLE FOR OPEN-LOOP SEPIC CONVERTER FOR IGBT SWITCH

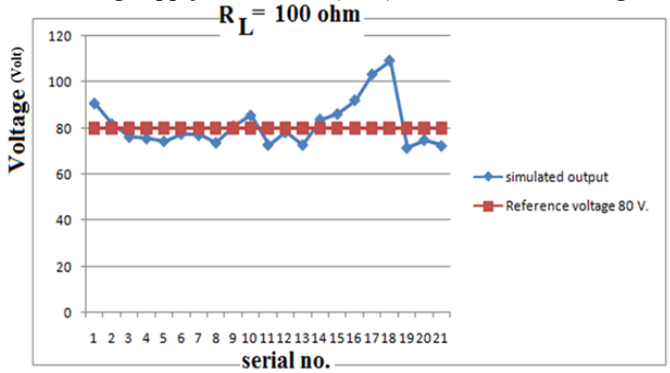
RESISTIVE & R-L LOAD

Input supply ac voltage(V)	Reference DC Voltage(V)	output DC voltage(V) of sepic	output current(A)	Open loop stability
R=100Ω				
230	Not Applicable	654.2	6.542	Stable
150	Not Applicable	425.4	4.254	Stable
100	Not Applicable	282.2	2.822	Stable
R=400Ω				

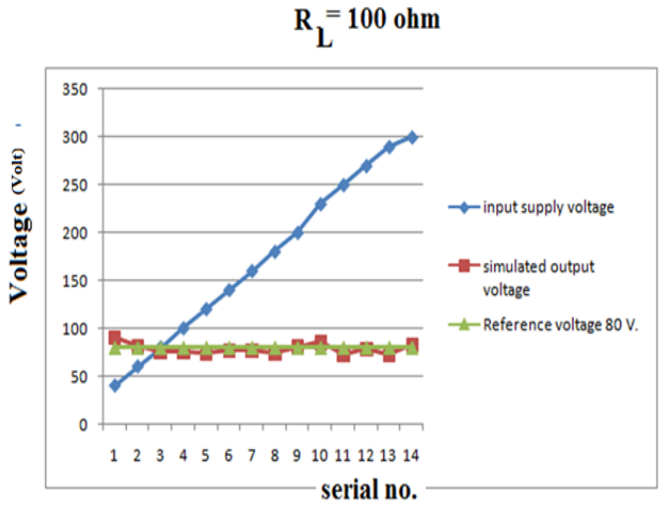
230	Not Applicable	799.8	1.999	Stable
150	Not Applicable	520.1	1.3	Stable
100	Not Applicable	345.2	0.863	Stable
R=10KΩ				
230	Not Applicable	853.8	0.08538	Stable
150	Not Applicable	555.2	0.05552	Stable
100	Not Applicable	368.6	0.03686	Stable
R-L LOAD				
R=100Ω, L=700μH				
230	Not Applicable	707.6	6.778	Stable
150	Not Applicable	460.1	4.408	Stable
100	Not Applicable	305.5	2.426	Stable
R=400Ω, L=700μH				
230	Not Applicable	802.3	2.011	Stable
150	Not Applicable	521.7	1.308	Stable
100	Not Applicable	346.3	0.8683	Stable
R=10KΩ, L=700μH				
230	Not Applicable	853.9	0.08538	Stable
150	Not Applicable	555.2	0.05552	Stable
100	Not Applicable	368.6	0.03685	Stable



Plot among supply, Reference (48V) and Simulated voltages



Reference Voltage (80V) versus Simulated Result Plot



Plot among supply, reference (80V) and Simulated voltages

REFERENCES

[1] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, D. P. Kothari,"A review of single-phase improved power quality AC–DC converters", IEEE Trans. Ind. Electron., Vol. 50, No. 5, pp. 962–981, 2003. 2nd ed. Norwell, MA: Kluwer, 2001.

[2] J. Chen, D. Maksimovic, R. W. Erickson,"Analysis and design of a low-stress buck-boost converter in universal- input PFC applications", IEEE Trans. Power Electron., Vol. 21, No. 2, pp. 320–329, 2006.

[3] J. Qian, F. C. Lee,"Ahigh efficient single stage single switch high power factor ac/dc converter with universal input", IEEE Trans. Power Electron., Vol. 13, No. 4, pp. 699–705, 1998.

[4] C. Qiao, K. M. Smedley, "A topology survey of single-stage power factor corrector with a boost type input current-shaper", IEEE Trans. Power Electron., Vol. 16, No. 3, pp. 360–368, 2001.

[5] M. H. L. Chow, Y. S. Lee, C. K. Tse,"Single-stage single- switch isolated PFC regulator with unity power factor, fast transient response, and low-voltage stress," IEEE Trans. Power Electron., Vol. 15, No. 1, pp. 156–163, 2000.

[6] J. L. Lin, W. K. Yao, S. P. Yang,"Analysis and design for a novel single-stage high power factor correction diagonal half-bridge forward ac-dc converter", IEEE Trans. Power Electron., Vol. 53, No. 10, pp. 2274–2286, 2006.

[7] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. R. Romaneli, R. Gules,"Voltage multiplier cells applied to non- isolated DC–DC converters",IEEE Trans. Power Electron., Vol. 23, No. 2, pp. 871–887, 2008.

[8] Q. Zhao, F. C. Lee,"High-efficiency, high step-upDC–DC converters", IEEE Trans. Power Electron., Vol. 18, No. 1, pp. 65–73, 2003.

[9] R.J.Wai, R.Y. Duan,"High step-up converter with coupled- inductor", IEEE Trans. Power Electron., Vol. 20, No. 5, pp. 1025–1035, 2005.

[10] R.J. Wai, R.Y. Duan,"High-efficiency power

conversion for low power fuel cell generation system", IEEE Trans. Power Electron., Vol. 20, No. 4, pp. 847–856, 2005.

[11] P. F. de Melo, R. Gules, R. Romaneli, R. C. Annunziato,"A Modified SEPIC Converter for High-Power-Factor Rectifier and Universal Input Voltage Applications", IEEE

