

# DESIGN AND IMPLEMENTATION OF MULTI-PORT MEMORY

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**Abstract:** System-on-chip designs moving from logic dominant chips to memory dominant chips to be able to meet future application requirements. Embedded memory density and area on-chip is increasing day by day. Attain high-quality memory yield, an at-speed test technique such as built-in self test (BIST) must be implemented to test these embedded memories. Memory Built-in Self Test (MBIST) is the popular approach to test embedded memories. MBIST typically use the deterministic pattern such as MARCH check algorithm to test memories. In MARCH test algorithm, the patterns are generated according to specified predetermined values. The existing March algorithms consist of as many as four or seven operations for every March element. Therefore, it is essential to describe new test algorithms which fulfill the requirement of detecting new fault. BLC test having form of operations per part according to the today's rising need of embedded memory testing with improved fault using Verilog HDL as a prime language and used Modelsim as simulation tool.

**Keywords:** Xilinx, Memory Built-In Self Test (MBIST), Verilog, BIST

## I. INTRODUCTION

Multi-ported memory is largely used in up to date designs on FPGAs. The excessive requirement of BRAMs to implement multi-ported memory on FPGA would slab the procedure of BRAMs for other parts of a design. This issue becomes a serious concern especially for designs that require huge internal storage capacity. BRAM well-organized plan on increasing read port and write port. When compare with earlier works, the proposed multi-ported memory can reduce requirement on BRAMs with only minor frequency degradation. BIST controllers are capable of running the test algorithms in a pre-specified sequence during industrialized test. these controllers are modified and hardwired for a given memory architecture and a pre-defined set of algorithms, the area overhead is low and tests can be applied at speed. With rapid changes in technology, it is becoming extremely difficult to predict the defect types that could manifest during the manufacturing process. A chip or its later change stays long enough to be manufactured with different technology nodes. Under such circumstances, test algorithms that would work well for a certain technology for which the controller was designed may no longer work when manufactured using the next technology node. There is a rising requirement for a programmable BIST answer that would allow certain level of flexibility to change the test programs at run time. This would help analyzing the failing parts during production test, identifying of the defects that are escaping, re-designing the existing algorithms or introducing new algorithms, and use it to reduce the test escapes. Specifically, the following

summarizes some of the advantages of a programmable BIST controller:

a. Flexibility to create different data backgrounds, addressing schemes, and test algorithms. b. original test algorithms residential for newly recognized defects. This helps in improving the test quality, which is especially useful for military, medical, and automotive applications. c. Helping failure analysis thereby expediting the yield learning period of a fabrication process. d. improved managing of test time as dissimilar sets of algorithms can be applied at different phase of test, such as wafer sort, burn-in test, parametric, package, etc

Memories with more read/write ports can be extended technique that can attain efficient multiported memory designs. This technique would avoid the issue of congested routing and potentially enhance the overall performance of the multiported designs. The design can reduce the number of BRAMs while at the same time enhance the operating frequency.

## II. PROPOSED MBISR ARCHITECTURE

MBIST (Memory Built-In Self Test) is test circuitry made around memory to test it on-chip. The functional model of memory is shown in Figure

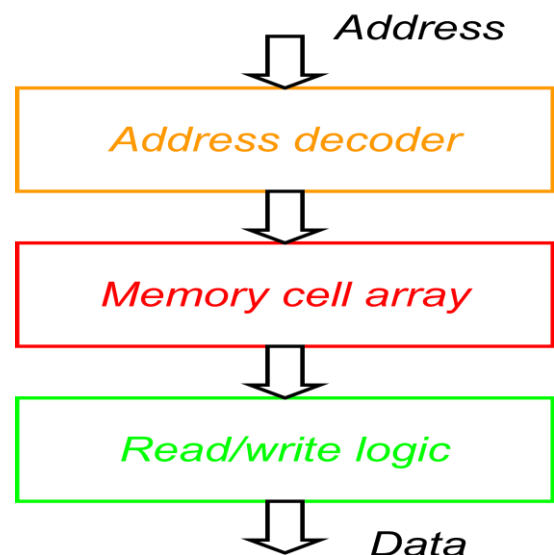


Fig 1. Functional Model Of Memory

From functional block shown in above Figure, there are basic 3 factors we need to test during test of memory and that are: Address, Data stored and Read-Write control signal.

So for tester, random Address, Data, Read-Write control signal are acts as test-vectors. BIST contain an internal finite-state machine (FSM) which gives test vectors to test memory during test mode, this also reduces external test

requirements. Test vectors randomly generate Address, data and Read/Write control. The Address, Data, Read/Write control together also is called test collar. These addresses, data, read/write control signal is given to the comparator and also to the input multiplexer. Through multiplexer we can choose the mode, either test mode or normal mode. During normal mode, memory acts as regular memory and during test mode, memory content is provided by test collar's test vectors to test it. In test mode, during read, the data from test collar given to comparator as well as to memory and output of memory again given to the comparator. Here comparator compares test collar's test vectors with output of memory. If memory is working properly, then no fault pulse will generate and it is declared as memory is defect free. But if fault pulse becomes high, then we need to repair memory to avoid defect. The operation of MBIST is shown in Figure.

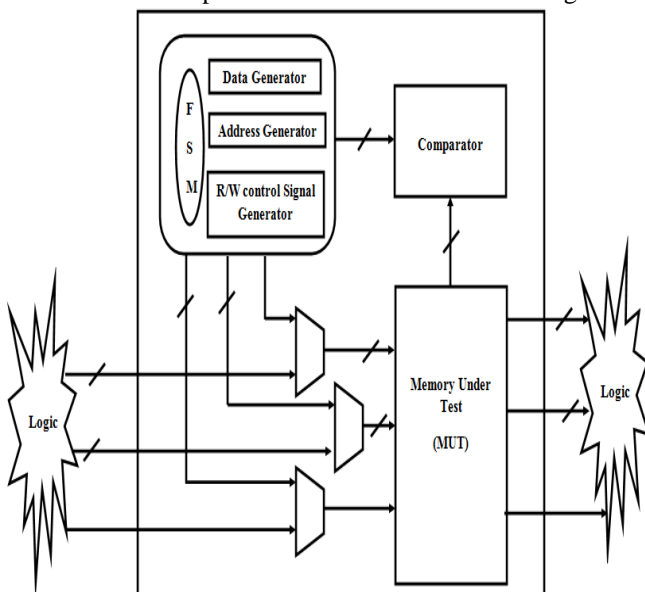


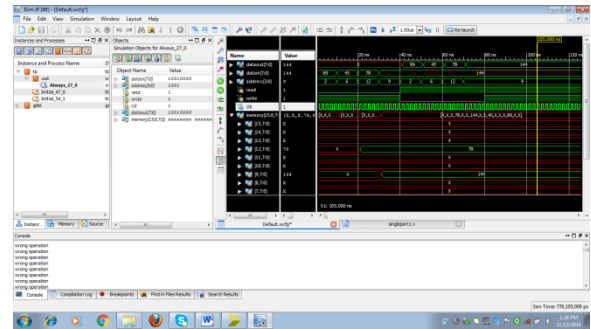
Figure 2. P-MBIST Mechanism

### III. PERFORMANCE ANALYSIS

In proposed project, single port RAM is used for testing. We can test different types of memories like single or dual port memory. Parallel Testing: Multiple memories can be tested simultaneously. This facility decreases test performance time but may increases power dissipation. This is one of the most important challenges for test engineers. During normal mode, test controller is in idle mode. So power dissipation caused due to test controller during normal mode can be avoided in future to design power efficient tester for memory. So here we can see result varication of various port and how BIST become more advanced and powerful in the form of testing.

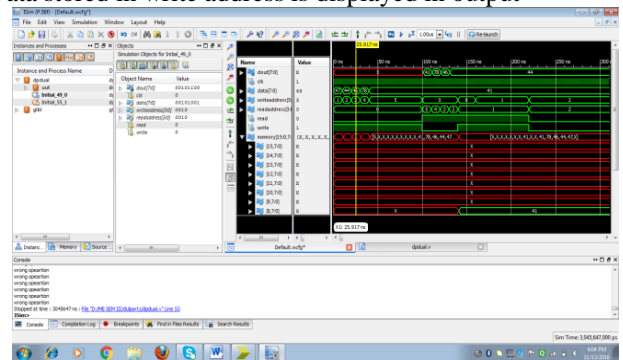
#### Single Port

When data – 7 is stored in address – 4, read signal is 0 and write signal is 1. Only write function is active that's why dout is 0 as no read operation is performed correct operation - Write low, read high and vice versa  
 Wrong operation -read/write both r either high or low



#### Dual port

2 address can be accessed - 1 for write and other for read  
 Wrong operation - Cannot read and write simultaneously from same address –  
 Data stored in write address is displayed in output



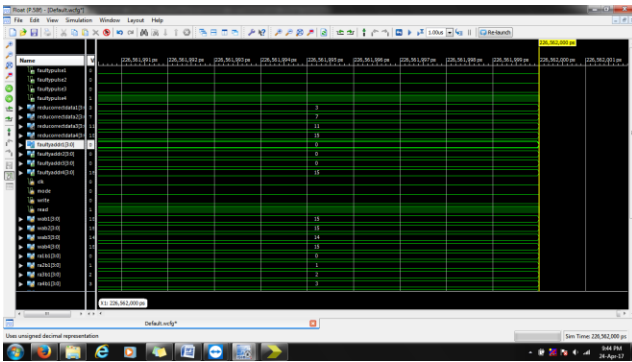
#### Multi Port

Multi Read and write can be done simultaneously  
 At a time, 2 outputs are displayed  
 Data stored in write address will be displayed in output  
 For write address 15 it keeps only that data port



#### Bist

It is uses at high speed testing for detect the faults in embedded memory .This only solution that allows atspeed testing for embedded memories  
 Write and read operation can be performed from same address  
 First data is stored in address and then it is read and shown in output  
 15 data is stored in write address4, it is first read and then displayed in output. Fault arises in address 4 that is why 15 is displayed in faulty address 4  
 Faulty pulse shows fault address



#### IV. CONCLUSION

Efficient BRAM-based multiported memory designs on FPGAs. The existing design methods require significant amounts of BRAMs to implement a memory module that supports multiple read and write ports. Occupying too many BRAMs for multiported memory could seriously restrict the usage of BRAMs for other parts of a design. This paper proposes techniques that can attain efficient multiported memory designs. This paper introduces a novel 2R1W/4R memory. By exploiting the 2R1W/4R as the building block, this paper proposes a hierarchical design of 4R1W memory that requires fewer BRAMs than the previous designs based on replication. XOR-based and LVT-based approaches, these designs can reduce BRAM usage for 4R2W memory designs with 8K-depth. For complex multi ported designs, the proposed BRAM-efficient approaches can achieve higher clock frequencies by alleviating the complex routing in an FPGA. For 4R3W memory with 8K-depth, the proposed design can save no. of BRAMs while at the same time enhance the operating frequency.

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