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PERFORMANCE ANALYSIS OF LOW POWER ALU USING NOVEL FULL ADDER AND PASS TRANSISTOR LOGIC BASED MULTIPLEXER

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Abstract: An optimized compensation strategy for two-stage CMOS OTA has been proposed for a high frequency OPAMP design. Here, the slew rate and bandwidth has been increased by employing thin and long transistors into the design at output stage and wide transistors in input stage. These two techniques are able to increase the gain up to a great extent by increasing the output resistance and input transconductance respectively. There is a slight increase in static power dissipation of proposed architecture, but, the overall advantage of increased slew rate and gain bandwidth product which is very important parameter of communication so it compensates for this limitation.

I. INTRODUCTION

The operational transconductance amplifier (OTA) is an amplifier whose differential input voltage produces an output current. Thus, it is a voltage controlled current source (VCCS). There is usually an additional input for a current to control the amplifier's transconductance. The principle differences from standard op-amp are-

- Its output of a *current* contrasts to that of standard operational amplifier whose output is a *voltage*.
- It is usually used "open-loop"; without negative feedback in linear applications. This is possible because the magnitude of the resistance attached to its output controls its output voltage. Therefore a resistance can be chosen that keeps the output from going into saturation, even with high differential input voltages.

The schematic symbol of an Operational Transconductance Amplifier (OTA) is shown in Figure 1.1

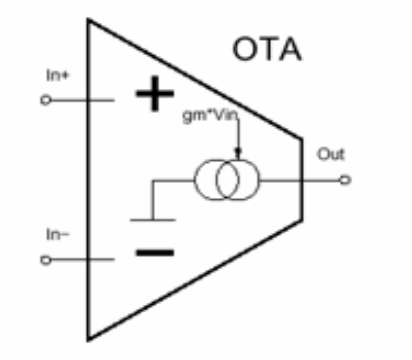

Figure 1.1 OTA Symbol

The OTA converts an input voltage to an output current relative to a transconductance gain parameter Gm=io/vi. Ideally the input and output resistances are infinite (Ri=Ro=∞) such that ii=iRo=0 and the output current is absorbed solely by the load. The conventional OTA is classified as a Class A amplifier and is capable of generating maximum output currents equal to the bias current applied. The equivalent circuit model indicates the transconductance amplifier generates an output current (io) proportional to an input voltage (vi) based on the transconductance gain Gm. The open circuit voltage gain of the conventional OTA model IN Figure 1.1 (B) is given by A=GmRo.

II. LOCAL COMMON MODE FEEDBACK

Industry is researching techniques to reduce power requirements, while increasing speed, to meet the demands of low (battery) powered wireless systems. These systems require amplifiers with low bias currents, capable of producing large dynamic currents. Application of Local Common Mode Feedback (LCMFB) techniques to the conventional OTA architecture produces an efficient class AB amplifier with enhanced gain-bandwidth and slew rate.

Characterization Parameters

Several common characterization methods are used to classify the functionality of OTA structures. These performance measurement techniques will be used to analyze designed structures via theoretical calculation, simulation, and experimentation throughout the documentation presented in the following chapters. A list of the measured characteristics is provided below.

1. Open Loop Gain (AOL)
2. Gain Bandwidth (GB)
3. Maximum Output Current (IOUTMAX)
4. Slew Rate (SR)
5. Static Power Dissipation (PSTATIC)

III. DESIGN AND IMPLEMENTATION OF PROPOSED OTA

3.1 Single Ended Proposed OTA

The conventional OTA (Figure 3.1(a)) uses a differential pair in conjunction with three current mirrors to convert an input voltage into an output current. A Differential Amplifier has been implemented using Microwind 3.0 with its simulation result shown in Figure 6.1.

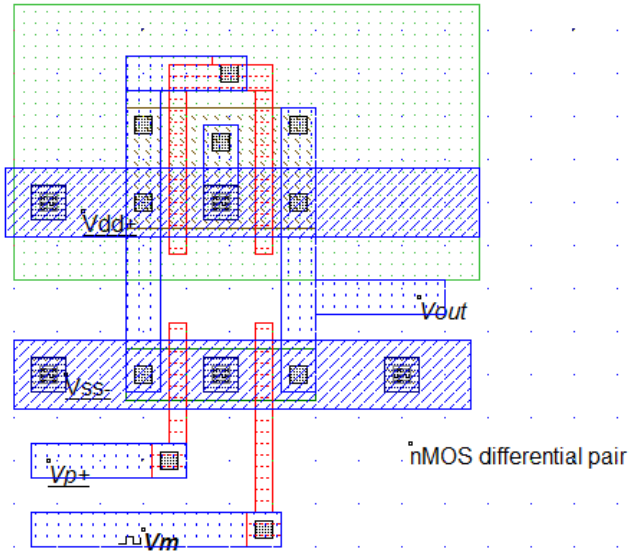

Fig. 5.1 Differential Amplifier MSK

An approach to show that current mirror circuit is more beneficial than conventional Diode load has been implemented using Microwind 3.0. The simulation of this circuit has been shown in next chapter in Figure 6.2.

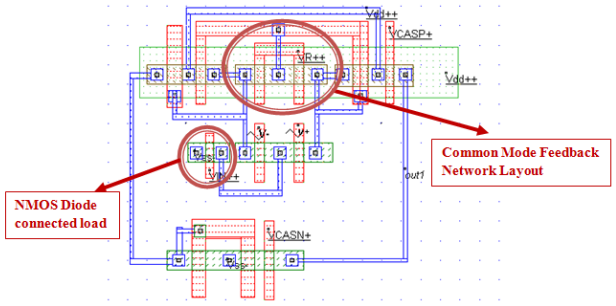

Figure 5.2 Proposed OTA Circuit MSK

The schematic layout of Conventional Operational Transconductance Amplifier (Figure 3.1(a)) in S-Edit Tanner EDA Tool and LTSPICE IV is shown in Figure 5.3 below.

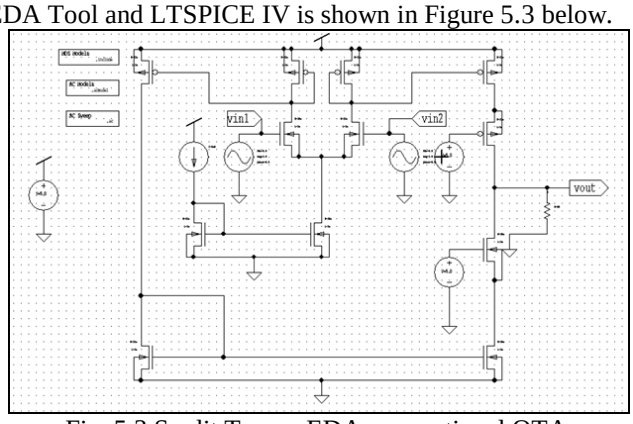

Fig. 5.3 S-edit Tanner EDA conventional OTA

Class AB operation characteristics allow the LCMFB structure to outperform the conventional structure with unity mirror gain. The analysis for the LCMFB OTA will therefore be based on a unity mirror gain factor (K=1, M3=M4=M5=M6, and M7=M8).

Figure 5.4 shows the LCMFB OTA structure with transistors MR1, MR2 implemented to function in the triode region and act as programmable resistors.

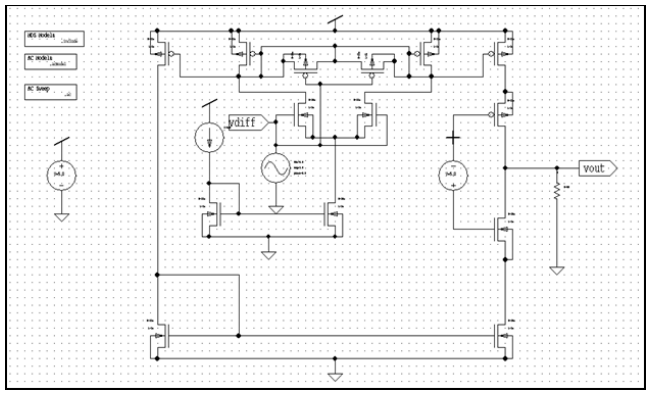

Figure 5.4Schematic layout of Proposed OTA Circuit in S-Edit TANNER EDA Tool

For quiescent (or common mode) operation, the drain currents of transistors M1-M10 have equal values ($ID_{1-10}=I_{bias/2}$) while the current i_R in transistors MR1, 2 is zero. The gate-source voltage of M3, 4 is the same as their drain-source voltage. For common mode signals, these transistors perform as low impedance (diode connected loads) with value:

$$R_L^{CM} = \frac{1}{gm_{3,4}} \qquad 5.1$$

Upon application of a differential signal, the signal current component ($i_d=i_r$) flows through transistors MR1, 2, and $i_{D1,2}$ are given by:

$$i_{D1,2}=I_D+ i_D =\frac{I_{Bias}}{2}+ i_r \qquad 5.2$$

where,

$$i_r=gm_{3,4}\frac{v_d}{2}\sqrt{1-\left(\frac{v_d/2}{V_{GS\,1,2}-V_{THN\,1,2}}\right)\left(\frac{v_d/2}{V_{GS\,1,2}-V_{THN\,1,2}}\right)} \qquad 5.3$$

and, v_d is the applied differential voltage. The drain currents in M3, 4 remains unchanged ($i_{D3,4}=I_{BIAS/2}$). The current i_r generates differential complementary voltage changes at nodes A and B while node C remains at a constant voltage.Signal voltages at nodes A and B are given by:

$$V_A = -V_B = i_r R_{MR1,2} \qquad 5.4$$

Where $R_{MR1,2}$ is the resistance generated by transistors MR1, MR2 and, based on the triode channel resistance equation, is given by:

$$R_{MR1,2}= \frac{1}{\beta_{MR1,2}(V_C-V_{THP}-V_R)} \qquad 5.5$$

Where V_R is the applied control voltage (Figure 5.1 (b)), $\beta_{MR1,2}=KP\,(W_{MR1,2}/L_{MR1,2})$, and V_C is the constant voltage at node C. This complementary swing at A, B generates large, non-complimentary, signal current in the shell (M5-10) of the OTA by creating large gate-source voltage differentials for common source transistors M5, M6, respectively. The schematic layout of Proposed OTA architecture in S-Edit Tanner EDA tool and LTSPICE IV has been shown below:

5.2 Design Parameters of Proposed OTA

The gain bandwidth of the conventional OTA is defined as:

$$GB = (Kgm_{1,2})/ 2C_L\pi \qquad 5.6$$

Rearranging equation (5.24), with unity mirror gain (K=1), the following equation can be used to calculate the

transconductance gain of the input differential pair.

$$2\pi C_L\, GB = gm_{1,2} \qquad 5.7$$

The transconductance of a MOS transistor can be calculated with the following expression:

$$gm = \sqrt{\frac{2KPW\, I_D}{L}} \qquad 5.8$$

Using this expression, the width of the NMOS differential input pair (M1, 2) can be determined based on a fixed bias current and predetermined length by rearranging Equation (5.26) for the following relation:

$$W_{1,2} = \{(gm_{1,2})^2\, L_{1,2}\}/2KP_N I_D \qquad 5.9$$

Utilizing a drain current of $I_D=I_{BIAS}/2=250\mu A$ (for $V_{DS,\,SAT}\approx 0.25V$), a length $L_1=3\lambda$ ($L_{1,2}>L_{MIN}=2\lambda$ for improved matching) and recognizing $KP_N=3KP_P$, Equations (5.25) and (5.27) can be used to size all transistors for the conventional OTA.Designed transistor sizes and corresponding $V_{DS,\,SAT}$voltages, based on theoretical calculations are listed below in Table 5.1.

Table 5.1 Conventional OTA Theoretical Design Transistor Sizes

TRANSISTORS	DIMENSIONS (W/L)	$V_{DS,\,Sat}$ (V)
M1=M2	4.122/0.18 µm	0.25
M3	1.912/0.18 µm	0.28
M4	7.21/0.18 µm	0.28
M5	7.7/0.18 µm	0.28
M6=M7=M8	5.18/0.18 µm	0.23
M9=M10, (L_{MIN})	1.098/0.18 µm	0.24

Cascoding output transistors (M9, M10) do not require matching design and were designed with minimum length for speed. Their widths were reduced by a factor 2 to reduce area.

The SE-LCMFB OTA is designed for comparison with the conventional structure. For an equivalent comparison, the SE-LCMFB structure is designed with core transistor sizes identical to those of the conventional OTA listed in Table 5.1. The core of the SE-LCMFB structure is therefore identical to the conventional structure and the only design required is the sizing of triode resistance transistors MR1, MR2.

The resistance formed by MR1, 2 (RMR1, 2) can be used to trade slew rate and gain bandwidth enhancement with phase margin for the class AB SE-LCMFB OTA. The high frequency pole at nodes A/B, maximum output current, and open loop gain are all functions of $R_{MR1,\,2}$. $R_{MR1,\,2}$ is programmable, is determined by the control voltage V_R, and is given by:

$$R_{MR1,\,2}=\frac{1}{(V_C-V_R-V_{THP})\beta_{MR1,2}} \qquad 5.10$$

Where, V_R is the control voltage applied at the gate of MR1, 2, V_C is the constant voltage at node C, and $\boldsymbol{\beta_{MR1,2}=KP_P(W_{MR}/L_{MR})}$. For design of MR1, 2, a range of $\boldsymbol{\Delta R_{MR1,\,2}}$can be determined based on a desired range of phase margin ΔPM. Simplifying for the position of the high frequency pole (phase margin) as a function of the resistance R_{MR} ***(assuming $r_{o1}\approx r_{o2}\approx r_{o3}\approx r_{o4}$)*** the following expression is obtained:

$$f_{pA,\,B}=\frac{1}{2\pi R_{MR1,2}C_{gs5,6}} \qquad 5.11$$

This relationship indicates a decrease in $\boldsymbol{f_{pA,\,B}}$and consequently, a decrease in phase margin, as $\boldsymbol{R_{MR1,\,2}}$increases. A decrease in $R_{MR1,\,2}$ would then lead to an increase in $\boldsymbol{f_{pA,\,B}}$and an increase in the phase margin. The design method for sizing MR1, 2 involves replacing transistors MR1, 2 with resistors R1, 2 as shown in Figure 5.5.

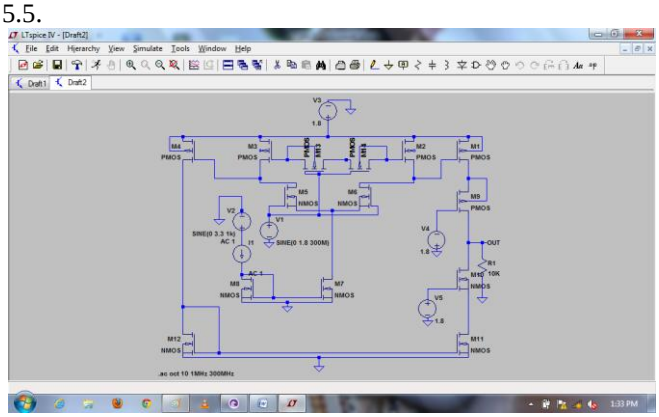

Figure 5.5 Schematic layout of Proposed OTA Circuit in LTSICE IV

A parametric step of resistors R1, 2 in simulation will then determine a desired range of resistance $\boldsymbol{(\Delta R_{MR1,\,2})}$ corresponding to a desired range of phase margin $\boldsymbol{(\Delta PM\approx 40°<PM<80°)}$. A parametric simulation of the structure shown in Figure 5.5, with core transistor sizes listed in Table 5.2, resulted in a resistance range of $\boldsymbol{(R_{MR,MIN}=200\Omega>R_{MR1,2}<R_{MR,MAX}=1000\Omega)}$ corresponding to a range of phase margin $\boldsymbol{(40°<PM<80°)}$. $\boldsymbol{W_{MR}}$and $\boldsymbol{L_{MR}}$can then be determined analytically by rearranging Equation (5.30) for the following:

$$\frac{W_{MR1,2}}{L_{MR1,2}}=\frac{1}{KP_P(V_C-V_R-V_{THP})R_{MR1,2}} \qquad 5.12$$

The voltage at node C (V_C) can be calculated, leaving the control voltage range $\boldsymbol{\Delta V_R=V_{RMAX}-V_{RMIN}}$as the unknown variables. Simultaneous functions of Equation (5.30) can then be solved for $\boldsymbol{W_{MR1,\,2}/L_{MR1,\,2}}$based on a voltage range ΔV_R that corresponds to the desired resistance range $\boldsymbol{\Delta R_{MR1,\,2}}$. Results are shown below in Table 5.2.

Table 5.2 SE-LCMFB MR1, 2 Design Transistor Sizes

PARAMETER	MINIMUM VALUE	MAXIMUM VALUE
Phase Margin	40°	90°
$R_{MR1,\,2}$	200	1000
V_R (V)	-1.75	-0.75
Transistors	$W_{MR1,\,2}$(µm)/$L_{MR1,\,2}$(µm)	
MR1, MR2	1.4/0.18 µm	
MB1	1.098/0.18 µm	
MB2	2.677/0.18 µm	

Table 5.3 Analysis Table

PARAMETERS	WORK(results)
Slew Rate (V/µs)	**910**
Bandwidth (GHz)	**2.4**
Maximum O/P Current	**0.5**

(mA)	
Static Power Dissipation (mW)	**4.95**
Phase Margin (Degree)	**88.3**

Simulation Results

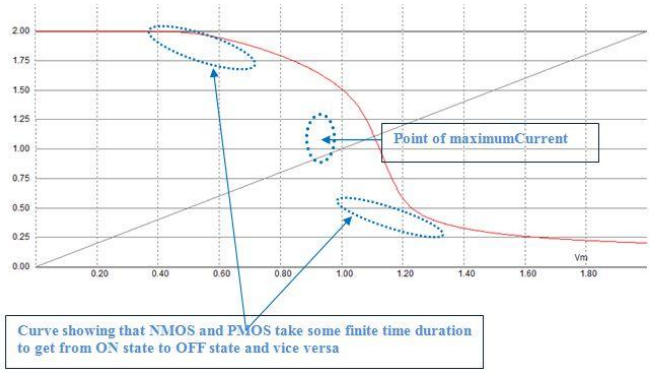

Figure 6.1 Output waveform of Differential Amplifier Circuit

The simulation result of the differential amplifier shown in figure 5.1 is shown above. It is a graph plotted between output voltage (y-axis) and input voltage (x-axis). It is evident that there is a point of maximum current shown by dotted circle. There are various regions of operation indicating the ON OFF time period of NMOS and PMOS. The curves indicate that NMOS and PMOS don't turn off or turn on instantly and take some finite duration.

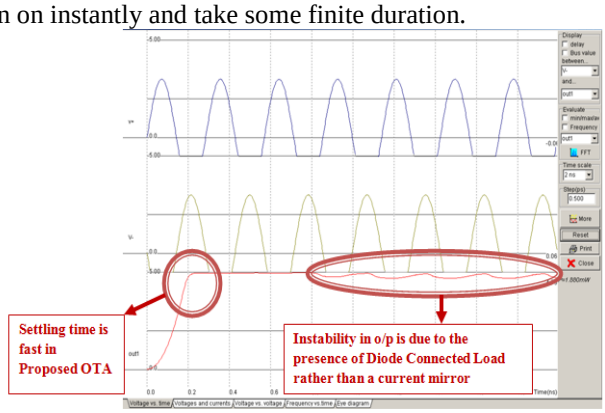

Figure 6.2 Output waveform of Proposed OTA Circuit

The simulation result of Proposed OTA Circuit (Figure 5.2) is shown above. From the simulation graph it is evident that settling time is fast and due to the presence of NMOS Diode connected load, rather than a current mirror circuit, the system is instable.

IV. CONCLUSION

An optimized compensation strategy for two-stage CMOS OTA has been proposed for a high frequency OPAMP design. Here, the slew rate and bandwidth has been increased by employing thin and long transistors into the design at output stage and wide transistors in input stage. These two techniques are able to increase the gain up to a great extent by increasing the output resistance and input transconductance respectively. There is a slight increase in static power dissipation of proposed architecture, but, the overall advantage of increased slew rate and gain bandwidth product which is very important parameter of communication so it compensates for this limitation.

FUTURE WORK

The single ended Local Common Mode Feedback Network CMOS Operational Transconductance Amplifier serves as prototype, and, hence, can be reconfigured to many OTA architectures to be used in smart cards, credit cards, etc. for random number generations. This single ended LCMFB CMOS OTA can be further enhanced to a fully differential LCMFB Operational Transconductance Amplifier for improved performance in gain and phase margin as well.

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