COMBINATION OF BATTERY-STORAGE SL Z-SOURCE CONVERTER AND PARALLEL INVERTERS IN HIGH-POWER APPLICATIONS

Reza Choupan[1], Mahmudreza Changizian[2], Farhad Sheikh Ansari[3], Mostafa Shakeri[4]
[1]Department of Electrical and Computer Engineering, Urmia University, Urmia, Iran.
[2]Department of Electrical and Computer Engineering, Iran University of Science and Technology, Iran.
[3]Department of Electrical and Computer Engineering, Sardar Jangal Institute of Higher Education, Iran.
[4]Department of Electrical and Computer Engineering, Shahrood University of Technology, Iran.

Abstract: ***This paper presents modeling, designing, and stability analysis of parallel-connected three-phase inverters for application in high power systems. To enlarge voltage adjustability, the proposed inverter employs an improved switched inductor Z-source impedance network to couple the main circuit and the power source. Compared with the classical Z-source inverter (ZSI) and switched inductor Z-source inverter (SL-ZSI), the proposed inverter significantly increases the voltage boost inversion ability and also can increase the power capacity and the reliability of inverter systems. The proposed topology and its performance are validated using simulation results which are obtained in Matlab/Simulink.***

Index Terms: Z-source inverter (ZSI), Switched inductor Z-source inverter (SL-ZSI), Modulation index, Voltage gain.

I. INTRODUCTION

In some renewable energy utilization applications, the input power source is a DC voltage source which has a wide voltage variation range, such as the grid-tied photovoltaic generation and fuel cell generation [1]. In these cases, an inverter with boost capability is required to generate electricity at low input DC voltage. Different inverter topologies meeting the requirement can be found and classified into two categories: the isolated inverters and non-isolated inverters. The isolated inverters are usually equipped with a step-up transformer which makes the system bulky and low efficiency while the non-isolated inverter is considered high efficiency and high power density [2]. There are typically two popular non-isolated topology candidates for these applications. One is the traditional two-stage boost-buck inverter, and the other one is the recently proposed Z-source inverter (ZSI) [3].

The ZSI presents a new single-stage structure to achieve the voltage boost/buck character in a single power conversion stage, which has been reported in applications to renewable energy systems. The ZSI has gained popularity as a single-stage buck-boost inverter topology among many researchers. However, its boosting capability could be limited and therefore it may not be suitable for some applications requiring very high boost demanding of cascading other dc-dc boost converters. This could lose the efficiency and demand more sensing for controlling the added new stages.

Over the recent years, more and more attention has been paid in many directions to develop ZSI to achieve different objectives [4]-[10]. In [11]-[13], the focus is on improving the boost factor of the ZSI. For instance, [11] and [12] add inductors, capacitors and diodes to the Z-impendence network to produce a high dc-link voltage for the main power circuit from a very low input dc voltage. In [13], two inductors of the impedance Z-network are replaced by a transformer with a turn ratio of 2:1 to obtain high voltage gain. These topologies suit solar cell and fuel cell applications that can require high voltage gain to match the source voltage difference.

Applying switched-capacitor, switched-inductor, hybrid switched-capacitor/switched-inductor structures, voltage-lift techniques, and voltage multiplier cells [14]-[16] to dc–dc conversion provides the high boost in cascade and transformerless structures with high efficiency and high power density. A successful combination of the ZSI and switched-inductor structure, called the switched inductor ZSI (SL-ZSI) [11], provides strong step-up inversion to overcome the boost limitation of the classical ZSI.

On the other hand, many industrial systems demand a reliable power supply [17]. One way to increase the reliability is to increase the number of sources. Different control strategies like Model Predictive Control also may be utilized to increase the reliability of power systems [18]. Another way to increase the reliability is to have parallel inverters and this would increase the redundancy as well as the maintainability of the inverters [19]. Moreover, the parallel connected inverters effectively offer a significantly higher level of availability than conventional approaches. Commercially available ratings range from several kVA to hundreds of kVA. Parallel connection techniques for inverters have been gaining increasing attentions in motor-drive systems, converter systems, and distributed generation systems [20]-[23].

Paralleled inverters can be built in numerous ways. First and the most obvious way is to have independent inverters with separate dc sources [24] and the other possibility is to connect the inverters into a common dc bus [25]. First method is common as it is simple. However, it requires more than one power source. In the context of Z-source inverter, this method requires more than one independent Z-source impedance network. Therefore, this paper proposes a new structure based on improved SL Z-source impedance network and parallel inverters which share one dc-input voltage to increase the output voltage in a wide range, usable

in renewable energy systems. Moreover, because of the divided output current among parallel inverters, the proposed topology has the ability of supplying high load currents.

The remainder of this paper is organized as follows. The next section is devoted to a detailed topology analysis of the improved SL Z-source impedance network. Operating principles and the equivalent circuit of the proposed topology are presented in section 3. Section 4 presents the simulationresults and finally, conclusions are included in Section 5.

II. CIRCUIT ANALYSIS OF IMPROVED SL Z-SOURCE IMPEDANCE NETWORK

As illustrated in Fig. 1, the proposed improved SL Z-source impedance network consists of four inductors, two capacitors, six diodes and two batteries. The combination ofL_1, L_3, D_1, D_2, D_3, $B_1$and the combination ofL_2, L_4, D_4, D_5, D_6, B_2 performs the function of the top SL cell and the bottom SL cell, respectively.

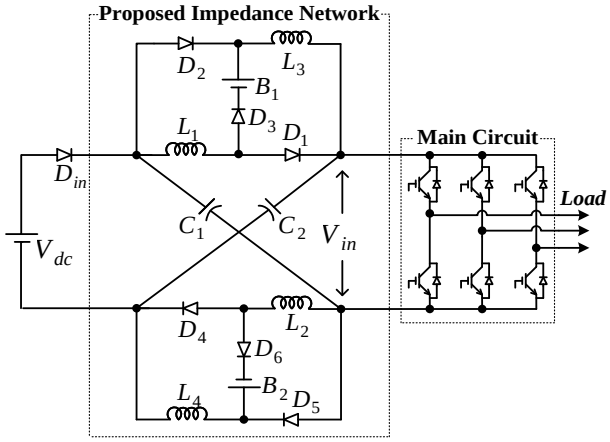

Fig. 1. Topology of the improved SL-ZSI.

From the viewpoint of the switching states of the main circuit connected with SL impedance network, the operation principles of this impedance network are similar to those of the classical Z-source impedance network. For the convenience of analysis, the equivalent circuit of the improved SL Z-source impedance network viewed from the dc bus is shown in Fig. 2(a) in which a virtual active switch S and a passive switch D0 are introduced to simulate the practical shoot-through actions of the top and bottom arms. Therefore, the sub-states of this impedance network are classified into the shoot-through state and the non-shoot-through state, respectively.

The circuit of the proposed topology during shoot-through state is shown in Fig. 2(b). In this state, Switch *S* is ON whileD_{in} and D_0 are OFF. The diodes D_3 and D_6 are also turned off, but the diodes D_1 and D_2 from top cell and D_4 and D_5 from bottom cell are conducting. In this condition, batteries are out of circuit because of the diodes D_3 and D_6 do not conduct.

Assuming that the four inductors (L_1, L_2, L_3andL_4) have the same inductance (L), two capacitors (C_1andC_2) have the same capacitance (C) and the value of two batteries (B_1andB_2) are equal. As a result, the network becomes symmetrical. From symmetrical circuit, the voltage across the capacitors and inductors become:

$$V_{C1} = V_{C2} = V_C \tag{1}$$

$$v_{L1} = v_{L2} = v_{L3} = v_{L4} = v_L \tag{2}$$

From Fig. 2(b) that shows the equivalent circuit of the shoot-through state:

$$v_L = V_C \ , v_{in} = 0 \tag{3}$$

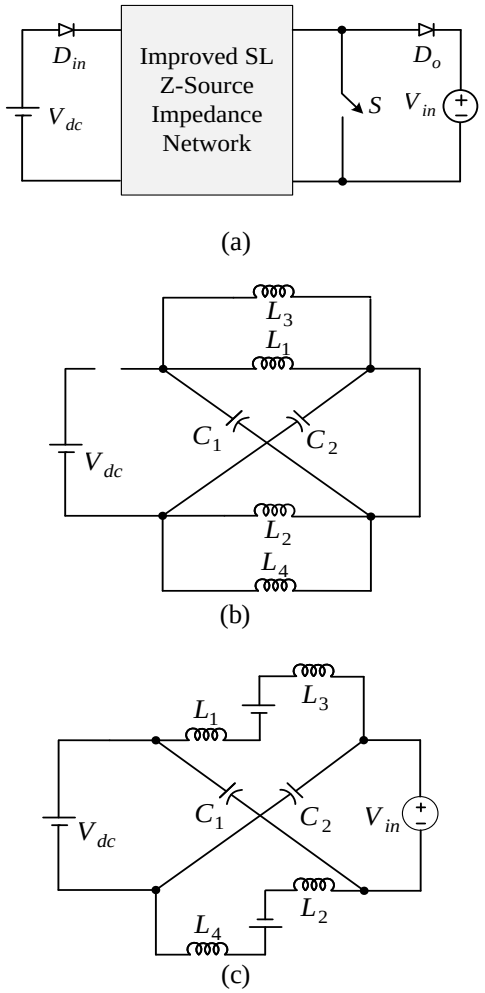

Fig. 2. Equivalent circuits. (a) Improved SL-ZSI viewed from the dc-link bus. (b) Shoot-through state. (c) Non-shoot-through state.

The equivalent circuit of the proposed topology in non-shoot-through state is depicted in Fig. 2(c). In this condition, the diodes D_{in}, D_0, D_3 and D_6 conduct and as a result the diodes D_1 and D_2 from top cell and D_4 and D_5 from bottom cell are turned off. Therefore, the batteries are in the circuit since the diodes D_3 and D_6 are conducting. Considering KVL in the left and right loop of the equivalent circuit shown in Fig. 2(c):

$$V_{dc} = v_{L1} - V_{B1} + v_{L3} + V_{C2} \quad (4)$$

$$v_{in} = V_{C1} + V_{B1} - v_{L1} - v_{L3} \quad (5)$$

In the above equations, V_{B1} is the voltage of battery B_1 that is equal to the voltage of battery B_2. Considering (3) and (5):

$$V_{dc} + V_B - V_C = 2v_L \quad (6)$$

$$v_{in} - V_C - V_B = -2v_L \quad (7)$$

From the volt-second law, the average voltage across inductors during each switching cycle T is zero. Therefore, the following equation can be derived:

$$V_L = \bar{v}_L = \frac{T_0 V_C + (T - T_0)\left(\frac{V_{dc} + V_B - V_C}{2}\right)}{T} = 0 \quad (8)$$

Where, $T_0$is the shoot-through time interval over a switching cycle, or $(T_0/T)=D$ is the shoot-through duty ratio.
From (6),

$$V_C = \frac{D-1}{3D-1}(V_{dc} + V_B) \quad (9)$$

By adding (6) and (7):

$$v_{in} = 2V_C - V_{dc} \quad (10)$$

Therefore, the peak dc-link voltage across the inverter bridge can be written:

$$\hat{v}_{in} = \frac{(-D-1)}{(3D-1)}V_{dc} + 2\frac{(D-1)}{(3D-1)}V_B \quad (11)$$

If the voltages of batteries and input voltage are considered to be equal (V_B=V_{dc}), the above equations can be summarized as:

$$\hat{v}_{in} = \frac{(3-D)}{(1-3D)}V_{dc} \quad (12)$$

Thus, the boost factor B is expressed as:

$$B = \frac{3-D}{1-3D} = \frac{3-(T_0/T)}{1-3(T_0/T)} \geq B_1 \geq B_0 \quad (13)$$

Where, B_0 and B_1 are defined as the boost factor of the classical Z-source and switched inductor Z-source impedance networks, respectively. Their expressions are given by [11] as:

$$B_0 = \frac{1}{1-2D}, B_1 = \frac{1+D}{1-3D} \quad (14)$$

For the comparison of the individual boost ability, the curves of the boost factor$B$versus the duty ratio$D$for improved SL Z-source, SL Z-source and classical Z-source impedance networks are shown in Fig. 3. As shown in Fig. 3, the boost ability of the improved SL Z-source impedance network is significantly increased compared with SL Z-source and classical Z-source impedance networks.

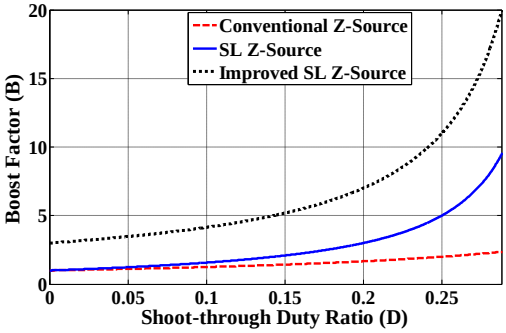

Fig. 3. Boost ability comparison.

III. PROPOSED TOPOLOGY

Parallel operation of inverters has many advantages such as modularity, ease of maintenance, $(n+1)$ redundancy, high reliability and many others [26-28]. In addition to these, output current ripple of the paralleled inverter can be reduced significantly by virtue of interleaving effect [29]. Fig. 4 shows the basic concept of the proposed improved SL Z-source impedance network with 2-parallel inverters.
It is assumed that inverters share the same dc bus that is fed from the improved switched inductor Z-source impedance network. Since the voltage at the point of common connection is derived from the switching of different power semiconductors, an intermodule reactor is absolutely necessary to interconnect the different inverters.

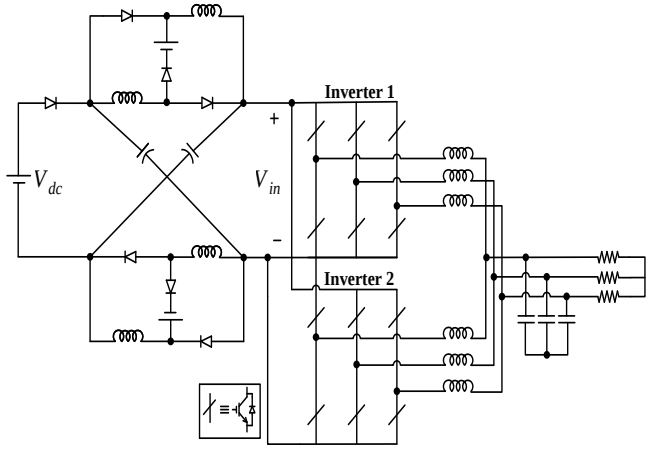

Fig. 4. Parallel improved SL Z-source inverters.

Fig. 5 shows the waveforms and switching strategy of maximum boost control method which has been explored in [4]. The key point for this method is that all zero states need to be turned into the shoot-through state so as to make the duty ratio as large as possible. Therefore, the shoot-through duty cycle varies in each cycle.
As described in [4], the average duty ratio of the shoot-through zero state, $\bar{D}$ is expressed by:

$$\bar{D} = \frac{\bar{T_0}}{T} = \frac{2\pi - 3\sqrt{3}M}{2\pi} \quad (15)$$

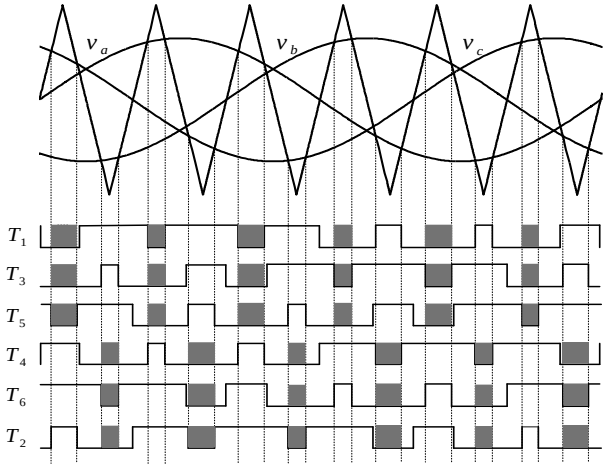

Fig. 5. Sketch map of maximum boost control.

Substituting (14) into (9), we can get the equivalent boost factor $\bar{B}$ under the condition of variable duty ratios:

$$\bar{B} = \frac{3 - \bar{D}}{1 - 3\bar{D}} = \frac{4\pi + 3\sqrt{3}M}{9\sqrt{3}M - 4\pi} \quad (16)$$

Therefore, the maximum voltage conversion ratioG_{max} versus any desired modulation index M approximates to:

$$G_{\max} = M\bar{B} = \frac{M(4\pi + 3\sqrt{3}M)}{9\sqrt{3}M - 4\pi} > G_{1-m} > G_{0-m} \quad (17)$$

Where, $G_{0\text{-}m}$and $G_{1\text{-}m}$are defined as the maximum voltage conversion ratio of the classical ZSI and SL-ZSI, respectively. Their expressionsare given by [10] as follows:

$$G_{0-m} = \frac{\pi M}{3\sqrt{3}M - \pi},\ G_{1-m} = \frac{M(4\pi - 3\sqrt{3}M)}{9\sqrt{3}M - 4\pi} \quad (18)$$

Fig. 6 shows the maximum obtainable voltage conversion ratios versus the given modulation index under the maximum boost control condition.It is shown that the voltage boost inversion abilities of theseinverters have been enhanced to a wider range by this method. So, the proposed inverter exhibits its advantage of stronger voltage boost inversion ability at the low modulation index.

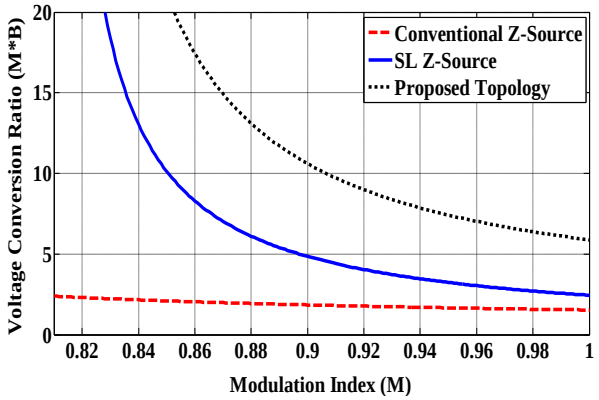

Fig. 6. Maximum voltage conversion ratio under the maximum boost control condition.

IV. SIMULATION RESULTS

Extensive computer simulation using Matlab-Simulink has been performed to prove performance of the proposed inverter. The simulation schematic for the proposed topology is shown in Fig. 4 and the selected parameters are: V_{dc}=V_{B1}=V_{B2}=*36*V, L_1=L_2=L_3=L_4=*1*mH, C_1=C_2=*500*μF, Switching frequency= *10*kHz, L_f=*1*mHand C_f=*22.5*μF (Three-phase output filter), Three-phase resistive load = 10/phase. In the simulation, all components are assumed ideal. The proposed topology is compared to the other topologies which have been proposed in [3] and [11], under the maximum boost control method with the same shoot-through duty ratio.

Under the condition of the maximum boost control, according to (14-16), we consider*M=0.967*. Therefore, we obtain $\bar{D} = 0.2$, $\bar{B} = 7$ andG_{max}=*6.769*. The simulation results for the proposed topology are plotted in Fig. 7, which are voltage across the inverters (V_{in}), voltage of capacitors (V_c), output voltage, current waveforms of the up and down inverters and also the load current waveform, respectively. Because the duty ratio varies periodically, a small oscillation has been introduced into V_{in} andV_c. All simulation results comply with the equations derived in sections 2 and 3.

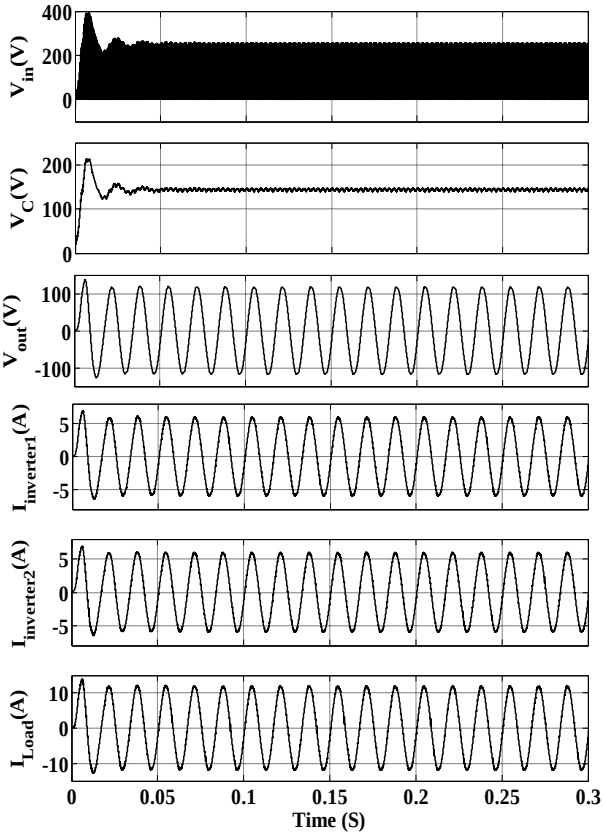

Fig. 7. Simulation results for the proposed topology.

For the case of the classical ZSI and SL-ZSI, when M is taken as 0.967, the boost inversion ability is still very weak. The corresponding parameters are: $\bar{B} = 1.668$, G_{max}=*1.613*for the classical ZSI and $\bar{B} = 3$, G_{max}=*2.901*for the SL-ZSI. The simulation results for these structures are shown in Figs. 8 and 9 respectively.

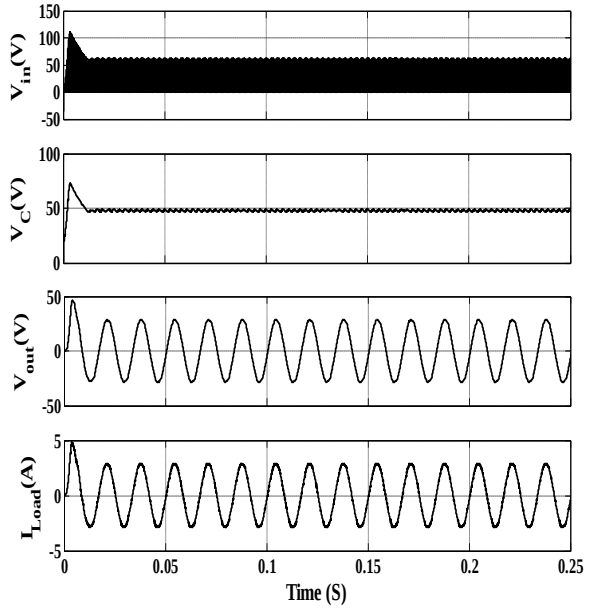

Fig. 8. Simulation results of the ZSI.

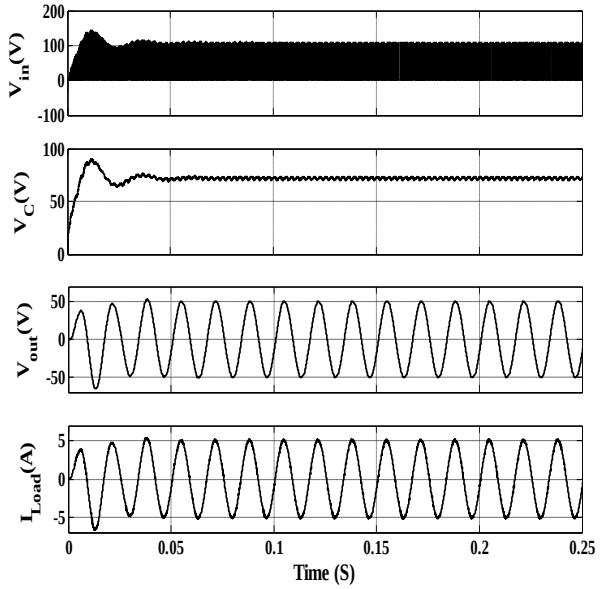

Fig. 9. Simulation results of the SL-ZSI.

V. CONCLUSION

This paper has presented a new hybrid structure based on improved switched inductor Z-source and parallel inverters to expand the range of system's voltage gain and supply high load currents. With this structure, the proposed inverter has the following features:

- The proposed inverter has all the advantages of paralleling power converters such as modularity, ease of maintenance, (*n+1*) redundancy, high reliability, reducing of the output current ripple, etc.
- It can be short- or open-circuited without damaging switching devices. Therefore, it is very resistant to EMI noise and therefore its robustness and reliability are significantly improved.
- The boost factor has been increased to*(1+2D)/(1-4D)*.
- Since here the load current can be divided between all inverters, in conditions where the load requires high current, the probable damages to the switches which can be caused by high currents are preventable.

The steady state operation is performed to analyze the boosting capability then it is validated by simulation results.

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