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POWER GATING ON DIFFERENT SINGLE BIT FULL ADDER 8T, BUFFER AND SCHMITT TRIGGER AT 180NM TECHNOLOGY

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Abstract: Power consumption has become a primary design consideration for IC designers. With exponential growth of electronics devices low power consumption becomes a very demandable in the market or in the electronic field. Full adder is the basic building block in all the electronics devices in ALU, microprocessor etc. Lowering the power consumption of full adder we can lower power consumption of any processor. Low power devices increase the reliability and reduce the packaging problem and also reduce the cost of any device. the major concern of the VLSI designers were area, speed and cost. In recent years, this has changed and power dissipation is being given increased weightage in comparison to area and speed.
Keywords: Adder cell, sleep transistor, leakage power, buffer cell, Schmitt trigger.

1. INTRODUCTION

With exponential growth of electronics devices like cellular device. Laptops, and multimedia have increase the demand of low power devices. As the chip density increasing it adds to packaging and reliability problems. As the power dissipation goes high as well as cost and packaging problem increases. Average power dissipation in CMOS digital circuits can be expressed as the sum of three components : 1) switching power due to capacitor charging and discharging .2) short circuit due to flow of supply from vdd to gnd 3) static power due to leakage current. Binary addition is basic and mostly used arithmetic operation in microprocessor, digital signal processors (DSP) etc. That's why adders are crucial building blocks in VLSI circuits and performance of these circuit also impact on the entire system.

In past year's different standard CMOS 10 transistor, 28 transistors, 14 transistors is most widely reported using pull up and pull down transistors. In mobile applications, designers work with limited leakage power specification. Power gating is well known technique where a sleep transistor is added between the actual ground rail and circuit ground .The device is turned off during the sleep mode to cut off the leakage path. This technique results in reduction of leakage current with minimal impact on the circuit performance. This paper will focus on reducing leakage power reduction during sleep to active mode operations. It implies that leakage power would contribute more than 50% total power so it becomes extremely essential to lower the static power without compromising the performance. Many well-known techniques are present to lower the leakage power. Power gating is one such technique in which uses sleep transistor which cut off a circuit block when the block is not switching.

As technologies have gotten miniaturized, power management has become a challenge. The current study provides an appropriate choice for leakage power minimization technique for a particular application by VLSI circuit designer bases on a sequential analytical approach. It 's concluded that the important performance parameters like dynamic power, leakage power, propagation delay, and therefore the PDP are strongly interrelated. There are several power reduction techniques present to scale back the power of the circuits. Every approach comes with a demerit that every transistor within the original, base case, traditional CMOS design leads to increasing no of the sleepy Transistor. Power consumption (dissipation) in digital circuits is primary concern because

It affects the chip life and circuit's efficiency because of the overheating of the circuit. Thus there's a requirement to reduce power dissipation as much as possible. There are different reasons for reducing the smaller transistors and shorter interconnects result in less capacitance and altogether increased the speed of the integrated circuit. Nonetheless, the extent of scaling is constrained by physical limitations like short-channel effects. The main consequences are the leakage currents contributing to massive static power dissipation. The leakage current increases with the scaling of device channel length. By using proposed to XNOR gates we become able to minimize transistor count of the full adder the subsequent decreasing power and delay. The delay has been measure between the time when the changing input reaches 50% of voltage level to the time it output reaches 50% of voltage level for both rising and fall transition for Sum and Cout. Many well-known techniques are present to lower leakage power.

Power consumption depending upon a specific application within the field of mobile communication, battery life has to

be maximized. This demands low power consumption by these devices.

Hence, the research on establishing high-performance adder cells becomes feverish. The designing of 1- bit full adders which forms the fundamental building blocks of all digital VLSI circuits has been undergoing to minimizing the transistor, minimizing power consumption, and increasing the speed. In CMOS circuit total power dissipation becomes a very important factor due to continuous scaling of a threshold voltage.

By using power gating techniques we are making circuits feasible for the low power applications like mobile, laptops, etc. After applying power gating techniques power consumption decreases as compared to the previous power level of the same circuit. Leakage reduction improves the efficiency of the circuits. The purpose of employing power gating in the circuits to reduce the sleep power by strongly shuts off the leakage path during sleep modes means there is no close loop between the supply and ground path. In this method at the stand by condition leakage power will be minimized. The simulation using tanner will show the greatly reduced power consumption by using power gating techniques.

1. To study the various low power techniques
2. To study the full adder circuits in cmos technology
3. To propose the new adder circuits with low power.
4. To propose the new low power CMOS buffer and Schmitt trigger.

2. POWER MINIMIZATION TECHNIQUE

MTCMOS

The low-power and high-performance design requirements of recent VLSI technology are often achieved by using MTCMOS technology. Low, normal, and high threshold voltage transistors are wont to design a CMOS circuit during this technique. With the scaling of CMOS technology, Supply and threshold voltages are reduced. Sub threshold leakage current increases exponentially with the lowering of threshold voltage. Multi-threshold CMOS (MTCMOS) is design technique during which high threshold sleep transistors are connected between the logic circuit and power or ground, thus creating a virtual supply rail or virtual ground rail, respectively. Fig shows MTCMOS circuit technology which satisfies both requirements of lowering threshold voltage to get high speed and reducing standby current for low power. It's been need to reduce the leakage power by placing a sleep transistor between actual ground rail and circuit ground (virtual ground). Here low leakage NMOS is employed as a sleep transistor. Estimation of ground bounce noise is completed when the circuit is connected to the sleep transistor. Many well-known use a high threshold voltage sleep transistor which cut-off a circuit block when the block isn't switching. This technique is present to lower leakage power. Power gating is one such technique.

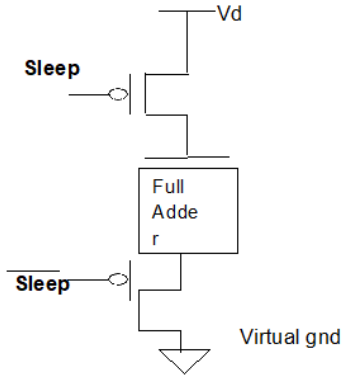


Fig.1.1 MTCMOS ARCHITECTURE

PROPOSED CIRCUITS

(A) 8T FULL ADDER BY MTCMOS

The 8-t full adder contains 3 modules two2-XNOR gates and a couple of transistors, multiplexer (2- TMUX). It can work on high speed with low power dissipation. By using proposed to XNOR gates we become ready to minimize transistor count of the complete adder the following decreasing power and delay. The delay has been measure between the time when the changing input reaches 50% of voltage level to the time it output reaches 50% of voltage level for both rising and fall transition for Sum and Cout. Many well-known techniques are present to lower leakage power. Power gating is one such technique.

This method uses a high threshold voltage sleep transistor which cut-off a circuit block when the block isn't switching. Here the sleep transistor is connected between actual ground rail and virtual ground. It increases time delays as power gated modes need to be safely entered and exited.

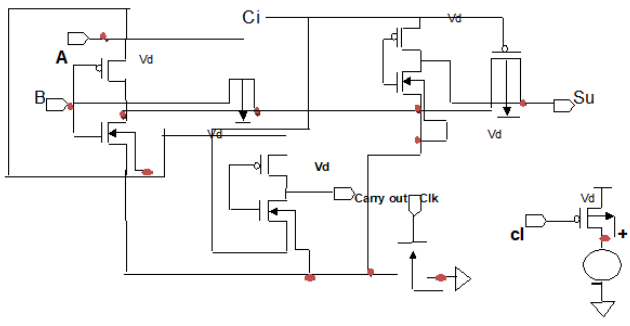


Fig1.2 8T Full adder by MTCMOS

CMOS BUFFER CKT

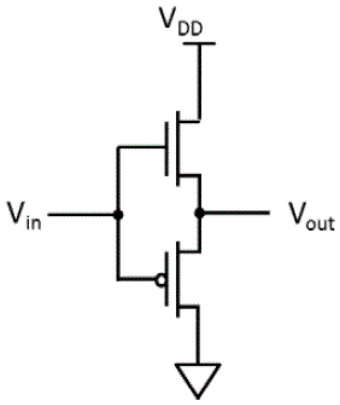


Fig.1.3 CMOS buffer

The buffer circuits take these input signals with imperfections and convert them into full digital logic levels by 'slicing' the info signals at correct levels which depends upon the switching point voltage. CMOS buffer topology's as word line drivers while driving large capacitive loads for minimizing power dissipation and propagation delay.

SCHMITT TRIGGER

There are two symbols for the Schmitt Trigger. The symbol is a triangle with an input and an output, just like the one used for the non-inverting buffers. Inside there is the hysteresis symbol. Depending on the sort of Schmitt Trigger, inverting, or non-inverting (standard), the hysteresis curve sign differs. The Schmitt Trigger is sort of comparator with two different threshold voltage levels. Whenever the input voltage goes over the High threshold value, the output of the comparator is switched HIGH (it is a standard ST) or LOW (it is an inverting ST). The output will remain during this state, as long because the input voltage is above the second threshold value, the Low threshold. When the input voltage goes below this level, the output of the Schmitt Trigger will switch.

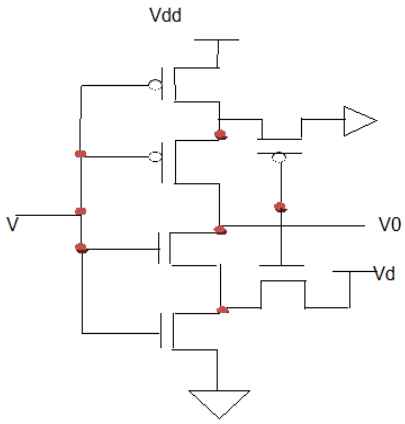
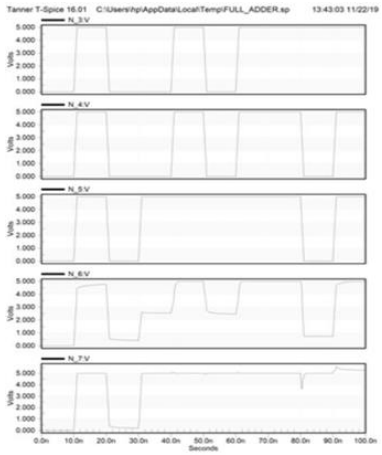


Fig.1.4 Schmitt trigger

The Schmitt Trigger is a comparator circuit that includes feedback. Schmitt triggers are extensively employed in digital also as analog systems to separate out any noise present during a signal line and produce a clean digital signal. The result has been compared in terms of power consumption.

8T FULL ADDER OUTPUT WAVEFORMS



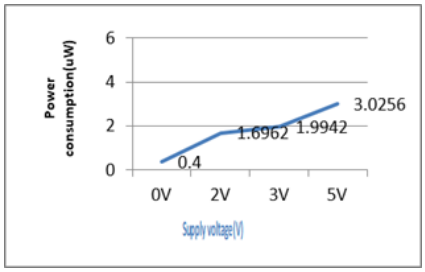


Fig.1.6 Power consumption of 8T full adder circuit

10T FULL ADDER OUTPUT WAVEFORMS

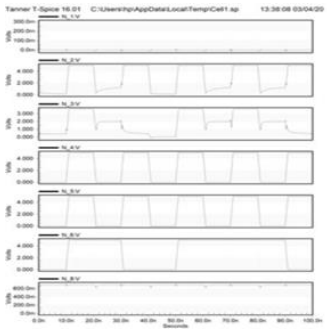


Fig.1.7 output waveforms

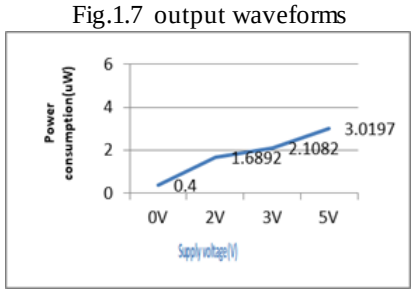


Fig.1.8 Power consumption of 10T full adder circuit

CMOS BUFFER OUTPUT

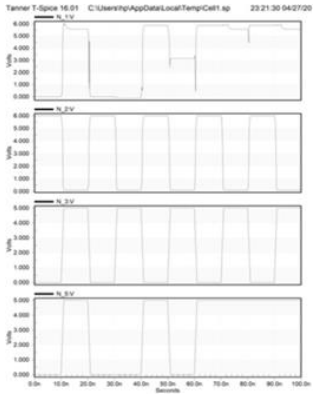


Fig 1.9 Output waveforms

POWER CONSUMPTION IN CMOS BUFFER

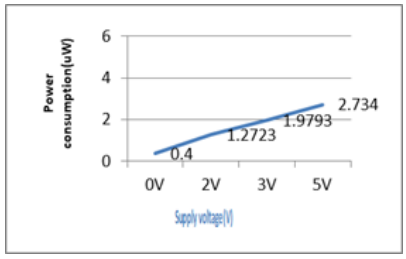


Fig 1.10 Power consumption of CMOS buffer with supply voltage

POWER CONSUMPTION IN SCHMITT TRIGGER

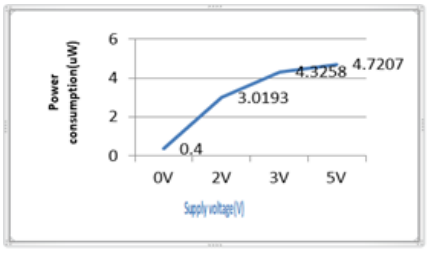
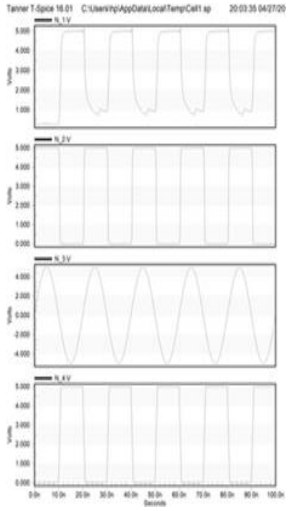


Fig 2.1Power consumption of Schmitt trigger with supply voltage

OUTPUT WAVFORMS OF SCHMITT TRIGGER



3. CONCLUSION

In this thesis existing techniques of power reduction which are power gating techniques are applied on all the circuits. Low power consumption is target at the circuit-design level. The work concludes that 8T , full adder , Schmitt trigger & cmos buffer cell with power gating technique is implemented where 2 sleep transistors are added between actual ground rail & circuit. This active power consists of dynamic power also because the static power so it's being named as active power. a. In VLSI design, an excellent deal of effort has been made to explore low-power and area design options. Gating techniques reduces the facility consumption into various ckt. All proposed circuits show less power consumption and better output levels. Table.1 shows power consumption at all together the circuits at 2.5v. Power consumption increases due to the no of transistors are increases. At 5V power supply 8T consumes 2.0256-2uW, Power consumption varies from 1.2745e-2uW to five .4255e-3uW with variation in power supply voltage from [2.5V-5V].

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