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ENERGY EFFICIENT ENCODING FOR NOC

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ABSTRACT: This paper deals with increasing energy efficiency of Network on Chips through reduction in switching activity and thereby reducing the dynamic power consumed by the chip. With the rise of new technologies, system on chip is having multiple cores along with memory, DMA, timers, ports on a single chip. Thereby a lot of power is consumed in data transfer in between the cores or memory on chip. This power consumed is switching power or dynamic power. Portable devices which are mostly battery operated will definitely go for techniques which help to conserve the power. Hence there is a need to reduce the dynamic power by reducing the switching activity on the internal buses of the system thereby optimizing the energy efficiency of Network on chips. We are presenting an unique way to reduce the switching activity on chips by encoding data packets. Thus this technique doesn't require modifying the on chip router or inter-connects. This simple idea is to encode data packets before they are transmitted on the internal bus in such way that there is a reduction in the switching activity on the bus. Along with data encoding it is necessary to minimize data losses while data transmission on the bus. Hence we have used LDPC codes for error checking. The Experiments carried out on simulator show that we can reduce dynamic power up to 35 percent without any significant performance degradation.
Index terms: network on chips, LDPC, data encoding, power analysis.

I. INTRODUCTION

According to Moore's law density of transistors on chip doubles every 18 months. In future the system on chips will have more number of cores. According to [2], there will be further rise in complex MPSoC. A network on chip is a communication subsystem on integrated circuit which transfers data packets between the Cores of the SoC. A NoC improves the power efficiency of the system on chip by managing data traffic on the system buses [3]. The power required to transfer data in between the cores is called as dynamic power or switching power. As the complexity grows the data transfers increases and thereby increasing the dynamic power. In this paper we will discuss the method of reducing this dynamic power by reducing the power dissipated in network interconnects (NI). The power dissipated in these interconnects can be reduced by coding the data to be transferred in such a way that the transitions are minimized. Thus we can reduce the switching activity on system buses and reduce the dynamic power. Also the channel might become noisy with increasing data traffic and in order to avoid the crosstalk we are using the Low Density Parity Check (LDPC) codes which are a linear error correcting code.

II. DATA ENCODING METHOD

This method is to encode data packets before transferring to network interfaces in such a way that the numbers of transitions are reduced. This can be achieved by comparing the current data cycle with the previous one. The following table illustrates the types of transitions based on the comparisons [1].

Time	Normal			Odd Inverted		
	Type I			Types II, III, and IV		
$t-1$	00, 11	00, 11, 01, 10	01, 10	00, 11	00, 11, 01, 10	01, 10
t	10, 01	01, 10, 00, 11	11, 00	11, 00	00, 11, 01, 10	10, 01
	T1*	T1**	T1***	Type III	Type IV	Type II
$t-1$	Type II			Type I		
t	01, 10			01, 10		
	10, 01			11, 00		
$t-1$	Type III			Type I		
t	00, 11			00, 11		
	11, 00			10, 01		
$t-1$	Type IV			Type I		
t	00, 11, 01, 10			00, 11, 01, 10		
	00, 11, 01, 10			01, 10, 00, 11		

Table 1:- Transition types

The amount of power dissipated in network interfaces for type I and II is higher than type III and IV. The idea is to encode data flits in such a way that the Type I & II transitions are converted in to the Type III & IV. Then this data flit is sent over on-chip communication channel so as to reduce self switching activity and coupling switching activity. In fact these two self switching and coupling switching account for most of the dynamic power. Once the data flit is out of network interface it is decoded back to original form. The following schematic illustrates the same.

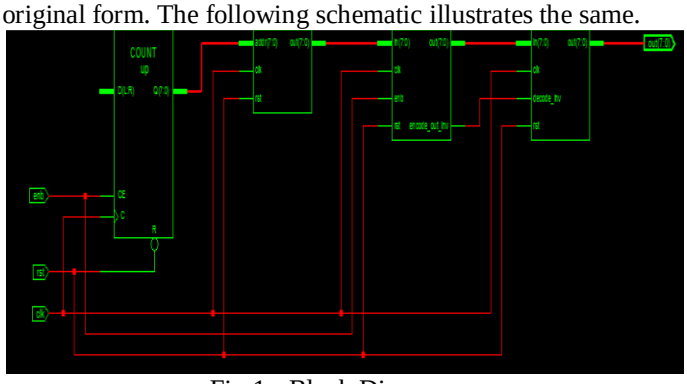

Fig 1:- Block Diagram

Encoder Architecture

The design of encoder is simple so as to keep area of the chip under check. The following figure explains the architecture [1].

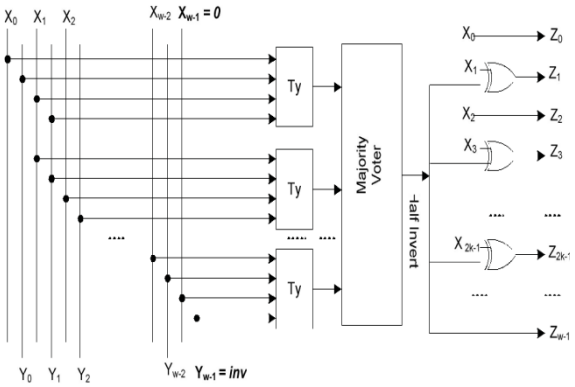

Fig 2: Encoder Architechture

Here the previous input is compared with the current input to determine a transition. The Ty block is set if there is a transition. The majority voter determines the number of transitions. If it is greater than half the bus width odd inversion is done on the current data flit using simple ex-or gates. After the odd inversion the Type I transitions are converted in Type III or IV whereas the Type II is converted in Type I. Thus it results in power reduction in switching activity.

III. PROPOSED SCHEME

In the proposed scheme we will use above mentioned power saving encoder in the Low Density parity check (LDPC) architecture. LDPC is a linear error correcting code which is used over a noisy channel due to its high reliability and simple decoder design. Each LDPC code in the set of LDPC codes is defined by a matrix **H** of size *m*-by-*n*, where *n* is the length of the code and *m* is the number of parity check bits in the code. The number of systematic bits is *k*=*n*-*m*.

The matrix **H** is defined as

$$\mathbf{H} = \begin{bmatrix} \mathbf{P}_{0,0} & \mathbf{P}_{0,1} & \mathbf{P}_{0,2} & \cdots & \mathbf{P}_{0,n_b-2} & \mathbf{P}_{0,n_b-1} \\ \mathbf{P}_{1,0} & \mathbf{P}_{1,1} & \mathbf{P}_{1,2} & \cdots & \mathbf{P}_{1,n_b-2} & \mathbf{P}_{1,n_b-1} \\ \mathbf{P}_{2,0} & \mathbf{P}_{2,1} & \mathbf{P}_{2,2} & \cdots & \mathbf{P}_{2,n_b-2} & \mathbf{P}_{2,n_b-1} \\ \vdots & \vdots & \vdots & \cdots & \vdots & \vdots \\ \mathbf{P}_{m_b-1,0} & \mathbf{P}_{m_b-1,1} & \mathbf{P}_{m_b-1,2} & \cdots & \mathbf{P}_{m_b-1,n_b-2} & \mathbf{P}_{m_b-1,n_b-1} \end{bmatrix} = \mathbf{P}^{H_b}$$

Where Pi,j is one of a set of z-by-z permutation matrices or a z-by-z zero matrix.[9][10].Although some extra bits are added due to LDPC encoding but the number of 1's are much less than the number of 0's. Here we are using Euclidean Geometry EG-LDPC with Majority logic decode (MLDD) as it uses little area overhead and are highly reliable [11]. EG (m, 2s) is a m-dimensional Euclidean geometry over the Galois field GF (2^s) where m and s are two positive integers. This geometry consists of 2^{ms} points, each point is simply an m-tuple over GF (2^s). The all-zero m-tuple 0 = (0, 0, …, 0) is called the origin. The 2^{ms} m-tuples over GF (2^s) that represent the points of EG (m, 2^s) form an m-dimensional vector space over GF (2^s). Therefore, EG (m, 2^s) is simply the m-dimensional vector space of all the 2^{ms} m-tuples over GF (2^s). A line in EG (m, 2^s) is either a one-dimensional subspace of EG (m, 2s) or a co-set of a one-dimensional subspace. Therefore, a line in EG (m, 2^s) consists of 2^spoints. There are $2^{(m-1)s}(2^{ms} - 1)/(2^s - 1)$ lines in EG(m,2^s) . Every line has $2^{(ms-1)} - 1$ 1 lines parallel to it. For any point in EG (m, 2^s), there are $(2^{ms} - 1)/(2^s - 1)$ lines intersecting at this point [11]. A EG-LDPC designed on Xilinx design suite is shown below

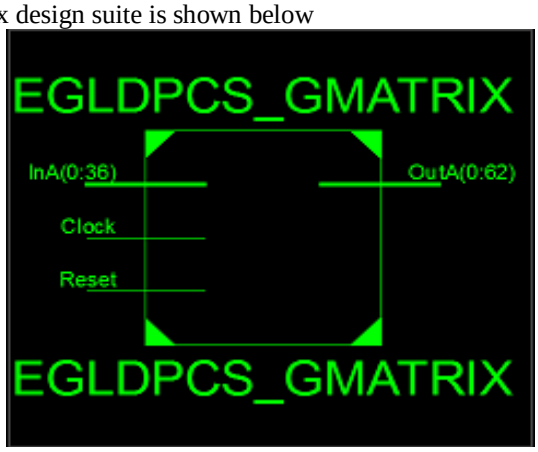

Fig 3: EG-LDPC

IV. RESULTS AND CONCLUSION

The above experiment was carried out on Xilinx design suite on random data. The following table 2 and table3 shows power output for normal LDPC and the proposed LDPC respectively. Comparing the tables we observe that the dynamic power is reduced from 0.11W to 0.7W. Thus a approximate 35 percent of dynamic power is reduced by using the proposed scheme. Whereas Table 4 shows the on chip area required for proposed scheme.

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.027	0.001	0.026
Vccaux	2.500	0.018	0.000	0.018
Vcco25	2.500	0.006	0.004	0.002
		Total	Dynamic	Quiescent
Supply Power (W)		0.092	0.011	0.081

Table 2:- power consumption for normal LDPC

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.027	0.001	0.026
Vccaux	2.500	0.018	0.000	0.018
Vcco25	2.500	0.004	0.002	0.002
		Total	Dynamic	Quiescent
Supply Power (W)		0.088	0.007	0.081

Table 3:- power consumption for proposed LDPC

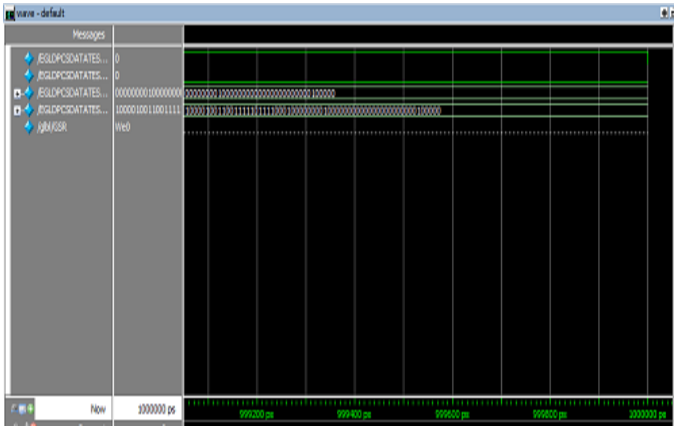

FIG 4: Output of EG-LDPC encoder on modelsim simulator

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of 4 input LUTs	97	9,312	1%
Number of occupied Slices	49	4,656	1%
Number of Slices containing only related logic	49	49	100%
Number of Slices containing unrelated logic	0	49	0%
Total Number of 4 input LUTs	97	9,312	1%
Number of bonded IOBs	102	232	43%
IOB Flip Flops	63		
Number of BUFGMUXs	1	24	4%
Average Fanout of Non-Clock Nets	2.78		

Table 4:- Device Utilization for proposed LDPC

Thus we can conclude that we are able to achieve dynamic power reductions with a little area overhead.

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