International Journal For Technological Research In Engineering
Volume 3, Issue 7, March-2016 *ISSN (Online): 2347 - 4718*

DESIGN OF LOW POWER MULTIPLIER USING CADENCE TOOL

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Abstract: This paper shows a low power and High Speed bypassing multiplier. The essential power decreases are gotten by tuning off MOS parts through multiplexers when the operands of multiplier are zero. The multiplier embraces ripple-carry adder with less extra equipment components. In addition, the bypassing architecture can improve operating speed by the extra parallel architecture to abbreviate the delay time of the multiplier. Both unsigned and signed operands of multiplier are produced. Post-layout simulations are performed with standard TSMC 0.18 mm CMOS innovation and 1.8 V supply voltage by Cadence Specter tools. Simulation results demonstrate that the proposed configuration can achieve more power efficiency with less additional equipment and power delay product among various counterparts. For 4x4 and 8x4 multiplier, dynamic,static power utilization and delay has been assessed. Consequently from this outcome, as the number transistor increments in both 4x4 and 8X4 multiplier, dynamic power utilization, static power utilization and delay diminishes bit by bit.
Keywords: Row bypassing multiplier, Ripple carry adder, Cadence Spectre simulatiion, 4x4 and 8x8 Multiplier.

I. INTRODUCTION

With the high requesting of electronic versatile devices, the requirement of low power device is getting more consideration lately. The essential concen of electronic compact device is to amplify working hours without changing the battery dwelling in device. although advanced innovation upgrades battery life to work for more hours, the complicated operations in the top of the line convenient gadgets are still power hungry and is basic for the low power outline. Low power configuration can be accomplished at framework, rationale, innovation, design, and the circuit levels. Power sparing can be significant if the low power configuration is arranged in the before stage at framework level. Enhancing rationale level of circuit is additionally basic for the low power outline. To achieve this objective, committed programming should be produced. As innovation keeps on contracting, power utilization additionally can be downsized in the meantime. Numerous endeavors to accomplish low power necessities at circuit level can be found in numerous literary works. These endeavors fluctuate from voltage scaling, threshold voltage scaling, power-down techniques, and logic style. These alternatives can be picked at circuit and topology level to actualize diverse math functions. For instance, to actualize a specific capacity at design level, ripple-carry, carry-save, or carry look-ahead adder can be embraced. By picking one of these designs, low power utilization can be accomplished by exchanging off with different specifications, for example, speed or chip region. Point of interest of tree-based multiplier depends on the rate of multiplier expanding with the log of operand length. Then again, array-based models are more mainstream as far as normal design. In any case, array-based multiplier devours possibly more power than tree-based design. The reason is that extra adders are implanted in the tree-based multiplier that assimilate spurious exchanging and thus diminish power consumption. Be that as it may, the format of tree-based multiplier has a tendency to be confounded and actuates more parasitic capacitances. Furthermore, tree-based multiplier is constrained to shorter operand length (16 bits).
Multiplier with longer operand length can be executed by modified Booth encoding Wallace multiplier. Accordingly, array-based engineering is executed in the proposed plan. Numerous specialists have been concentrating on diminishing power consumption of multipliers. A modified binary tree multiplier is presented. Every single incomplete product can be created in one stage. Power diminishment is accomplished by minimizing power consumption of full adder. A multiplier with array and tree architecture is proposed into upgrade execution with low power consumption and smaller time-delay product. The multiplier of partitions every single incomplete product into four clusters. It utilizes latches to cripple clusters when cluster is in zero condition. The low power multiplication is accomplished by operand decay. Decay is performed at both multiplicand and multiplier to accomplish low power consumption by reducing logic transitions.. In significant power consumptions are diminished by growing new adder cell in various multiplier designs.

Among these strategies, the best way is reducing dynamic power consumption which overwhelms total power consumption. Thus, normal power consumption can be decreased significantly by embracing this strategy. Thusly, this paper plans to build up another outline to accomplish lower power and rapid multiplier. Consequently, a novel low power multiplier is proposed by minimizing exchanging exercises of multiplier while adopting so as to keep up the velocity of multiplier the parallel architecture. Bypassing technique accomplishes significant power sparing if the quantity of zeros in multiplicand has more than half of the span of multiplier. Be that as it may, extra equipment of embracing bypassing technique diminishes the operation speed of multiplier in the critical path of multiplier. Thus, parallel architecture is embraced to upgrade the speed of multiplier.

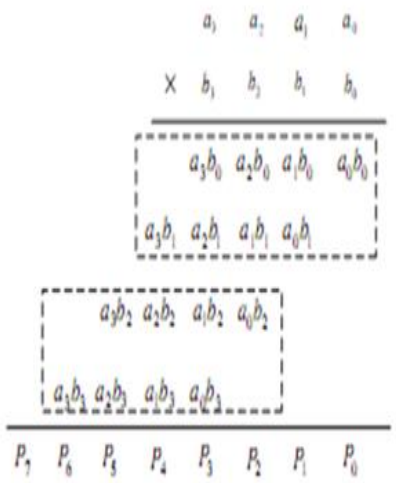

Fig.1. 4X4 Basic Multiplication

where α is switching probability, f is the average number of transitions, C_L is the output capacitance, V_{DD} is the supply voltage, I_{SC} is the short circuit current, and $I_{leakage}$ is the leakage current.

Power consumption is a basic parameter in planning electronic circuits, particularly in compact electronic and communication devices. CMOS technology has been generally utilized for VLSI circuit outline because of its impact of less power consumption. Power utilization of CMOS circuits can be isolated into static and dynamic power consumption. It indicates power consumption of advanced CMOS circuits. In the submicron technology, leakage current additionally expends significant bit of Power. Some leakage reduction strategies can be found. This paper predominantly concentrates on minimizing dynamic Power consumption of multiplier switching movement.

II. LITERATURE REVIEW

In this section, a short description of the papers reviewed for the improvement of proposed model is given The following are the papers gave a redesigned thought identifying with the present work. Different techniques being performed to accomplish the low power multiplier and different papers identified with treatment of the Cadence instrument is being exhibited.

M.K.Goswami et al;'Novel High Speed MCML 8-bit by 8-bit Multiplier', *IEEE Transaction vol (978-1-4673-0074-2)*

Expanding interest for high speed applications in communication has molded the requirement for exceptionally incorporated, fast multiplier. A logic style that is turning out to be progressively well known is MOS Current Mode Logic (MCML) because of its favorable circumstances over conventional CMOS logic for high speed applications. In this paper a 8-bit by 8-bit pipelined tree sort multiplier designed utilizing MCML, is displayed. An advancement technique for designing the general MCML gate for rapid application is discussed. The ideal throughput for the pipelined tree sort multiplier is acquired at 1.31GHz. All simulation are performed on a 0.6µm standard CMOS double metal double poly process, utilizing Cadence Design Tools.

Sushanta K. Mandal et al ; 'Low Power Multiplier Architectures Using Vedic Mathematics in 45nm Technology for High Speed Computing' *International Conference on Communication, Information & Computing Technology (ICCICT) jan 2015*

Speed and the general execution of any digital signal processor are to a great extent determined by the proficiency of the multiplier units present inside. The utilization of Vedic mathematics has brought about improvement in the execution of multiplier models utilized for high speed computing. This paper proposes 4-bit and 8-bit multiplier models in view of Urdhva Tiryakbhyam sutra. These low power designs are acknowledged in 45 nm CMOS Process innovation utilizing Cadence EDA instrument.

Naser Beyraghi, et al. " CMOS design of a low power and high precision four-quadrant analog multiplier "*International journal of electronics and communications vol 69 (2015)400-407.*

In this paper, a novel current-mode Four-quadrant simple multiplier is proposed. The recently designed current squarer circuits and one current mirror which all work in low supply voltage (2 V) are the essential building obstructs in acknowledgment of the numerical mathematical statements. The multiplier circuit is designed by utilizing 0.35µm standard CMOS innovation and to approve the circuit execution, the proposed multiplier has been reproduced in HSPICE test system. The reproduction results exhibit a linearity error of 0.17%, a THD of 0.16% in 1 MHz, a −3 dB transmission capacity of 485 MHz and a most extreme power consumption of 0.232 mW while the static force utilization is 0.111 mW.

III. PROPOSED SYSTEM

A. Unsigned Bypassing Multiplier Design

The array multiplier is made out of rows of adders as shown. The sum and carry signals are created from past rows and nourished into 2 of 3 inputs of current row. The force utilization can be lower if the moves of these data signals can be less regular. As demonstrated, the normal zero probability of data signals on various DSP applications is more than 73.8 percent. In this manner, the best approach to decrease the power of array based multiplier is to impair the move of adder. The operational principle of bypassing multiplier is discussed about. The CSA based bypassing multiplier can save certain power utilization.

The extra circuits by adopting bypassing strategy can degrade the operation speed of multiplier.CSA based multiplier can accomplish speedier operation speed contrasted with RCA based multiplier. Be that as it may, equipment cost is 50 percent more contrasted with conventional array multiplier. The proposed multiplier adopts the ripple-carry adder with less hardware parts and parallel design. The new bypassing design is proposed to improve operating speed and decrease power utilization of ripple-carry adder at same time.

A RCA adder is received with bypassing capacity in every

row of adders. The reason of adopting RCA adder rather than CSA adder is to accomplish parallel design.

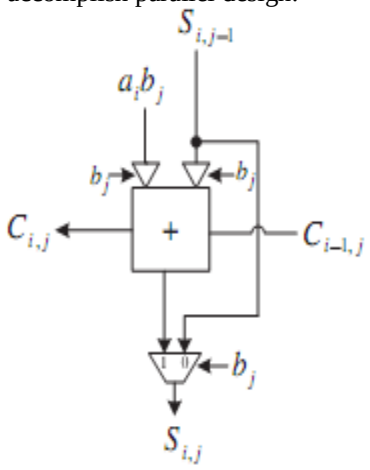

Fig.2. Proposed RCA with row bypassing technique

The two tri-state buffers are placed at two inputs of full adder to disable the operation of full adder when bj is 0. The tri-state buffer is designed by transmission gate (TG). The multiplexer is placed at the sum output of full adder. The value of sum can be selected from the bypassing value or sum output of full adder according to the value of bj. The proposed design does not need to add multiplexer for carry output and tri-state buffer for carry input of full adder. The reason is that two inputs of full adder in jth row need to be disabled while the value of bj is 0. Thus carry outputs of the full adders in the same row cannot be changed since two out of three-input full adder is disabled. Thereby, full adder only needs two tri-state buffers and one multiplexer. Moreover an AND gate is inserted into the last carry output in each row of full adder for correcting output when the value of bj is 0.

Therefore, significant portion of extra hardware can be saved without degrading speed performance. In addition, power consumption also can be reduced as a result of reduced hardware activities. It shows the proposed 4×4 multiplier based on the modified RCA full adder. The proposed RCA full adder only needs two tri-state buffers and one multiplexer. On the other hand, the full adder design in needs three tri-state buffers and two multiplexers. It is evident that the proposed design can reduce hardware area.

A multiplication test vector of 1111×1001 is set up for the proposed design shown. The values on the side of arrows indicate the value of sum bit or carry bit. From this example, the partial products which shall be summed in first and second row of adders are all zero because of b1=b2=0. Then, the sum of output equals to the results from previous row of adders. It is noteworthy that output carry bit of each full adder is zero in the same row and carry signal propagates with the same direction. Thus, we can discern that all carry signals propagate from zero to the next full adder in the jth row when the value of bj is 0.

Besides the above-mentioned method, the proposed multiplier also adopts parallel architecture to shorten delay time. The partial sums and carry output from these two 8×4 multipliers can be computed simultaneously. Note that the final stage adders consist of RCA adders in both sides and CSA adders in the middle. In this configuration, the parallelism of the proposed multiplier can be established. Furthermore, delay time of RCA multiplier can be shortened through this method. The proposed multiplier needs ((5/2) N-3) full adder delay in the worst case for N×N multiplier design. The proposed parallel architecture is not suitable for CSA based Braun multiplier. CSA based multiplier cannot be decomposed into two parallel 8×4 multipliers because the inputs of the current row CSA adder come from the upper row; the 16×16 signed multiplier can be designed by similar procedure.

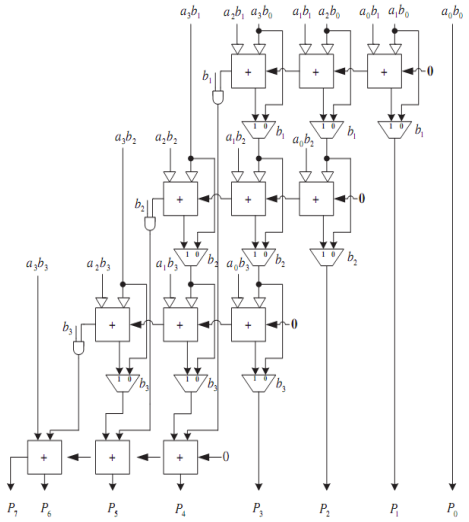

Fig.3. 4×4 Bypassing Multiplier Based On Carry Save Array

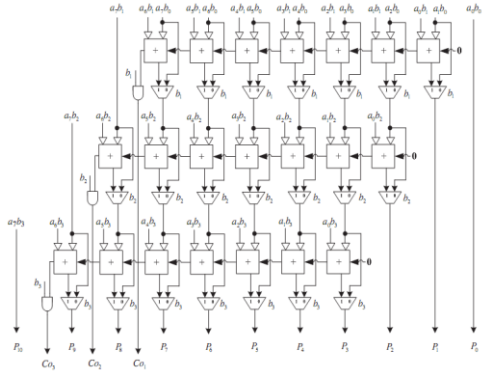

Fig.4. 8×4 Row Bypassing Multiplier Based On RCA

B. Signed Bypassing Multiplier Design

The multiplier introduced in the previous section is used to compute unsigned numbers. However, it is essential to design signed multipliers because computer system usually manipulates signed numbers. With regard to signed multiplier design, some signed multiplication algorithms are proposed .In conventional array multipliers such as Braun multiplier, signed multipliers can be realized through Baugh–Wooley multiplication algorithm, often used to deal with signed multiplication.

The algorithm uses 2's complement to represent the signed numbers and also uses the same framework of array multiplier. The advantage of this algorithm is accomplishing signed multiplication without expanding sign bits. Consequently, additional hardware cost is not increased;

thus, not dissipating extra power. Only the AND gate to NAND gate for corresponding operands is changed and an inverter is inserted at the final carry output. It shows the architecture of a 4×4 signed Braun multiplier.

For example, two signed 4-bits binary numbers $A = a_3 a_2 a_1 a_0$ and $B = b_3 b_2 b_1 b_0$ can generate a product P, which can be defined as follows:

$$P = 1\times 2^7 + a_3 b_3 2^6 + \left(\overline{a_3 b_2} + \overline{a_2 b_3}\right)2^5 + \left(\overline{a_3 b_1} + \overline{b_3 a_1} + 1\right)2^4 + \left(\overline{a_3 b_0} + \overline{b_3 a_0}\right)2^3 + \left(b_2 2^2 + b_1 2^1 + b_0\right)\left(a_2 2^2 + a_1 2^1 + a_0\right) \quad ----(3) \qquad (4.1)$$

Next, the same algorithm is utilized to design the proposed bypassing multiplier with signed operands. For bypassing multiplier, it could also utilize Baugh–Wooley multiplication algorithm to realize signed bypassing multiplier. According to Baugh-Wooley multiplication algorithm, some AND gates of original design must be changed to NAND gates for the corresponding operands. However, general CSA would be used instead of the modified full adders shown for the computation of last row of operands in multiplication. First, we know that disabling adders is performed only when operand is zero. The probability of a 2-input NAND gate with operand (AB)0 being zero is only 25 percent. If the adder shown is used for this row, additional logic must be added. Power consumption for these additional logics may be large. In others words, adders in this row may dissipate more power in most of time. Consequently, general CSA will be used for this row of adders because they do not dissipate power on the additional logic. Since it has to add one in the final step in Baugh–Wooley multiplication algorithm, additional one row of adders in the signed bypassing multiplier for carrying propagation is placed in the last row. The whole circuit architecture for a 4×4 signed bypassing multiplier is shown. The proposed multiplier also adopts the Baugh–Wooley algorithm for signed number multiplication. Considering an 8×8 signed multiplication, all operands are separated into two parts. Full adders are used to compute the last row of operands according to the analysis in the previous paragraph. Therefore, two different 8×4 bit signed ripple-carry array multipliers need to be designed. Blocks 1 and 2 are the two 8×4 bit signed ripple-carry array multipliers, respectively. Block 2 is different than Block 1 in hardware design as Block 1 uses the proposed full adder to compute all operands and Block 2 only differs in the computation of the last row of operands as ripple-carry adders are used to compute this row of operands. Since the proposed multiplier does not need additional full adder to correct the operation of multiplication, the addition in the final step can be computed without adding other full adders. Thus, hardware requirement for the proposed signed multiplier is less than the signed bypassing multiplier. Finally, these two blocks are combined and an inverter is placed at the carry output. The 16×16 signed multiplier can be designed by the similar procedure.

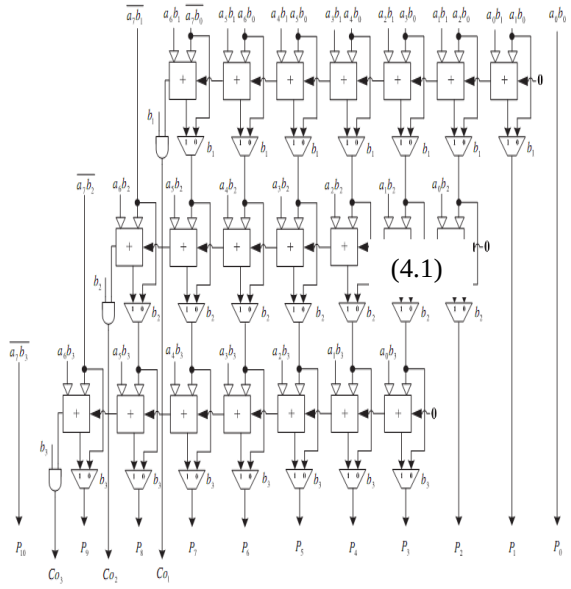

Fig.5. 8×4 signed RCA multiplier with row bypassing block1

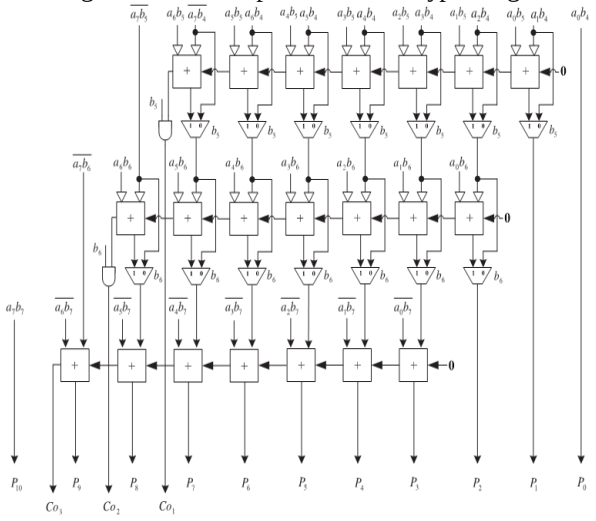

Fig.6. 8×4 signed RCA multiplier with row bypassing block 2

IV. RESULT AND DISCUSSION

In This section, the performance evaluation of the proposed multiplier along with the comparison to the conventional Braun multiplier is presented. Performances include power consumption, delay, and layout area. These circuits are designed in transistors level without using any standard cell from the technology library. Post-layout simulation formed with standardTSMC0.18mm CMOS technology and 1.8V supply voltage by Cadence Spectre simulation tools.

A. 4×4row Bypassing Multiplier Based On RCA

The 4X4 Row bypassing multiplier is designed by using cadence spectre simulation tools in order to finds its performance like dynamic power consumption, static power consumption and delay in the circuit operation.

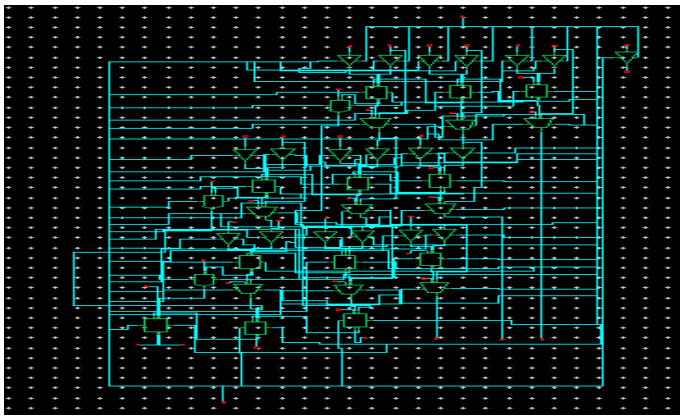

Fig.7. 4X4 Row Bypassing Multiplier.

B. 4x4 Multiplier Output:

The 4X4 multiplier is supplied with 0 to 1.8v in order to check how much delay(ns) and power(µW) is consumed by this multiplier.

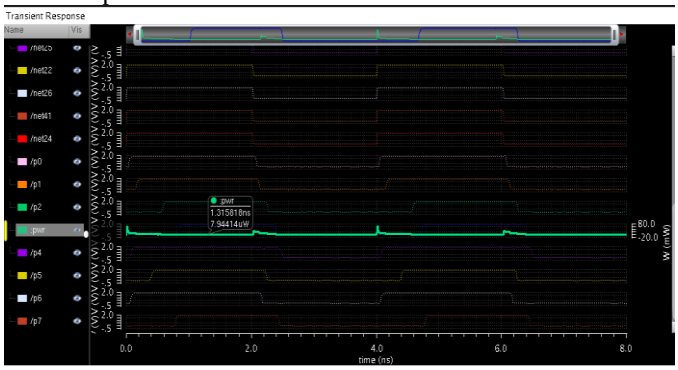

Fig.7. Simulated Output Of 4x4 Multiplier.

C. 8×4 Row Bypassing Multiplier Using RCA

The 8X4 Row bypassing multiplier is designed by using cadence spectre simulation tools in order to finds its performance like dynamic power consumption, static power consumption and delay in the circuit operation.

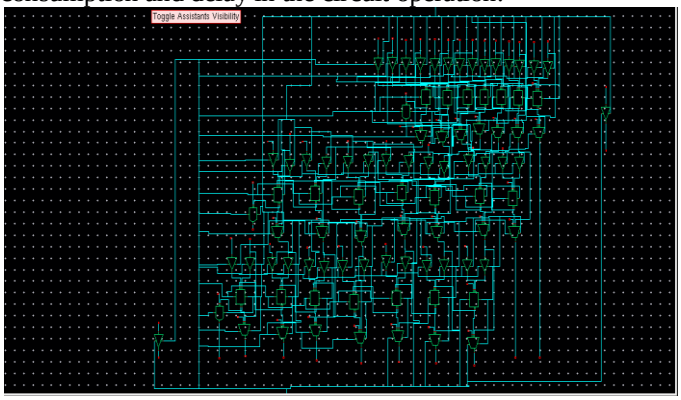

Fig.8. 8X4 Row Bypassing Multiplier.

D. 8x4 Multiplier Output

The 8X4 multiplier is supplied with 0 to 1.8v in order to check how much delay(ns) and power(µw)is consumed by this multiplier.

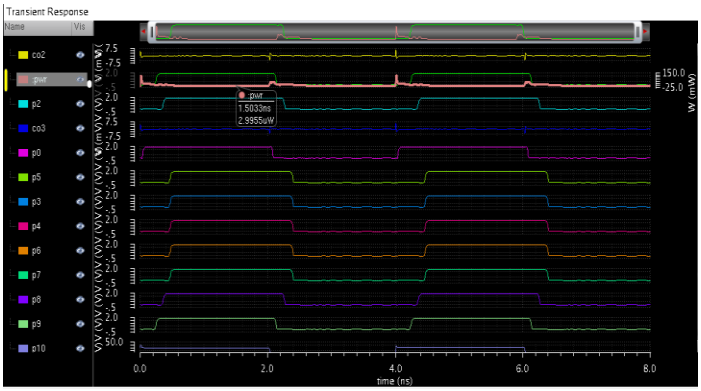

Fig.9. Simulated Output Of 4x4 Multiplier.

Thus the 4X4 and 8X4 row bypassing Multiplier has been designed. The dynamic power consumption, static power consumption and delay are calculated using Cadence Spectre simulator.

Table 1: Dynamic Power Consumption For Different Arrays

Types of adder	Dynamic Power	
Array	4X4	8X4
10T	4.55mW	9.20 mW
28T	1.88mW	5.34W

Table 2: Static Power Consumption For Different Arrays

Types of adder	Static power	
Array	4X4	8X4
10T	2.36 mW	5.32 mW
28T	1.88mW	3.71W

Table 3: Delay For Different Arrays

Types of adder	Delay	
Array	4X4	8X4
10T	954.853ps	565.839ps
28T	833.842ps	464.583 ps

For 4x4 and 8x4 multiplier, dynamic power, static power consumption and delay has been evaluated and its values are given in table I,II,III.

V. CONCLUSION

A low power and high speed CMOS array multiplier is presented. The proposed multiplier reduces power consumption by disabling adders resided in the multiplier when inputs are at zeros. Delay time of multiplier is also shortened by adopting parallel architecture. In order to validate the effectiveness of the proposed design, power consumption and delay are evaluated by Cadence Spectre post-layout simulation with standard TSMC 0.18 mm CMOS technology. Simulation results show that the proposed design can achieve greater power efficiency with less extra hardware and power-delay product among different counterparts. Hence from this result, as the number transistor increases in both 4x4 and 8X4 multiplier, dynamic power consumption, static power consumption and delay decreases gradually.

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