International Journal For Technological Research In Engineering
Volume 3, Issue 8, April-2016 *ISSN (Online): 2347 - 4718*

DESIGN OF POWER EFFICIENT ARCHITECTURE OF FIR FILTER ON FPGA FOR HIGH SPEED DSP SYSTEMS

Annapoorna M[1], Dr.Kurahatti N.G[2]
[1]Dept of ECE, EPCET, [2]Professor, Dept. of ECE, EPCET,
Bengaluru, KA

Abstract: In this paper, area and delay efficient architectures of FIR filter for high speed DSP systems are proposed. Most of the DSP applications demand faster adders for its arithmetic computations. To optimize, we proposed Carry Look Ahead Adder (CLA), Carry Save Adder (CSA), Wallace Tree Multiplier and Vedic Multiplier to reduce power and delay. These adders and multipliers are the fastest adders for its faster computation time. This work evaluates the performance of the proposed designs in terms of area, delay through Xilinx ISE 14.4(Verilog HDL) and this will be implemented in FPGA (Spartan 6).
Keywords: Carry Look Ahead Adder (CLA), Carry Save Adder (CSA), Wallace Tree Multiplier and Vedic Multiplier.

I. INTRODUCTION

In electronics, an adder or summer is a digital circuit that performs addition of numbers. Adders can be constructed for many numerical representations, such as BCD or Excess - 3; the most common adders operate on binary numbers. In [1] an improved differential coefficients method for realizing FIR filters, which offers considerable reduction of hardware and power consumption. In our NDCM-1, the minimal-difference differential coefficients are optimized using pseudo floating-point representation. Experimental results showed the average reductions of full adder, memory and energy.

Adders play major role in multiplications and other advanced processers designs. Filters shape the frequency spectrum of a sound signal. In [2] this paper they have presented a low power and low area FIR filter. To reduce power consumption and area they have used a combination of booth multiplier, low power serial multiplier and serial adder. In [3] this paper using computation reduction techniques which can either be used to obtain multiplier less implementation of finite impulse response (FIR) digital filters or to further improve multiplier less implementation obtained by currently used techniques. It was shown that about 20% further reduction in the number of add operations per coefficient can be obtained over the conventional multiplier less implementations. It is also shown that implementations requiring less than one adder per coefficient can be obtained using the presented approaches when using non-uniformly scaled coefficients quantized from infinite precision representation by simple rounding. In [4] a novel algorithm to solve the multiple constant multiplication problem i.e., the optimization of the multiplication of a variable by a set of constants, was proposed. The results show a significant reduction in either arithmetic operations or hardware necessary to implement those operations combined with satisfactory runtimes. Filters generally do not add frequency components to a signal that are not there to begin with. Boost or attenuate selected frequency regions. In computer music, an impulse is a very short pulse—a waveform that has significant amplitude only for a very short time (usually unipolar). For filters, we use a one-sample pulse, or unit impulse. The response of the filter to the unit impulse is the filter's Impulse Response (IR).

(1) Can be designed with exact linear phase.
(2) Filter structure always stable with quantized coefficients.

Disadvantages in using an FIR filter-

Order of an FIR filter is considerably higher than that of an equivalent IIR filter meeting the same specifications; this leads to higher computational complexity for FIR.

LTI system expressed in the z-domain:

$$Y(z) = X(z) * H(z)$$

where F(z) is the FIR's transfer function defined in z-domain by

$$Y(z) = \sum_{n=0}^{N-1} h(n) z^{-n}$$

The roots of polynomial F (z) define the zeros of the filter. FIRs are also called all zero filters.

II. METHODOLOGY

Literature survey on different FIR filter architectures has been carried out. Literature survey on different adders and multiplier units has been carried out. Simulink model of FIR filter was developed to understand the behavior. RTL has been developed for different adders, multipliers and FIR filters. RTL is simulated and functionality has been verified.

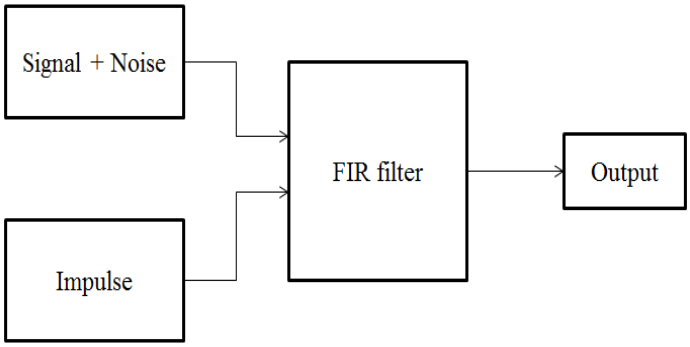

Fig 1: Block diagram of FIR filter

Figure-1 explains signal with noise and impulse is sent to

filter, impulse will remove unwanted components from the signal. In FIR filter, we can use different adders and multipliers for different architectures.

III. DESCRIPTION

Figure-2 explains a Carry-save adder. A carry-save adder is a type of digital adder, used in computer microarchitecture to compute the sum of three or more n-bit numbers in binary. It differs from other digital adders in that it outputs two numbers of the same dimensions as the inputs, one which is a sequence of partial sum bits and another which is a sequence of carry bits.

Figure-3 explains Carry look Ahead adder. A carry-look Ahead adder (CLA) or fast adder is a type of adder used in digital logic. A carry-look Ahead adder improves speed by reducing the amount of time required to determine carry bits. It can be contrasted with the simpler, but usually slower, ripple carry adder for which the carry bit is calculated alongside the sum bit, and each bit must wait until the previous carry has been calculated to begin calculating its own result and carry bits (see adder for detail on ripple carry adders). The carry-look Ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits.

Carry look Ahead logic uses the concepts of generating and propagating carries.

We are using this equation to predict carry,

$$C_{i+1} = G_i + (P_i \cdot C_i)$$

Notice that both the Propagate and Generate terms only depend on the input bits and thus will be valid after one gate delay. If one uses the above expression to calculate the carry signals.

The disadvantage of the carry-look Ahead adder is that the carry logic is getting quite complicated for more than 4 bits. For that reason, carry-look-ahead adders are usually implemented as 4-bit modules and are used in a hierarchical structure to realize adders that have multiples of 4 bits.

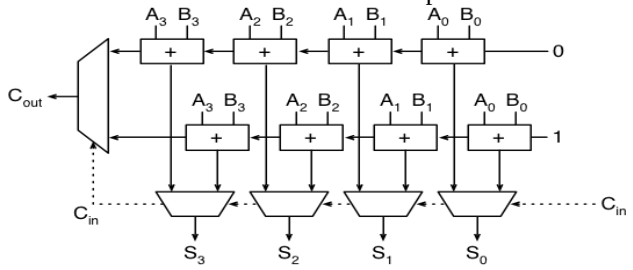

Fig 2: Carry save adder

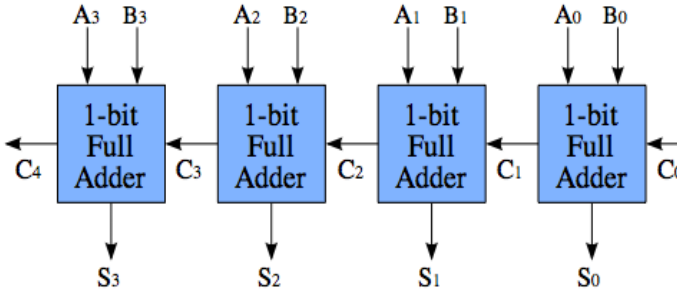

Fig 3: Carry look Ahead adder

Figure-4 explains signal flow of FIR filter. Filter is a device that removes unwanted frequency components from the signal. Digital filter is a system that performs mathematical operations on a sampled, discrete time signal to reduce or enhance certain aspects of that signal.

Where x(n) is the input, h(n) is the impulse response and y(n) is the output. Multiplier will multiply input and impulse response and gets added to another multiplied output and gives new output. It keeps on adding. Delay is one clock cycle. Here we can use different adders and multipliers in the adder and multiplier unit.

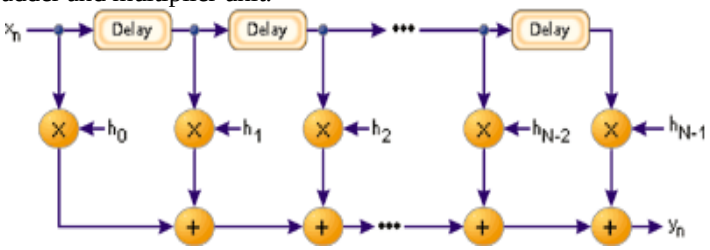

Fig 4: Signal Flow of FIR Filter

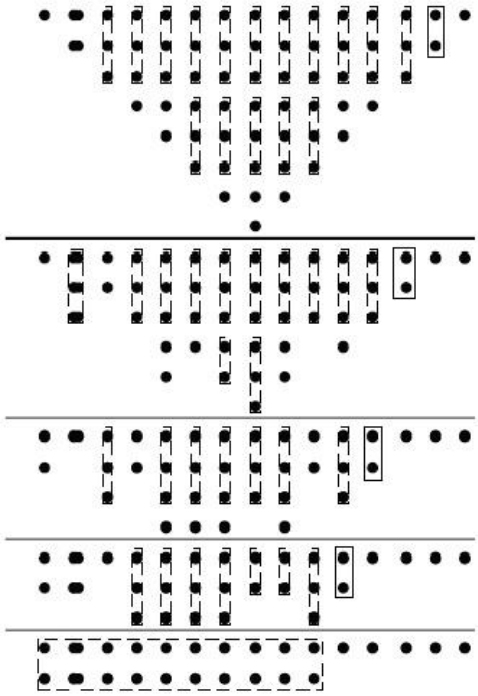

Fig 5: Architecture of Low Area Wallace Tree multiplier

From fig-5, several architectures have been proposed to perform the multiplication operations for serial as well as for parallel multipliers. The Wallace tree is found to be faster than the conventional array multiplier because its height is logarithmic in word size, not linear. The inputs to the Wallace tree is basically two unsigned integers. The Wallace tree requires large number of adder in each column to compute the summation of partial product bits. The designer's performed structural optimization in order to improve the latency of the total circuit.

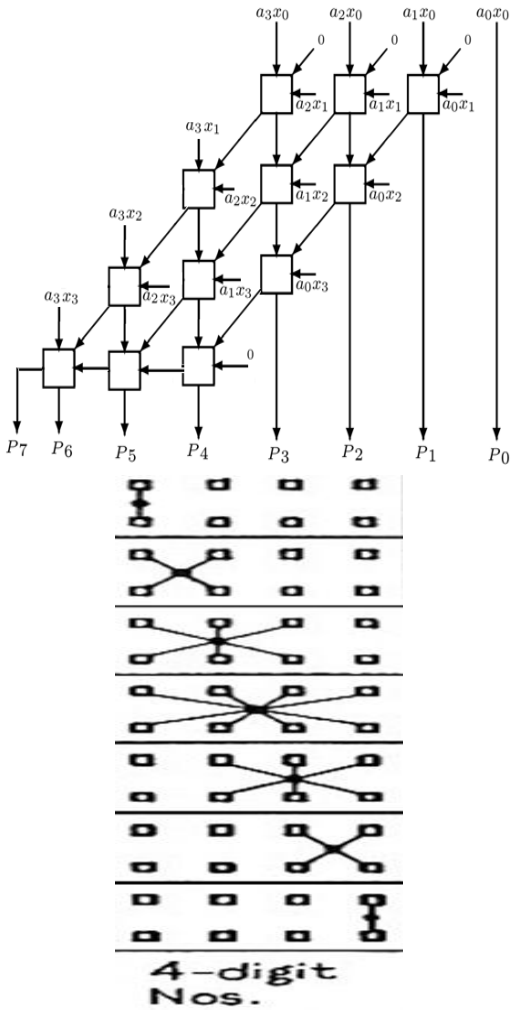

Fig 6: Vedic multiplier

Fig-6 explains write the rightmost digit of the starting number down. Add each pair of digits and write the results down, (carrying digits where necessary right to left).Finally write down the left most digit (adding any final carry if necessary) and continues.

IV. RESULTS

Delay and area is reduced using Carry look Ahead adder and Vedic multiplier. Simulation results for the proposed FIR filter design are shown in fig-7.

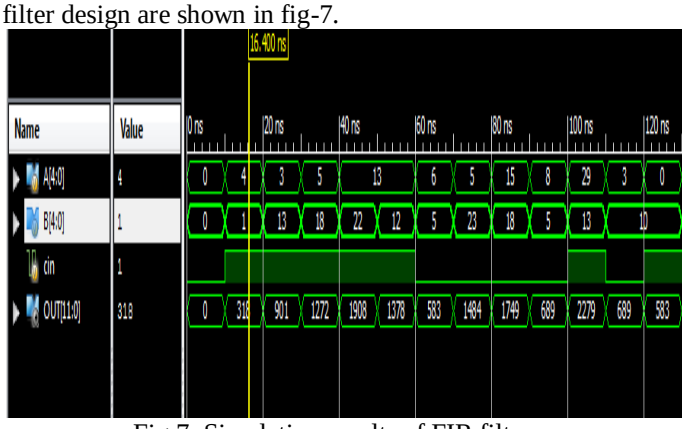

Fig 7: Simulation results of FIR filter

Using carry save adder and Vedic multiplier, delay and area has been reduced. Simulation results are shown in fig-8.

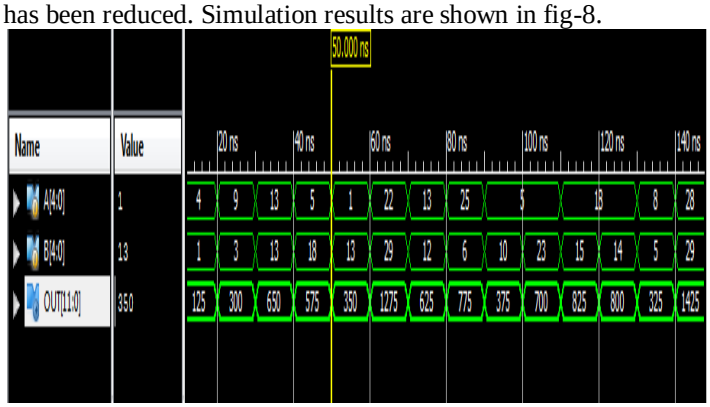

Fig 8: Simulation results of FIR filter

Table: Comparison of design parameters

Design	Area	Delay(ns)	Frequency(MHZ)
Carry look Ahead adder-Vedic	29	5.934	168.52
Carry look Ahead adder-Wallace	25	5.152	194.09
Carry save adder-Vedic	35	6.184	161.7
Carry save adder-Wallace	31	5.441	183.78

V. CONCLUSION

We have experimented on different adders and multipliers which reduces delay and area. Using a Carry Look Ahead adder, Carry save adder, Vedic multiplier and Wallace multiplier, we have proposed new FIR filter architecture. The best architecture is Carry Look Ahead adder and Wallace tree multiplier implemented in the FIR filter. The same design is prototyped on FPGA.

REFERENCES

[1] A.P. Vinod, A. Singla and C.H. Chang, "Low-power differential coefficients based FIR filters using hardware optimized multipliers", IET Circuits Devices System, vol.1, pp.13-22, 2007.

[2] Bahram Rashidi, Majid Pourormazd, "Design and implementation of low power digital FIR filter based on low power multipliers and adders on xilinx FPGA", DSP Journal, vol. 8, pp.21-29, 2008.

[3] K. Muhammad and K. Roy, "A graph theoretic approach for synthesizing very low-complexity high-speed digital filters", IEEE Trans.Computer-Aided Design, vol.21, no.2, pp.204-216, 2002.

[4] R. Pasko, P. Schaumont, V. Derudder, S.Vernade, and D. Durackova, "A new algorithm for elimination of common subexpressions", IEEE Trans. Computer-Aided Design, vol.18, no.1, pp.58-68,1999.

[5] K.H Chen and T.D Chiueh, "A low power digital based reconfigurable FIR filter", IEEE Trans. Circuits Syst. II, Exp. Briefs, vol.53, no.8, pp.617-

621, 2006.
[6] A.Senthilkumar, A.M.Natarajan, "Design and Implementation of Low Power Digital FIR Filters relying on Data Transition Power Diminution Technique", DSP Journal, vol. 8, pp.21-29, 2008.
[7] Shahzad Asif and Yinan Kong, "Low Area Wallace Multiplier",VLSI Design, vol.2014, Article ID 343960
[8] A.P. Vinod and E. Lai, "Low power and high speed implementation of FIR filters for software defined radio receivers", IEEE Trans. Wireless communication, vol.5, no.7, pp.1669-1675, 2006.

