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POWER EFFICIENT BIST USING BIT SWAPPING LFSR

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ABSTRACT: Bit Swapping Linear Feedback Shift Register (LFSR) is used to obtain pattern generators which are highly power efficient for Built-In-Self –Test (BIST) based VLSI architecture. BIST is a hardware entity and it has the ability of testing the circuit during manufacturing and also in situ conditions. BIST can use different types of random generations to generate test vectors which can achieve minimum fault coverage. Test pattern generations for VLSI testing fields demands low power designs, because the device dimensions are reducing drastically and most of them are made as portable devices (battery operated). Latest trends in test pattern generation consists of random pattern generator such as counter based circuits, scan chain based generators, LFSR in which LFSR is common. Bit Swapped LFSR based pattern generators are used to reduce transition power which is due to high switching activity in test vector generation. In this proposed design, a 25% reduction in power is attained. The above discussed BISTs were verified with a custom designed Circuit Under Test (CUT), defined in software simulators and result is shown on FPGA.

I. INTRODUCTION

Power Dissipation is a major challenging problem in System On Chips (SOCs) that contains a very large number of transistors. In CMOS technology, there are three types of Power Dissipation namely

Static Power Dissipation: It occurs when the gate output is stable.

$$P_{static} = V_{DD}.I_{leakage}$$

Short Circuit Power Dissipation: It occurs during switching when current flows from power supply to ground. It depends on short circuit current flowing to ground.

$$P_{short} = V_{DD}.I_{short}$$

Dynamic Power Dissipation: It is the predominant source of Power Dissipation in CMOS devices. It consists of approximately 90% of overall power consumption in CMOS. It occurs due to switching activities/

$$P_{dynamic} = \beta.C.V_{DD}^2.F$$

Where β is switching activity per node, C is Switched Capacitance, F is switching events per second, and VDD is Supply Voltage. Short circuit and Static Powers are of smaller magnitude than dynamic power. Therefore, dynamic power is a major source of CMOS power dissipation. In test mode, Power dissipation is more than normal mode. Power Dissipation increases during test because of high internal switching activities and due to extra design for test circuitry. This extra power consumption causes circuit damage, reduces the yield and life time of the product. In order to determine correct behavior of the Circuit Under Test (CUT), Automatic Test Equipment (ATE) are used to apply a test sets to CUT, but the cost of test pattern generator and equipment increases based on the complexity. Testability Design became an important solution which reduces both cost and test time by increasing controllability, observability and predictability of the circuit.

II. BUILT-IN-SELF-TEST (BIST)

BIST is an optimum solution for testing problems and provides maximum fault coverage. It is a Design For Testability (DFT) methodology, which detects faulty components in a circuit by integrating test circuit on the chip itself. Testing is faster and efficient because testing circuit is built into hardware. BIST has many advantages such as at-speed testing and reduces the need of expensive Automatic test equipment. Testing of internal modules and access to internal points is easy because of extra circuitry is built on the chip itself and testing can be done at normal operating speed. The cost of additional circuitry on chip is decreasing because of the betterment in the integration; hence BIST is a low cost test solution.

BIST consists of several blocks:

- Circuit Under Test (CUT): It can be combinational circuit or sequential circuit. It is the portion of the circuit to be tested.
- Test Pattern Generator (TPG): TPG generates test patterns for CUT.
- Test Controller: It controls the execution of the test.It provides signal to activate all blocks.If the signal from the test controller is 0, then the BIST is said to be in test mode and if the signal is 1, then the BIST is said to be in normal mode.
- ROM: It stores the signature which is to be compared with CUT output.
- Response Analyzer: It compares the test output with the stored response. If the test output matches with the stored response, then the CUT is non-faulty, otherwise circuit / chip is faulty.

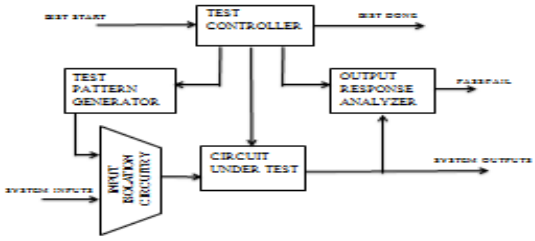

Figure 1: BIST basic block diagram

III. LINEAR FEEDBACK SHIFT REGISTER

LFSR is a linear feedback shift register whose input bit is a linear function of previous function that contains the signal through the register from one bit to the next most-significant when it is clocked. Linear feedback shift register can be made simple by performing exclusive-OR gate on the outputs of two or more of the flip-flops and feeding those outputs back in to the input of one of the flip-flops.

Drawback:

Linear Feedback Shift Register generates pseudo random patterns. This leads high switching activities and high power dissipation in CUT. LFSR needs to generate long pseudo random sequences to achieve target fault coverage.

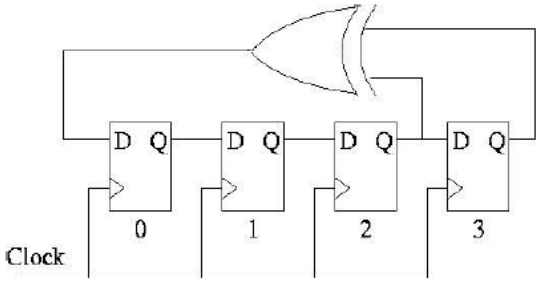

Figure 2: Diagram of Test Pattern generator using LFSR

IV. PROPOSED METHOD

A. BITSWAPPING LFSR

Bit swapping LFSR (BS LFSR) is a modified version of conventional LFSR which generate pseudo random pattern at output of LFSR with less transition between 0 and 1, which occur in the LFSR output stream. It reduces the average power dissipated by CUT because of reduction in internal switching activity. For the reduction of power, BS LFSR can be implemented either in Test-per-scan or Test-per-clock scheme. The power consumption of CUT mainly depends on the internal reduction of switching.

B. Basic Architecture of Bit Swapping LFSR

By reducing the number of transitions during test operation, BS LFSR reduces average and instantaneous, weighted switching activity. Power consumption can be reduced by several techniques. There are two direct techniques. In the first direct technique, frequency is reduced during testing which in turn reduces power dissipation. This technique does not require extra hardware. In the second direct technique, CUT is partitioned into blocks by applying appropriate test planning, to decrease power consumption. These direct techniques are not applicable for peak power reduction and also increase the test timing. BS LFSR reduces average and peak power dissipated by CUT, compared to other techniques.

C. Bit Swapping technique:

Consider an n-bit maximal length LFSR. Let one of its outputs (last bit i.e. n^{th} bit) to be a selection line that will swap two neighboring bits. If the value of selection line is set to 0 for swapping and n is made odd (bit n=0), then bit 1 will be swapped with bit 2, bit 3 is swapped with bit 4…..bit n-2 with bit n-1. If n is made even (bit n=0), then bit will be swapped with bit 2, bit 3 with bit 4…bit n-3 with bit n-2. If n=1, then no swapping operation is performed. The number of transitions is saved by using swapping arrangement. Let n=8.

The number of transitions saved by swapping = $T_{saved} = 2^6$

The number of transitions without swapping = $2x2^7 = 2^8$

Therefore by swapping bits,

$T_{saved} = 2^6/2^8 = 25\%$saved

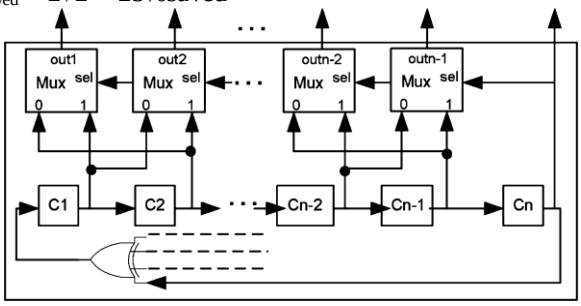

Figure 3: General architecture of Bit swapping LFSR

V. METHODOLOGY

- Bit Swapping Test pattern generator:Here Bit Swapping Linear feedback shift register is used for generating test patterns with reduced switching activities. Random patterns are generated using multiplexers and flip flops. These random numbers is sent as address to both Data memory and Signature memory.
- Data memory: The address is generated by BS LFSR. 256 different input values are saved in the data memory. The values pointed by that address is taken as input to the MUX when CHECK is 0.
- Circuit Under Test (CUT): Here 8x8 Vedic multiplier is designed as CUT. The input values are taken from Data memory when check is 0, else input values are taken manually. Then product is obtained.
- Signature Memory: The address is generated by BS LFSR. 256 different product values are saved in the signature memory. The product obtained from CUT is compared with the value stored in the signature memory addressed by BS LFSR. If the both values match, then valid bit is set to 1, else 0.

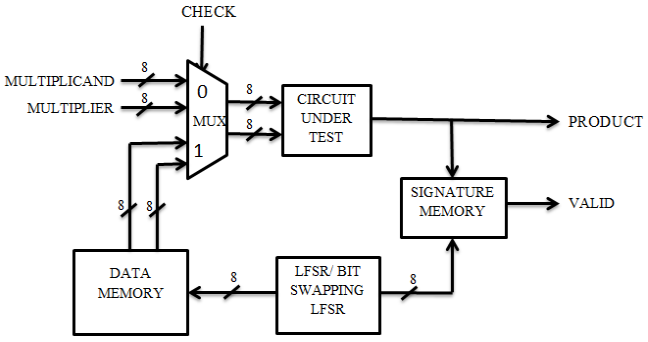

Figure 4: Block diagram of BIST using BS LFSR

VI. RESULTS

In this paper, simulation is done on Xilinx 14.7 version and model sim 6.3f. Power and area results are calculated for Conventional LFSR and BS LFSR.

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	57	1,920	2%	
Number of 4 input LUTs	683	1,920	35%	
Number of occupied Slices	398	960	41%	
Number of Slices containing only related logic	398	398	100%	
Number of Slices containing unrelated logic	0	398	0%	
Total Number of 4 input LUTs	684	1,920	35%	
Number used as logic	683			
Number used as a route-thru	1			
Number of bonded IOBs	44	66	66%	
Number of BUFGMUXs	1	24	4%	

Figure 5: Area result of modified LFSR

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	352	960	36%
Number of Slice Flip Flops	57	1920	2%
Number of 4 input LUTs	653	1920	34%
Number of bonded IOBs	39	66	59%
Number of GCLKs	1	24	4%

Figure 6: Area result of conventional LFSR

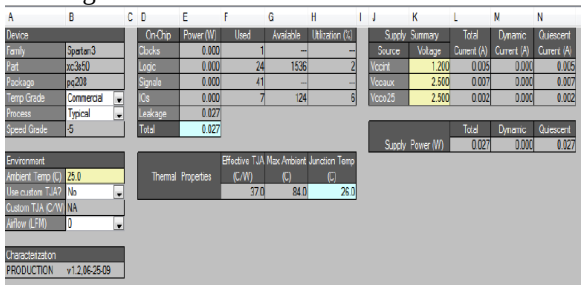

Figure 7: Power result of BS LFSR

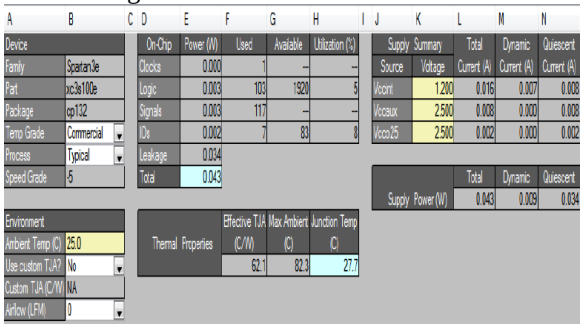

Figure 8: Power result of normal LFSR

VII. CONCLUSION

LFSR are widely used in digital circuit diagnostics to generate test patterns and to compress the output sequences of the CUT. This paper presented the design of aBit Swapping LFSR using Verilog which has the characteristics of low power consumption and suitable in processing environment where uniform distribution random numbers are required. Results show that Bit-swapping LFSR reduce transition states. Comparison between implemented BIST schemes by normal LFSR and Bit-swapping LFSR show that Bit-swapping LFSR can easily replace the normal LFSR for better result. The experimental results on Xilinx tool shows the effectiveness of proposed method and 25% reductions in dynamic power with respect to the conventional LFSR.

Test Pattern Generator	Dynamic Power
Conventional LFSR	0.43W
Bit Swapping LFSR	0.27W

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