TESTING OF APPLICATION COMMANDS USING EXECUTE IN PLACE FLASH MEMORY CHIP

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Abstract: In This document, we are raising the test set and test corroborates features of the EcoXIP chip. The span of this paper is to intend the design and Test Suiting the Applications has to be work on the microcontroller platform and interface with the FPGA Board to test commands [1] with the trade of the flash memory chip.
Keywords: EcoXIP, FPGA, flash memory

I. INTRODUCTION

The flash chip is a very faster flashing memory device which is mostly helpful in real time applications. The application code is executed through flash memory. The flash chip is added with the more accurate Erase function which helps for providing space for data storing and eliminating the dummy bytes in the memory location to get more storage space. This flash chip is worked out accurately for execute-in-Place (XiP) operations. This includes in the place where protocol allows the next cache line to be catched faster.

The flash chip supports two lines of data bus, four lines of data buses and also eight lines of data buses for the operational commands. The NOR flash device having a information Strobe (IS) extra pin for faster transferring of information from the master device to output slave device which helps as a signal that is synchronous to the output information. The NOR flash memory of this device uses only single 1.8V power supply, the device also supports many operational functions such as reading, writing or programming and erase operations additional power supply is not required. This device is having over all 10 pins.

They are selecting the chip, rate signal, serially input pin, information strobe pin, Clutch pin, and four input /output pins and etc [7]. There are namely three varieties of operations taking place, single method, quad method and octal interfacing method. The important application commands are reading array, block erasing, sequential programming command, program or erase suspending, write enabling ,write disabling, data one time programmable registers command, power downing commands and etc. With the help of microcontroller master device and FPGA platform [4].

II. PROBLEM STATEMENT

"Problem statement is to testing the application commands on the bases of serial NOR Flash."

III. IMPLEMENTATION

The flash memory device is especially helpful for optimizing the execution. This is the improved command version that is having more than 75% faster execution ability [9]. Here, we are developing the testing the commands which are made to work on the microcontroller board platform and are tested and communicate with the help of FPGA platform.

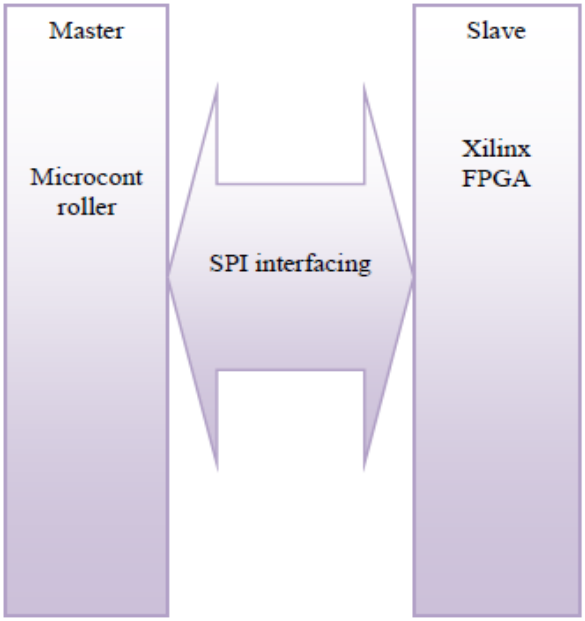

Fig.1. Diagram of SPI Interfacing

This NOR flash device memory is a high speed serially interface communication bus, which has used in consumer based application devices [2] [3]The microcontroller device has this memory chip and is communicates to the slave device. By using single interfacing bus or quad interfacing bus method or octal interfacing bus method, there is a connection takes place between master device and slave devices. The instruction or operation is always be begin by first activating the fragment select operational pin. After this fragment select pin is activated, the microcontroller device must have to transfer a valid 16 bit opcode on the bus [5]. The master then clock out a valid 16 bit opcode on the bus system after the opcode transmission, data bytes would then be clocked out by the master device. Each and every opcodes, address bytes and data bytes are transferred having the most significant bit first and there after least significant bit [6]. An operation is ended or terminated by deasserting or deactivating the fragment select pin.

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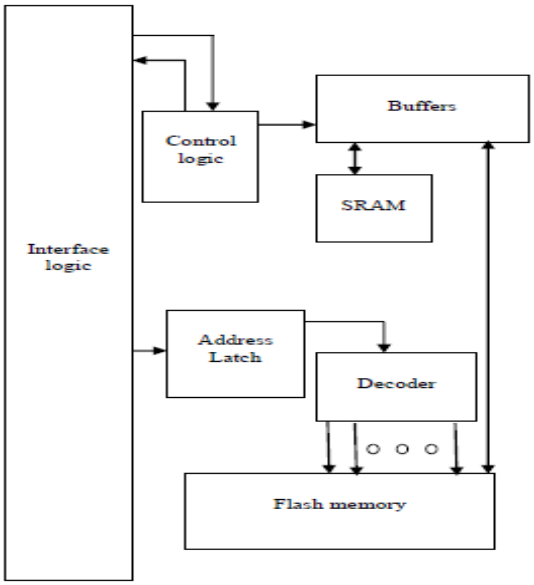

Fig. 2. Block Diagram of the Application

IV. PERFORMANCE RESULTS

Presentation can be done with the help of Vivado tool. The flow chart is shown in the Fig. 3. The functional commands are tested by transferring the commands from microcontroller device as master to the FPGA. The commands are demonstrated with the help of timing diagrams and those performances are shown in the screenshots. After transporting the opcodes [7], the address bytes are sent in. For quicker results supplementary dummy bytes are essential and are clocked into the slave device. For dissimilar methods of operations different dummy bytes are transferred. For solitary method of operation only one dummy byte are transferred. For courtyard and Octal, two or more dummy bytes are sent to the slave device. The courtyard method shows very fast throughput and these results are verified with the help of timing diagrams of fig4, fig 5, fig6 and fig7.

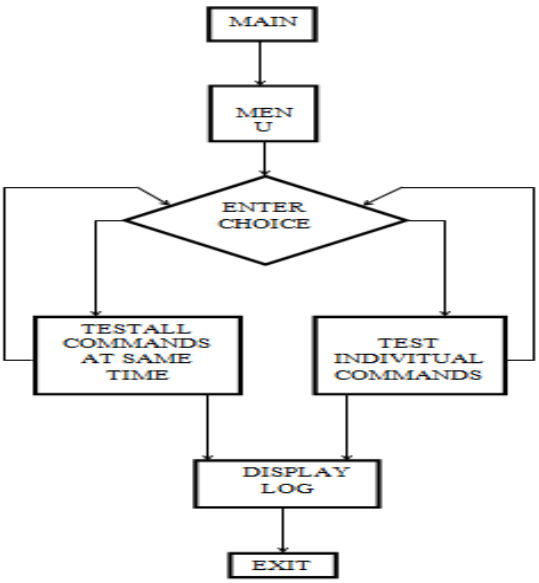

Fig. 3. Flow Chart for Testing the Application

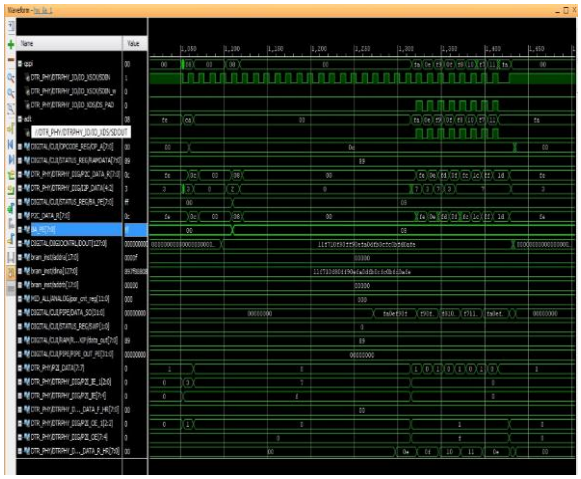

Fig. 4.Screenshot of fragment Erasing

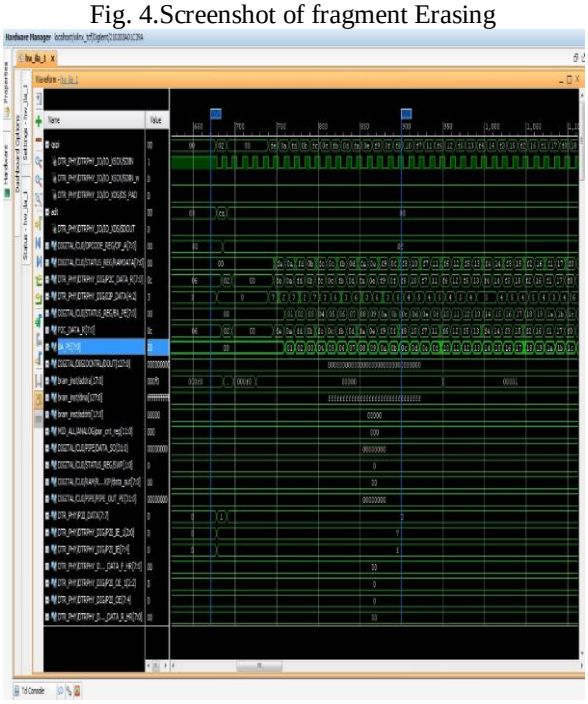

Fig. 5.Screenshot of Protect segment

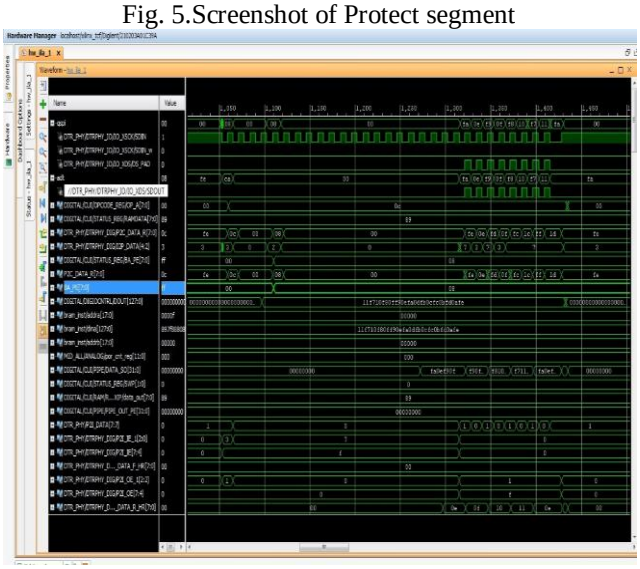

Fig. 6.Screenshot of Reading Sector fortification Register

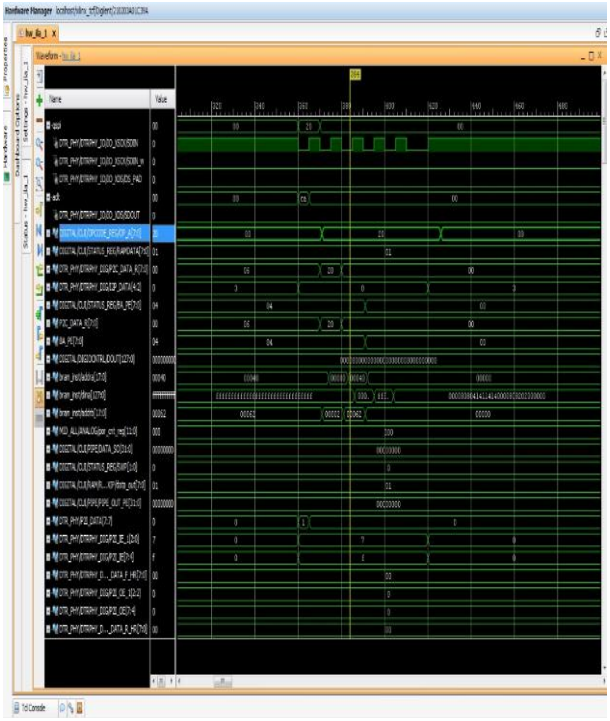

Fig. 7.Screenshot of chronological Program mode

V. CONCLUSION

In this paper, we have worked about improving the verification suite commands and designing of all functional commands which are most applicable to the consumer in the market field. Therefore, it uses information strobe as an extra pin to get high speed of response. There is availability of eight data line for communication between master microcontroller and slave device FPGA. therefore, this is more powerful device and these applications helps in the real world market field.

Acknowledgment

I express my heartfelt gratitude I express my heartfelt gratitude to Manager of power square company Mr.Sangameshwar Pujari for guiding me throughout my project and giving me such an amazing experience as an intern. I would like to thank Management, Principal and Dean of Appa Institute of Engineering & Technology, Gulbarga permitting me to carry out this project. Finally, I express my deep apperception to all staff members of our department, my parents and friends for their support and encouragement in the completion of this Project.

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