MODELLING AND SIMULATION OF UPQC FOR POWER QUALITY ENHANCEMENT AND VOLTAGE BALANCING

Akash M. Ugani[1], Mayur S. Thacker[2]
[1]PG Scholar, [2]Assistant Professor Electrical Department, HJD Institute of Technical Education and Research, Kera, Gujarat, India

ABSTRACT: Aim of this paper is to represents the design and control strategy of UPQC to get the highest benefit in terms of maximum power transfer capability and system stability. The UPQC design and controlling is shown using current source topology. FACTS devices are very effective and capable of increasing the power transfer capability of a line, as thermal limits permit, while maintaining the same degree of stability. With the improvements in current and voltage handling capabilities of the power electronic devices that have allowed for the development of Flexible AC Transmission System (FACTS), the possibility has arisen in using different types of controllers for efficient shunt and series compensation In series compensation, the FACTS Sis connected in series with the power system. It works as a controllable voltage source. Shunt compensation, power system is connected in shunt with FACTS. It works as a controllable current source. The rating of a shunt FACT device is selected in such a way so as to control the voltage equal to sending end voltage at the bus of the shunt FACT device. In this paper modelling and simulation has been done for voltage balancing of the system.

I. INTRODUCTION

In the modern times it is required to transmit power from the generating stations to the different load centres which is located at remote locations. Now for efficient and simple operation of the power system it is necessary to operate the power system different parameters like voltage, current and power flow within their operating ranges. In the modern times the different electrical equipments are interconnected with the power system and their performance has been improved using the FACTS devices. The interconnected power systems has been different advantages given as below:-

- Exploiting load diversity
- Sharing of generation reserves and
- Economy gained from the use of large efficient units without sacrificing reliability.

But there is also security problems occurs due to disturbances produced in a particular area can spread and propagate over the entire system due to that different power quality problems are occurred and sometimes also major blackouts caused by cascading outages. This thesis proposed the optimal location of shunt FACTS device in a series compensated transmission line to get the maximum possible benefit of maximum power transfer and system stability. In this the rating of a shunt FACT device has been selected in such a way that the receiving end voltage becomes equal to sending end voltage at which bus the shunt FACT device has been connected. A series capacitor is placed at the centre to get the maximum power transfer capability and compensation efficiency for the selected rating of the shunt FACTS device. In earlier times for power quality improvement there is active filter and passive filter based on current source and voltage source topology has been used.

But they have some limitation due to which their use has been reduced in the modern times. In place of these conventional devices there are different FACTS devices has been established and used in the power system. Among all the FACTS devices in the latest time one modern device UPQC has been used in very large area in the latest times because it is provide control both load current and supply voltage imperfections in the given system. The UPQC is a combination of series and shunt active power filters which are connected in cascaded connection through common DC link capacitor.

The main aim of a UPQC device is to compensate power quality issues like voltage sags, swells, unbalance, flicker, harmonics, and for load current power quality problems such as, harmonics, unbalance, reactive current and neutral current. To maintain the controlled power quality regulations some kind of compensation at all the power levels is becoming a common practice. At the distribution level UPQC is a most attractive solution to compensate several major power quality problems. It basically consists of two voltage source inverters connected back to back using a common dc bus capacitor.

II. UNIFIED POWER QUALITY CONDITIONER (UPQC)

A. Basic configuration of UPQC

UPQCs consist of combined series and shunt APFs for simultaneous compensation of voltage and current. The series APF inserts a voltage, which is added at the point of common coupling (PCC) such that the load end voltage remains unaffected by any voltage disturbance, whereas, the shunt APF is most suitable to compensate for load reactive power demand and unbalance, to eliminate the harmonics from supply current, and to regulate the common DC link voltage [2].

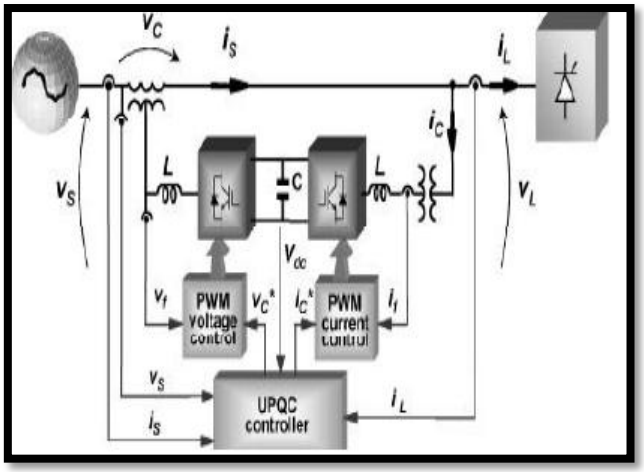

Figure 2.1- Basic configuration of the UPQC [2]

Figure 2.1 shows the basic configuration of the UPQC. The UPQC has two distinct parts:-

• Power circuit formed by series and shunt PWM converters
• UPQC controller

The series PWM converter of the UPQC behaves as a controlled voltage source, that is, it behaves as a series APF, whereas the shunt PWM converter behaves as a controlled current source, as a shunt APF. No power supply is connected at the DC link. It contains only a relatively small DC capacitor as a small energy storage element.

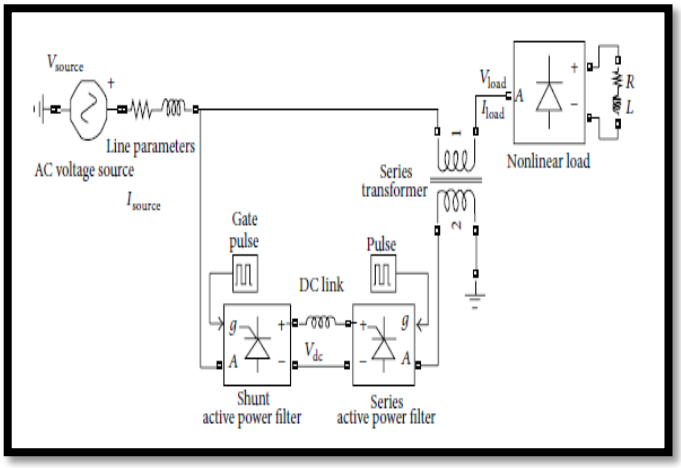

Figure 2.2: The design configuration of UPQC-CSC [3]

In this, the design configuration is right series and left shunt with the current source converter (CSC). In thesis, UPQC-CSC is designed and analysis of the results has been done. Unified power quality conditioner (UPQC) for nonlinear and voltage sensitive load has following facilities.

- It reduces the harmonics in the supply current, so that it can improve utility current quality for nonlinear loads.
- UPQC provides the VAR requirement of the load, so that the supply voltage and current are always in phase; therefore, no additional power factor correction equipment is required.
- UPQC maintains load end voltage at the rated value even in the presence of supply voltage sag.

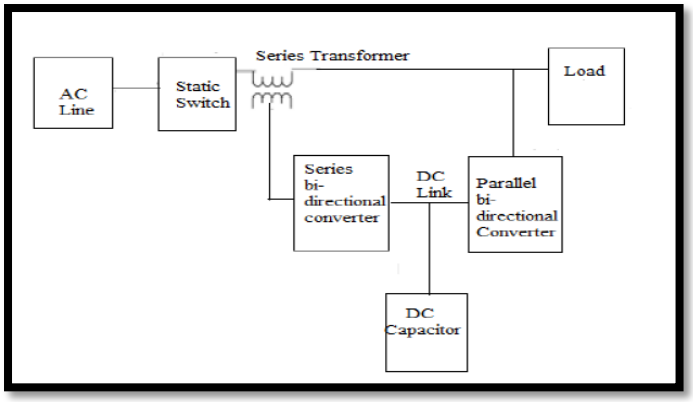

Fig 2.3- Block diagram of a UPQC

Conventional UPQC topology consists of the integration of two active power filters are connected back to back to a common dc-link bus. A simple block diagram of a typical UPQC is shown in Fig.2.3.

It can be configured either with voltage-source converters or current source converters in single phase, three-phase three wire, or three-phase four-wire configurations. The UPQC with the voltage-source converter (VSC) is most common because of its smaller size and low cost. Despite these previously mentioned advantages, the VSI topology has slow control of the converter (LC filter) output voltage and no short-circuit/over current protection. When the active rectifier inside the UPQC is used as a power factor corrector, dc bus voltage oscillations appear which makes the control of the series filter output voltage more difficult. The CSI-based UPQC has advantages of excellent current control capability, easy protection, and high reliability over VSI-based UPQC. The main drawback of the CSI-based UPQC has been so far the lack of proper switching devices and large dc-side filter. The new insulated-gate bipolar transistors (IGBTs) with reverse blocking capability are being launched in the markets which are suitable for the CSI-based UPQC. With the use of SMES coils, the size and losses can be reduced considerably. A configuration of UPQC using two current-source converters connected back to back through a large dc-link reactor is shown in fig 2.4.

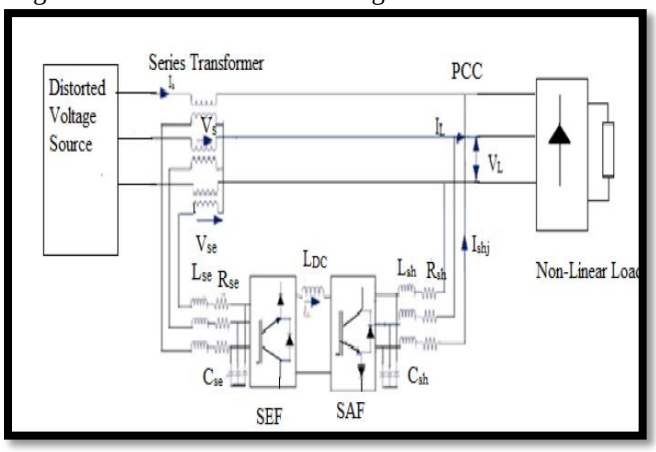

Fig 2.4 UPQC topology using current-source converters

The performance of the UPQC mainly depends on how accurately and quickly the reference signals are derived. After efficient extraction of the distorted signal, a suitable dc-link current regulator is used to derive the actual reference signals. A dc current regulator will serve as power-loss compensation in the filter circuits, which will take place through the activation of a shunt unit. This regulator will maintain dc-link current constant for stable operation of the filter. In the conventional PI controller, the error between the actual dc-link current and a reference value, which is generally slightly greater than the peak of the dc-link value, is fed to the PI controller. The output of the PI controller is added suitably for the generation of a reference template [5].

III. MATLAB DESIGN OF UPQC AND CONNECTION WITH THREE PHASE SYSTEM

From the above simulation results we can say that the three phase system without UPQC device generates distorted voltage, current and power. The value of these output quantities does not remains constant. So we have to interconnect the UPQC device with this three phase compensated network as shown in the fig below. As shown in the fig below the UPQC device is connected between source side and load side. The design of UPQC includes the VSC at input side and one VSC at output side. After the interconnection of UPQC system with three phase compensated network the output value of voltage, current and power becomes constant and pure sinusoidal.

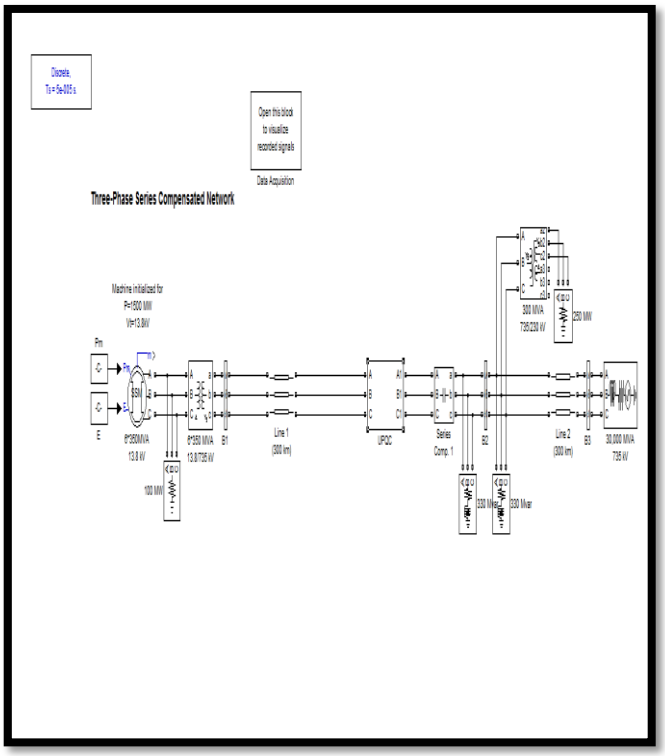

Fig 3.1- Three phase compensated network connect with UPQC system

Now the Subsystem of UPQC is shown in the fig below with their design configuration. As shown in the fig below design of UPQC includes two VSC at input and output side, which is connected through common D.C. link capacitor. The fig design configuration also includes the control circuit of gate triggering circuit for the VSC Thyristors triggering for the constant and pure sinusoidal output.

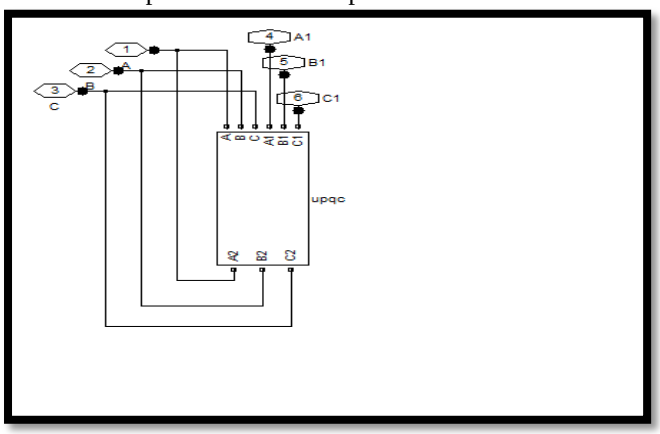

Fig 3.2-UPQC Subsystem

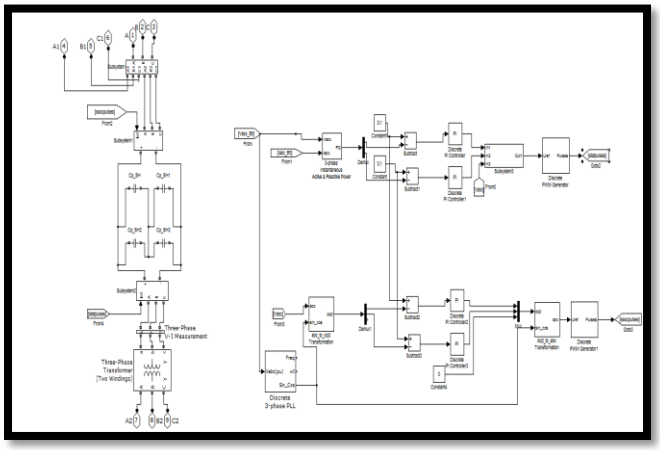

Fig 3.3-Configuration of UPQC System

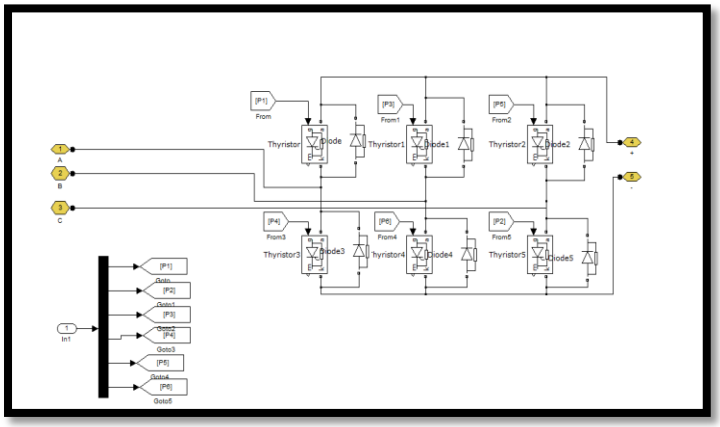

Fig 3.4- VSC configuration in UPQC design

The design configuration of VSC used in UPQC system is shown in the fig above. As shown in the fig above we can say that 6 Thyristors based configuration design used in the VSC at input and output side of UPQC subsystem. The gate signal for Thyristors triggering in this VSC in generated from the UPQC control strategy subsystem which shown in the fig below:-

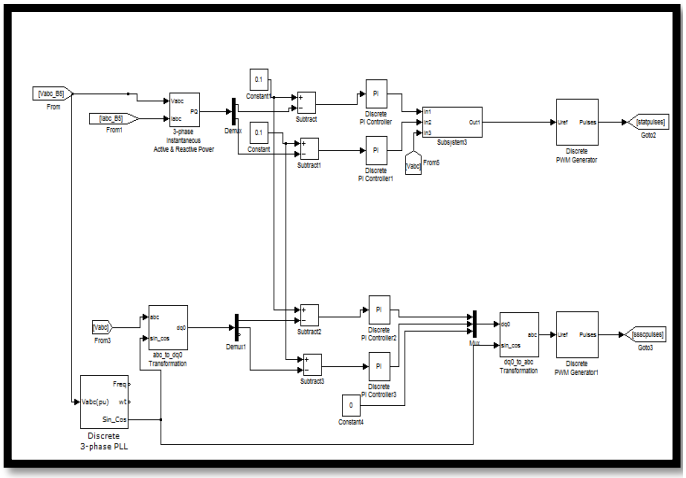

Fig 3.5-Control Strategy of UPQC System

In the control strategy of VSC at input side the voltage and current at output side is multiplied and value of power has been calculated. Than its value is compare with the constant value or add and subtract with constant value than give to PI controller for compare with the input side three phase voltages. The output of PI controller is given to PWM generator to compare with carrier frequency for pulses generation for VSC gate triggering at input side. Same as the above the control strategy is apply for output side VSC but there is PLL (Phase lock loop) system is provided to generate the constant frequency value phase which gives the phase value constant, and dqo transformation is done is done of the 3 phase system for easiness of calculation and compare with the PI controller. The output of PI controller is inverse into 3 phase voltage Vabc which is given to PWM generator for comparison of carrier signal and output of PI controller. The difference between these two signal provide pulses for gate triggering of Thyristors of VSC at output side which generates constant output value of voltage, current and power with pure sinusoidal waveform.

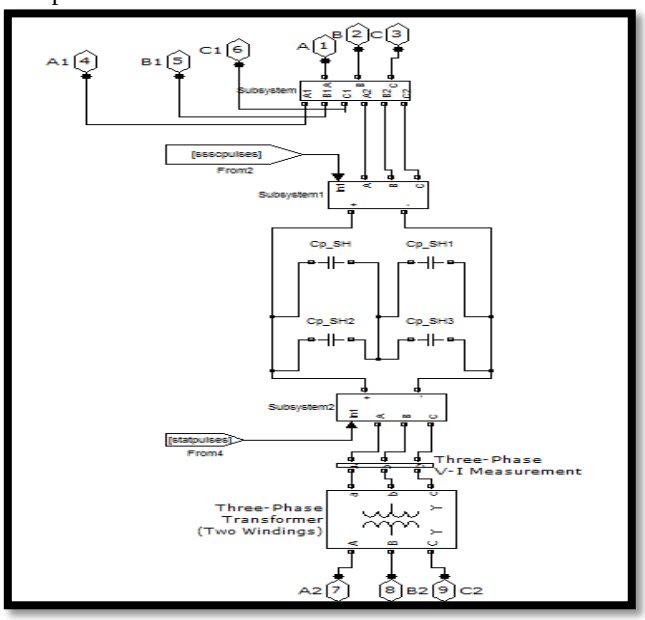

Fig 3.6-Controlling Subsystem

Simulation Results:-

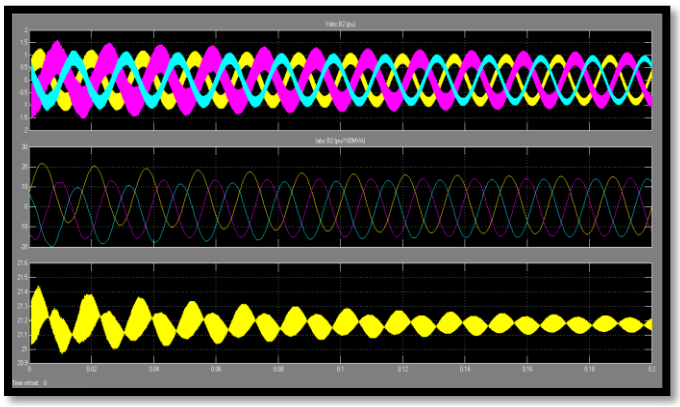

Fig 3.7-Voltage, Current & Power at Input Side

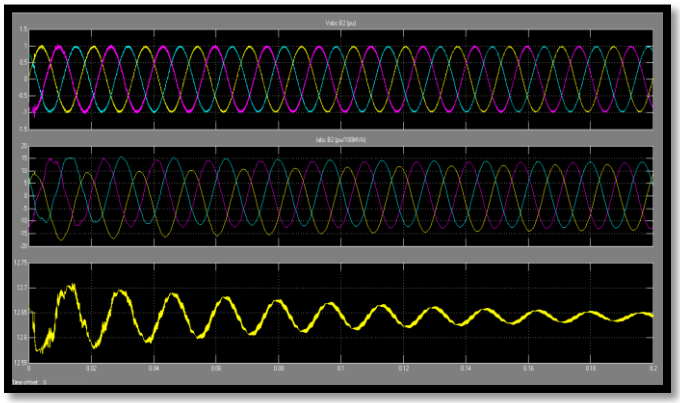

Fig 3.8-Voltage, Current & Power at Load Side (Case-I)

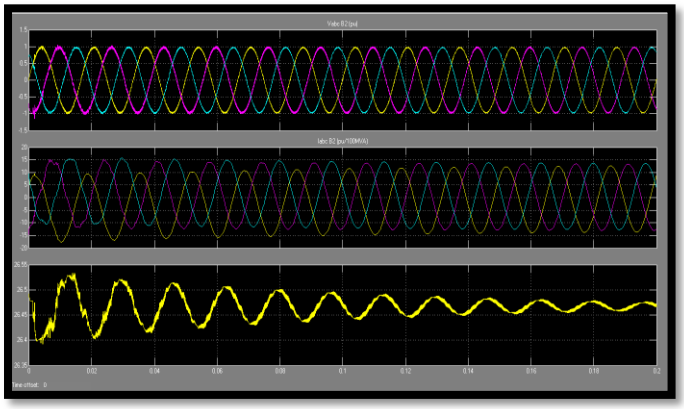

Fig 3.9-Voltage, Current & Power at Load Side (Case-II)

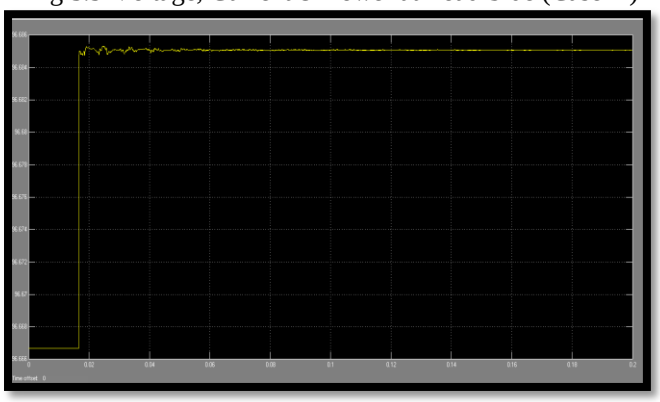

Fig 3.10-Difference in voltage at load side and input side

Voltage Balancing using Diode Clamped Multilevel Inverter

The diode-clamped multilevel inverter uses capacitors in series to divide up the dc bus voltage into a set of voltage levels. To produce m levels of the phase voltage, an m-level diode-clamp inverter needs m-1 capacitors on the dc bus. A single-phase five-level diode-clamped inverter, which can produce a nine-level phase to phase voltage waveform, is shown in Fig. 3.11.

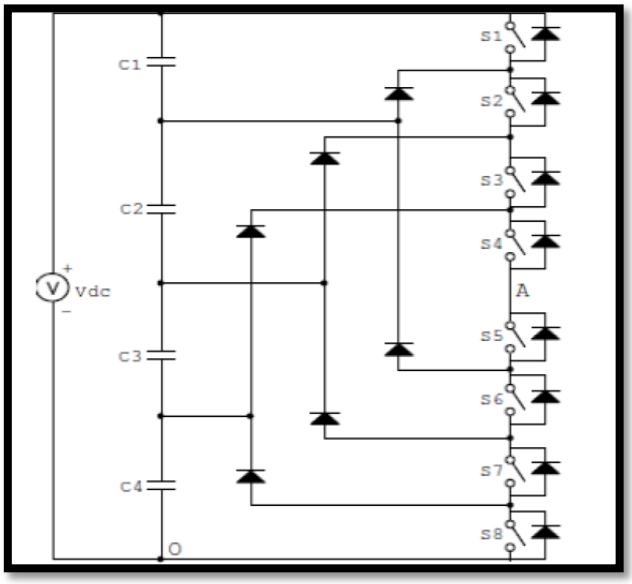

Figure 3.11- A single-phase five-level diode-clamped inverter

The dc bus consists of four capacitors, i.e., C1, C2, C3, and C4. For a dc bus voltage Vdc, the voltage across each capacitor is Vdc/4, and each device voltage stress will be limited to one capacitor voltage level, Vdc/4, through clamping diodes. DCMI output voltage synthesis is relatively straightforward. To explain how the staircase voltage is synthesized, point O is considered as the output phase voltage reference point. Using the five-level inverter shown in Fig.5.21, there are five switch combinations to generate five level voltages across A and O.

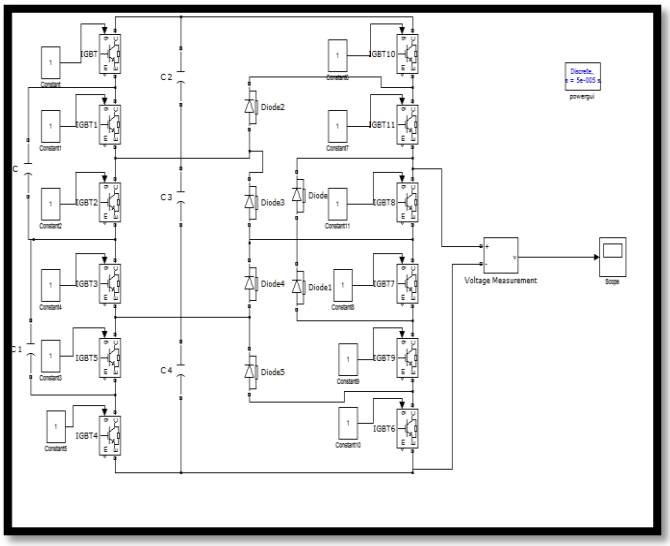

Fig 3.12-Matlab-Simulink model of multilevel inverter

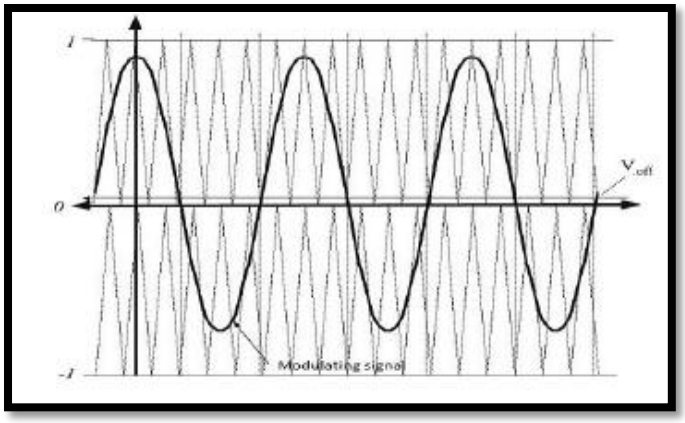

Fig 3.13-Offset addition PWM

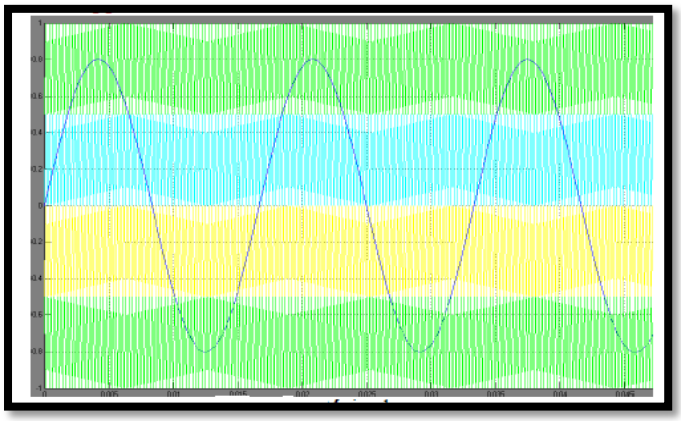

Fig 3.14-PWM signals

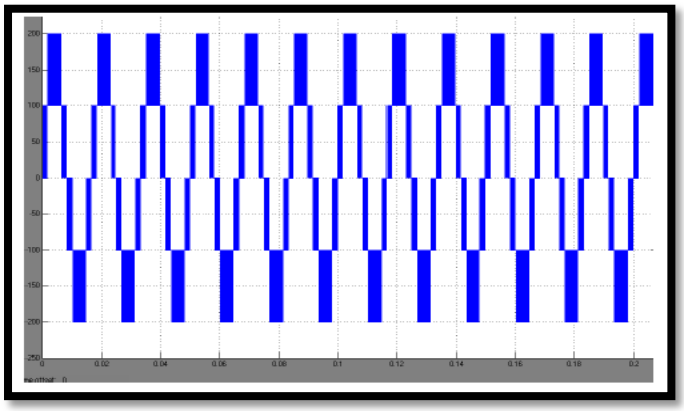

Fig 3.15-Five level output without filter

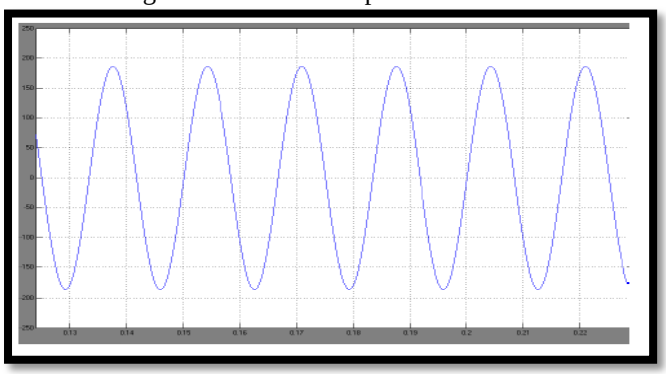

Fig 3.16-Output with filter

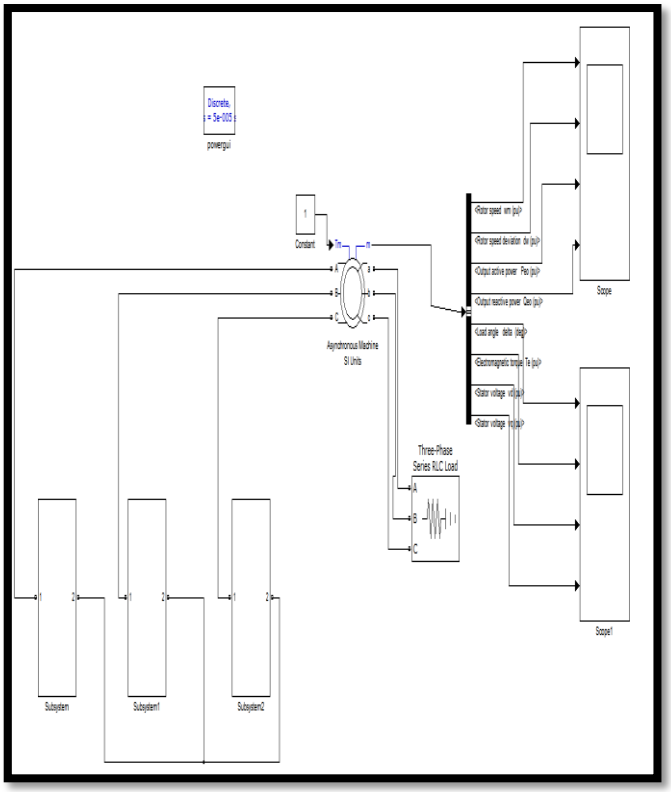

Fig 3.17-Three Phase converter with Synchronous Machine

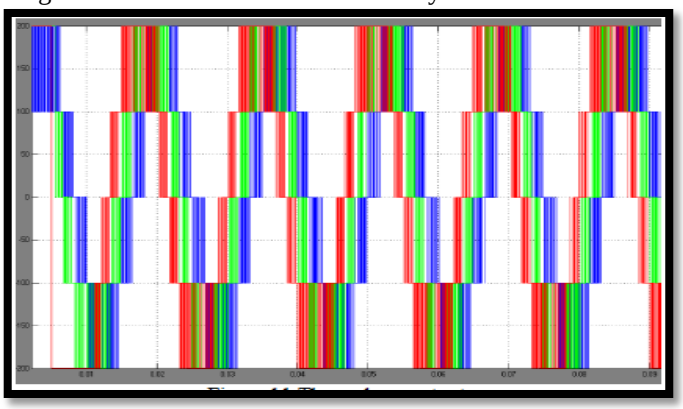

Fig 3.18-Three phase output

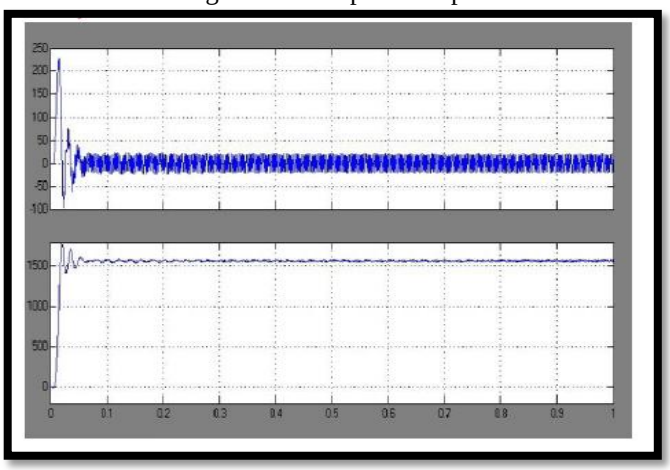

Fig 3.19-Electromagnetic Torque and Speed curves of synchronous machine

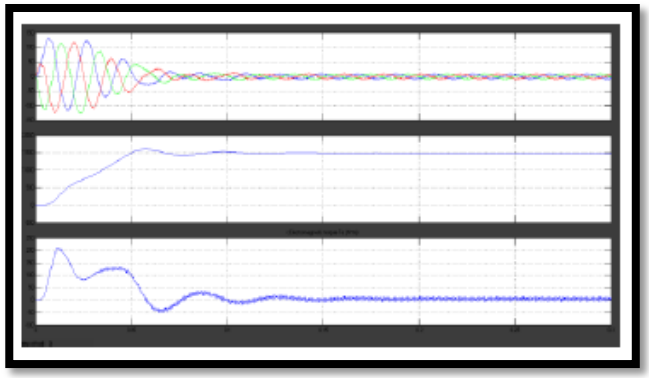

Fig 3.20-Voltage balancing of synchronous machine

IV. CONCLUSION & FUTURE SCOPE

From the simulation results we can say that after the application of UPQC in three phase system the distortion in voltage, current and power has been reduced. The power quality is improved using the control strategy of UPQC in three phase compensated system. Improve the simulation results of the three phase system and voltage balancing is done for different conditions. Compare the performance of UPQC with other FACTS devices like STATCOM and SVC etc.

REFERENCES

Papers

[1] Jan Verveckken, Fernando Silva, Dionísio Barros, Johan Driesen, "Direct Power Control of Series Converter of Unified Power-Flow Controller With Three-Level Neutral Point Clamped Converter", IEEE TRANSACTIONS ON POWER DELIVERY, VOL. 27, NO. 4, OCTOBER 2012.

[2] Mr. Shaktisinh N. Gohil, prof. M. V. Makwana, "A Comparative Analysis of UPQC for Power Quality Improvement", Journal of information, knowledge and research in electrical engineering, ISSN: 0975 – 6736| Nov 12 to oct 13 | volume – 02, issue – 02.

[3] Rajasekaran Dharmalingam,Subhransu Sekhar Dash, Karthikrajan Senthilnathan, Arun BhaskarMayilvaganan, and Subramani Chinna muthu, "Power Quality Improvement by Unified Power Quality Conditioner Based on CSC Topology Using Synchronous Reference Frame Theory", Hindawi Publishing Corporation the Scientific World Journal Volume 2014, Article ID 391975.

[4] G.Ganesh, Ch.Sampath Kumar, D.KumaraSwamy, "Voltage Sag and Swell Compensation using UPQC-S Technique", International Journal of Engineering Inventions e-ISSN: 2278-7461, Volume 3, Issue 2 (September 2013) .

[5] N.Ramchandra, V.SumaDeepthi, "Comparison of Different Controllers on Unified Power Quality Conditioner", IOSR Journal of Engineering (IOSRJEN) e-ISSN: 2250-3021, Volume 2, Issue 9 (September 2012.

[6] Manoj D. Kharad, Naveen Kumar, "Modelling and

Simulation of Unified Power Quality Conditioner (UPQC)", International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249 – 8958, Volume-3 Issue-6, August 2014.

[7] Sukhjinder Singh, Mukul Chankaya, "Enhancement of power Quality by UPQC: A Review", International Journal of Engineering and Technical Research (IJETR) ISSN: 2321-0869, Volume-3, Issue-2, February 2015.

[8] G.VIDHYA KRISHNAN, SU.DHIVYA, "Intelligent Technique for Unified Power Quality Conditioner to Enhance Power Quality", International Research Journal of Infinite Innovations in Engineering and Technology ISSN (Online): 2349-2287, ISSN (Print): 2349-2279 Volume 1 Issue 4 December 2014.

