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ZSI BASED DVR FOR POWER QUALITY ENHANCEMENT IN POWER DISTRIBUTION SYSTEM

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Abstract: The voltage events mostly voltage sags and voltage swells represent the most common, frequent and important power quality disturbances in today's complex power system. Dynamic Voltage Restorer (DVR) is one of the custom power device used to mitigate the supply voltage quality problems in terms of voltage sags and swells in the distribution system. It consists of an energy storage unit, a voltage source inverter, a filter, a coupling transformer and the control system. This paper presents six leg Z-source inverter based Dynamic Voltage Restorer (ZSI-DVR) for mitigation of voltage events such as voltage sags and swells with sudden addition or removal of the linear and nonlinear loads. The SRF control technique is used to generate the reference signals and control the operation of the ZSI-DVR. The response of ZSI-DVR for mitigation of voltage sags and swells are investigated using MATLAB/SIMULINK environment.

Keywords: Voltage sag; voltage swell; voltage source inverter; Z-source inverter

I. INTRODUCTION

In recent years, many researchers have given their focus on power quality. Discussing power quality is a complex issue and is measured in terms of such things as line interruptions, voltage sags, voltage swells, flickers, harmonics, phase unbalance and distortion. However, among all disturbances, the voltage sags and voltage swells represents the most common, frequent and important power quality problems in today's power system [1]. Voltage sags are commonly known phenomenon in supply systems. A voltage sag (or dip) is a disturbance where the rms value of the line voltage is reduced for a period ranging from one-half cycle of the voltage to 500 ms. A typical cause of voltage sags is the direct line start of large induction motors that normally draw 5 to 7 times their rated currents during start-up. Short circuits in the other branches of the supply are also a common origin of voltage sags. The sudden addition of a larger load and also loose or defective wiring can cause voltage sags [1].Voltage swell is defined as an increase in root mean square voltage from 110% to 180% of the normal voltage at the power frequency for the duration of 0.5 cycles of 1 minute. A voltage swell can occur due to a fault, switching off a large load and switching to a large capacitor bank [2, 3].Voltage Swells are characterized by their magnitude and duration [4]. There, are many different solutions have been proposed to eliminate voltage sags and swells, conventionally the passive filters are used for power quality issues. But nowadays power electronics based on new kinds of emerging custom power devices such as Dynamic Voltage Restorer, Distributed Static Compensator and Unified Power Quality Conditioner have been more popular because they offer the advantages of flexibility and high performance to improve the controllability of power distribution network. DVR is the key component used in the distribution system to compensate long duration voltage events such as voltage sags and voltage swells [5-7]. Generally, the DVRs consists of voltage source inverter based DVR (VSI-DVR), current source inverter based DVR (CSI-DVR) [8] and impedance source inverter based DVR (ZSI- DVR) [9-11]. The main disadvantage of VSI-DVR is their buck (step-down) type output voltage characteristics thereby the maximum output voltage is limited by DC link voltage. The upper and lower devices of each leg cannot be gated on simultaneously, so a shoot-through would occur and destroy the devices. The shoot-through is a forbidden switching state for the VSI. The CSI-DVR is a boost type so its output voltage has to be greater than the DC voltage. For the application where a wide voltage range is desirable an additional DC-AC boost converter is needed. The additional power conversion stages increase system cost and lowers efficiency. At least one of the upper devices and one of the lower devices have to be gated on and maintain on at any time. Otherwise, an open circuit of the DC inductor would occur and destroys the devices. ZSI is a new type of converter in power conversion which has unique features that can overcome the limitations of VSI and CSI. The unique feature of the ZSI is that the output AC voltage can be any value between zero and infinity regardless of the DC voltage. That is, the ZSI is a buck-boost inverter that has a wide range of obtainable voltage. Unlike a VSI and CSI, the shoot-through state is not harmful and actually has been utilized in ZSI [12-14].In this paper ZSI-DVR are discussed and simulated using MATLAB\SIMULINK platform for mitigation of commonly occur voltage events such as voltage sags and voltage swells under linear and nonlinear load condition.

II. CONFIGURATION OF DYNAMIC VOLTAGE RESTORER (DVR)

DVR can be implemented by three-phase Z-source inverters as shown in Fig.1. The structure of voltage sag/swell compensator contains a bank of three-single phase voltage source inverters. Each voltage source inverter unit is connected to the network through three-phase an isolating transformer which provides isolation between the converters. Further, it also provides the DC storage capacitor from being shorted through switches in different converters. It is to be noted that the capacitor must be pre-charged to sufficient high value in order to obtain satisfactory tracking performance. However, increasing the capacitor voltage increases the losses in the system. Lf represents the inductance of each transformer as well as an additional interfacing inductance. It has been used to filter out high-frequency components of compensating voltages. It also controls the switching frequency of the inverter.

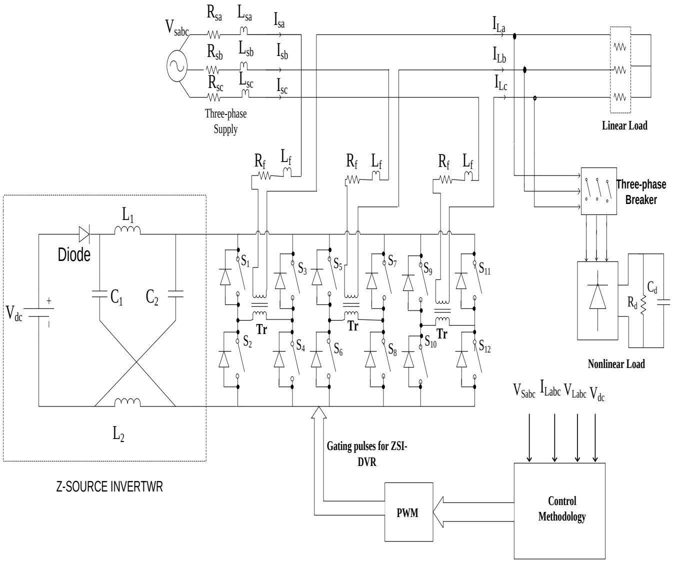

Fig.1 Schematic diagram of ZSI-DVR

III. OPERATING PRINCIPLE OF Z-SOURCE INVERTER

ZSIs are recently proposed inverter topologies that can perform both buck/boost function as a single unit. The VSI and CSI cannot provide such feature. The ZSI overcomes the above-mentioned conceptual and theoretical barriers and limitations of the VSI and CSI and provides a novel power conversion concept. The general configuration of three-phase ZSI is shown in Fig. 2. It consists of split inductors L1 and L2 and capacitors C1 and C2. Which, are composed to form a unique impedance network to avoid a short circuit when the devices are in shoot-through state.

The ZSI has three operating modes: (i) normal mode (ii) zero-state mode (iii) shoot-through mode.

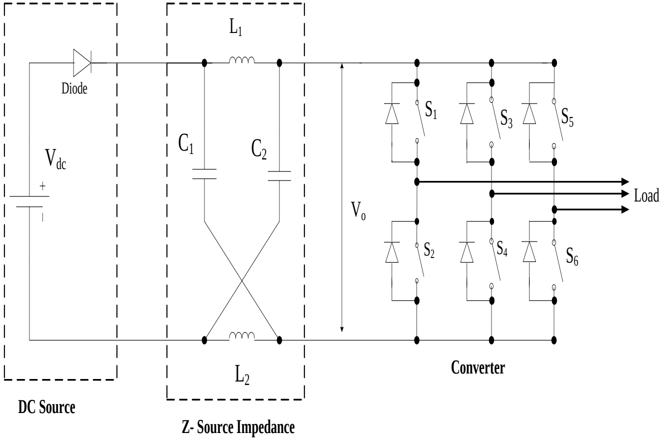

Fig.2 Basic configuration of Z-Source Inverter

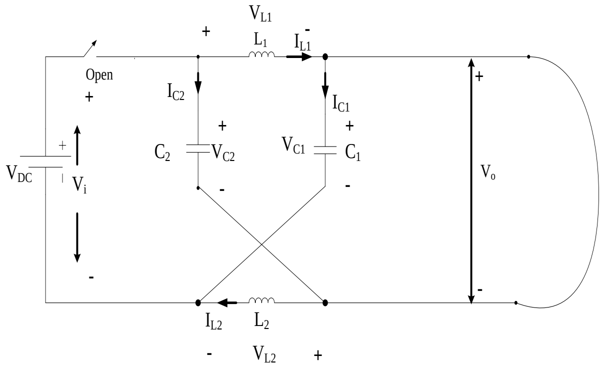

Fig.3 Active and Zero state of Z-Source Inverter

The Fig. 3 shows active and zero states of ZSI. In these states diode is forward biased at the DC-link side, so it conducts. The voltage across the inductors is

$$\left.\begin{aligned} V_L &= V_{DC} - V_C \\ V_C &= V_{DC} - V_L \end{aligned}\right\} \qquad (1)$$

And Vi =VDC. The input voltage across the converter during active and zero states during interval t1 is

$$\left.\begin{aligned} V_L &= V_{DC} - V_C \\ V_C &= V_{DC} - V_L \end{aligned}\right\} \qquad (2)$$

The mean voltage of the inductor over one switching interval t should be zero in steady state.

$$\left(\frac{V_C}{V_{DC}}\right) = \left(\frac{t_1}{t_1+t_0}\right) \qquad (3)$$

Fig. 4 shows the shoot-through switching state of the ZSI where two switches of three legs turned on simultaneously. In this state, the diode (D) at input side is reverse bias and capacitors C1 and C2 charges the inductors L1 and L2. The DC-link voltage of the inverter is zero in shoot-through interval t0. The mean DC-link voltage across converter bridge during one switching cycle.

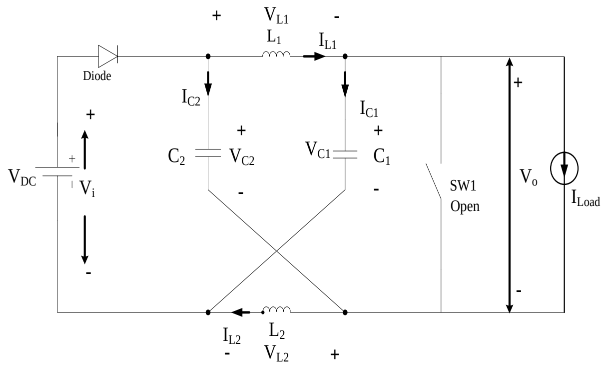

Fig.4 Shoot-Through state of Z-Source Inverter

$$V_i = V_{DC}\left(\frac{t_1}{t_1-t_0}\right) \qquad (4)$$

The peak DC-link Voltage across the inverter bridge is

$$V_0 = B_O V_{DC} \qquad (5)$$

Where $B_0 = \left(\frac{t}{t_1 - t_0}\right) \ge 1$ is the boost factor resulting from the shoot-through state.

The output peak phase voltage from the inverter can be expressed as

$$V_{AC} = M_i \left(\frac{V_0}{2}\right) \qquad (6)$$

Where M_i is the modulation index.

The voltage across the capacitors can be expressed as

$$V_C = \left(\frac{1 - {t_0}/{t}}{1 - {2t_0}/{t}}\right) V_{DC} \qquad (7)$$

IV. SRF CONTROL TECHNIQUE

Fig. 5 shows the control strategy of the series connected DVR. The voltages at the PCC (V_s) are converted to rotating reference frame using the abc-dqo conversion using the Parks transformation.

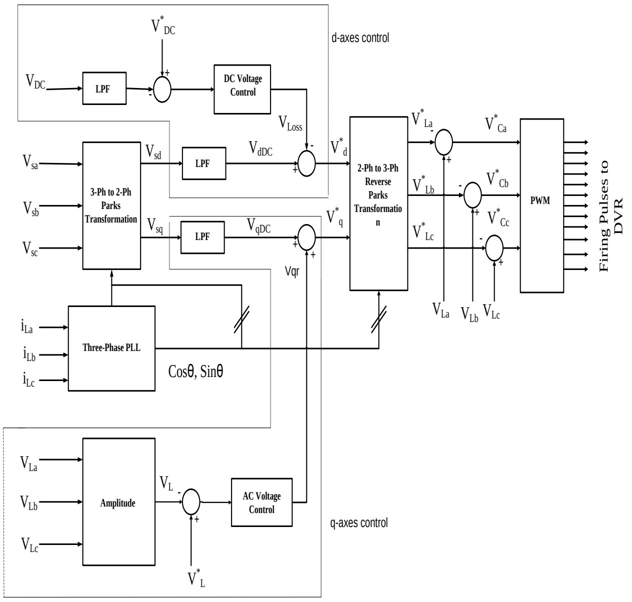

Fig.5 Block diagram of SRF control technique

$$\begin{bmatrix} V_{Sd} \\ V_{sq} \\ V_{so} \end{bmatrix} = (2/3) \begin{bmatrix} \cos\theta & \text{-}\sin\theta & 0.5 \\ \cos\left(\theta - 120^0\right) & \text{-}\sin\left(\theta - 120^0\right) & 0.5 \\ \cos\left(\theta + 120^0\right) & \text{-}\sin\left(\theta + 120^0\right) & 0.5 \end{bmatrix} \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} \qquad (8)$$

Low pass filters (LPFs) are used to eliminate the harmonics and oscillatory components of voltages. The components of voltages of direct and quadratutre axes are

$$V_{sd} = V_{dDC} + V_{dAC} \qquad (9)$$

$$V_{sq} = V_{qDC} + V_{qAC} \qquad (10)$$

In order to maintain the DC bus voltage of the self-supported capacitor, a PI controller is used at the DC bus voltage of the DVR and output is considered as the voltage loss (V_{Loss}) for meeting its losses.

$$V_{Loss(n)} = V_{Loss(n-1)} + K_{p1}\left(V_{de(n)} - V_{de(n-1)}\right) + K_{i1} V_{de(n)} \quad (11)$$

Where $V_{de(n)} = V_{DC}^{*} - V_{DC(n)}$ is the error between the reference DC voltage (V_{DC}^{*}) and sensed DC voltage (V_{DC}) at the nth sampling instant. K_{PI} and K_{i1} are the proportional and the integral gains of the DC bus voltage PI controller. Therefore, reference direct axes (d-axes) load voltage is

$$V_d^{*} = V_{dDC} - V_{Loss} \qquad (12)$$

The amplitude of the load terminal voltage (V_L) is controlled by its reference voltage (V_L^{*}) using another PI controller. The output of PI controller is considered as the reactive component of voltage (V_{qr}) for voltage regulation of load terminal voltage.

$$V_{qr(n)} = V_{qr(n-1)} + K_{p2}\left(V_{te(n)} - V_{te(n-1)}\right) + K_{i2} V_{te(n)} \quad (13)$$

Where $V_{te(n)} = V_L^{*} - V_{L(n)}$ denotes the error between the reference load terminal voltage (V_L^{*}) and actual load terminal voltage ($V_{L(n)}$) amplitudes at the nth sampling instant. K_{p2} and K_{i2} are the proportional and the integral gains of the DC bus voltage PI controller. The reference quadrature axes (q-axes) voltage is

$$V_q^{*} = V_{qDC} + V_{qr}$$

(14)

The reference load voltages ($V_{La}^{*}, V_{Lb}^{*}, V_{Lc}^{*}$) in abc frame are obtained from the reverse Parks transformation as in equation (15)

$$\begin{bmatrix} V_{La}^{*} \\ V_{Lb}^{*} \\ V_{Lc}^{*} \end{bmatrix} = \sqrt{\left({2}/{3}\right)} \left\{ \begin{matrix} \cos(\omega t) & \sin(\omega t) \\ \cos\left(\omega t\text{-}\left({2\pi}/{3}\right)\right) & \sin\left(\omega t\text{-}\left({2\pi}/{3}\right)\right) \\ \cos\left(\omega t\text{+}\left({2\pi}/{3}\right)\right) & \sin\left(\omega t\text{+}\left({2\pi}/{3}\right)\right) \end{matrix} \right\} \begin{bmatrix} V_d^{*} \\ V_q^{*} \end{bmatrix} \qquad (15)$$

The errors between the sensed load voltages (V_{La}, V_{Lb}, V_{Lc}) and reference load voltages are used in the PWM controller to generate gate pulses for the VSC of the DVR.

V. SIMULATION OF DVR

Fig. 1 show the three Z-source inverter configurations of the test system used to carry out the simulation with the associated control technique. This ZSI-DVR model is simulated under linear and nonlinear load condition with simulation period 0.25 s.

VI. SIMULATION RESULTS AND DISCUSSION

In this section, simulation results of three different inverter topologies based on DVR for mitigation of voltage sag and swell under nonlinear load condition is presented. Load1 is considered as fixed resistive load (R-load) and load2 is considered as a nonlinear load. The nonlinear load is realized by three-phase diode-rectifier with R-C load. A three-phase breaker is used to control the connection of a nonlinear load to the distribution network. Initially, both the loads are connected to the network, but after a certain period of time load2 are switched on and off by opening the breaker. Due to the sudden change of the heavy load, voltage sag and swell occurs in the source voltage.

A. Voltage sag and swell mitigation by ZSI-DVR under linear load

Figs. 6(a) - 6(d) depicts the simulation results of ZSI-DVR with a nonlinear load. Because of sudden load variation voltage sag and voltage swell occurs in the distribution system. A three-phase balanced voltage sag of magnitude 19% of the normal voltage which starts at t=0.01s and ends at t=0.05s and three-phase voltage swell of magnitude 18% of the normal voltage from 0.15-0.2s. Then the source voltage signal recovers to its normal levels. For balanced voltage sag/swell, the supply voltage signal before compensation, the compensation voltage, the load voltage after voltage sag/swell compensation and variation of DC link voltage are depicted in Figs. 6a to d. Figs. 6b and c shows the capability of the ZSI-DVR in compensation of voltage sag and swell is when ZSI-DVR is connected to the distribution system. DVR does not produce any voltage during normal condition, but during voltage sag and swell condition, it generates voltage with required magnitude and polarity and injects to the system and keeps the load voltage at the desired level as in the normal operating condition.

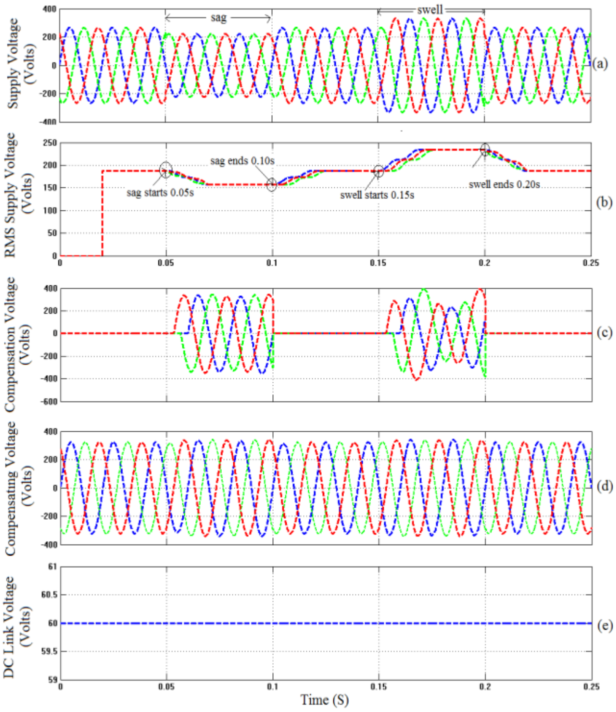

Fig.7 Simulation results of ZSI-DVR (a) voltage sag (b) Injected voltage of ZSI-DVR (c) Load voltage and (d) DC-link Voltage

B. Voltage sag and swell mitigation by ZSI-DVR under nonlinear load

Figs. 7(a) - 7(d) depicts the simulation results of ZSI-DVR with a nonlinear load. Because of sudden load variation voltage sag and voltage swell occurs in the distribution system. A three-phase balanced voltage sag of magnitude 25% of the normal voltage which starts at t=0.01s and ends at t=0.05s and three-phase voltage swell of magnitude 14% of the normal voltage from 0.15-0.2s. Then the source voltage signal recovers to its normal levels. For balanced voltage sag/swell, the supply voltage signal before compensation, the compensation voltage, the load voltage after voltage sag/swell compensation and variation of DC link voltage are depicted in Figs. 7a to d. Figs. 7b and c shows the capability of the ZSI-DVR in compensation of voltage sag and swell is when ZSI-DVR is connected to the distribution system. DVR does not produce any voltage during normal condition, but during voltage sag and swell condition, it generates voltage with required magnitude and polarity and injects to the system and keeps the load voltage at the desired level as in the normal operating condition.

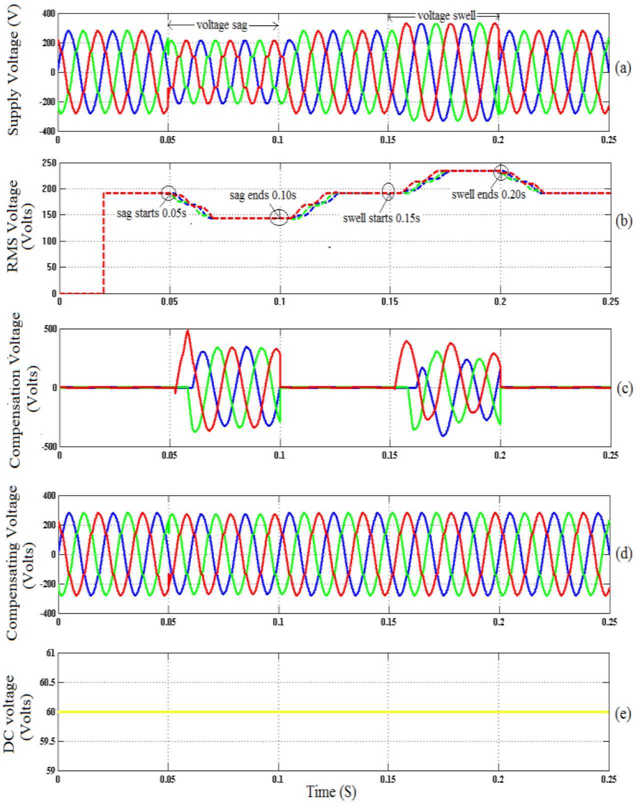

Fig.8 Simulation results of ZSI-DVR (a) voltage sag (b) Injected voltage of ZSI-DVR (c) Load voltage and (d) DC-link Voltage

The voltage sag and swell mitigation capacity of the ZSI-DVR depends very much on the maximum voltage injection capability of the device during voltage sag and swell period. It can be observed from the Fig. 9 that ZSI-DVR produce and injects a higher amount of compensation voltage in linear load compared to nonlinear load during voltage sag and voltage swell condition.

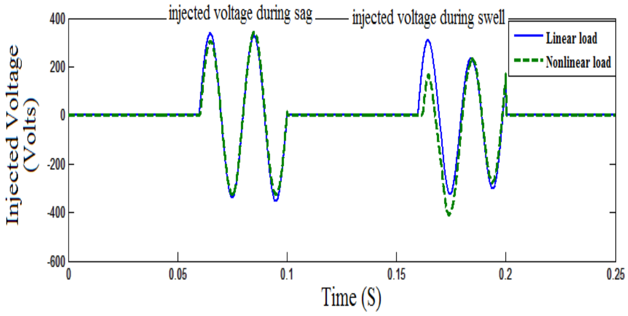

Fig.9 Injected voltage under liner and nonlinear load

VII. CONCLUSION

In this paper ZSI-DVR are tested using MATLAB/SIMULINK platform under linear and nonlinear load condition for mitigation of supply voltage disturbances like voltage sags and swells in a distribution system. It is found that ZSI-DVR shows a superior performance in linear load compared to nonlinear load to mitigate the most significant power quality events such as voltage sags and swells in the supply voltage.

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