International Journal For Technological Research In Engineering
Volume 3, Issue 10, June-2016 *ISSN (Online): 2347 - 4718*

A LOW POWER CMOS REALIZATION OF CONSTANT DELAY LOGIC STYLE

G. Divya Praneetha[1], P. Parvathi[2]
[1,2]Assistant Professor, Dept of ECE, G. Pulla Reddy Engineering College, Kurnool, A.P, India

Abstract: A constant delay (CD) logic vogue is projected during this paper, targeting at full-custom high-speed applications. The CD characteristic of this logic vogue no matter the logic kind makes it appropriate in implementing difficult logic expressions like addition. CD logic exhibits a novel characteristic wherever the output is pre-evaluated before the inputs from the preceding stage is prepared. This feature offers performance advantage over static and dynamic domino logic designs during a single-cycle period circuit block. many style issues together with temporal arrangement window breadth adjustment and clock distribution area unit mentioned. victimisation 65-nm all-purpose CMOS technology, the projected logic demonstrates a mean speed of ninety four and fifty six over static and dynamic domino logic, severally, in 5 completely different logic gates. Simulation results of 8-bit ripple carry adders show that CD logic is thirty ninth and twenty third quicker than the static and dynamic-based adders, severally. CD logic additionally demonstrates thirty ninth speed and 64% (22%) energy-delay product (EDP) reduction from static logic at 100% (10%) knowledge activity in 32-bit carry lookahead adders. For 8-bit Wallace tree multiplier factor, CD logic achieves the same speed with a minimum of five hundredth EDP electronic knowledge processing EDP automatic data processing (ADP) reduction across all data activities.

I. INTRODUCTION

High-Performance energy-efficient logic vogue has always been a preferred analysis topic within the field of VLSI circuits thanks to the continual demands of ever increasing circuit in operation frequency. The invention of the dynamic domino logic [Fig. 1(a)] within the Nineteen Eighties is one among the answers to the present request, because it permits designers to implement superior circuit blocks, i.e., arithmetic logic units, at Associate in Nursing in operation frequency that ancient static and pass semiconductor unit CMOS logic designs realize troublesome to realize . However, the performance sweetening comes with many prices, as well as a reduced noise margin, a tangle of charge-sharing, and better power issipation because of a better information activity. many variations of the dynamic domino logic, specifically NP domino (NORA domino) , zipper domino , and data-driven dynamic logic (D3L) are planned however they're ne'er widespread within the VLSI business .Compound domino logic (CDL), wherever dynamic and static gates alternating between one another, has become the foremost logic style in superior circuit blocks, i.e., 64-bit adder, in fashionable CPUs. During this style, the output electrical converter is replaced with a additional complicated inverting static gate, i.e., NAND, such the monotonicity demand is glad whereas conducting complicated logic operations while not wasting the one electrical converter delay furthermore, all the dynamic stages except the primary stage will be footless in CDL. This implementation, however, comes at the expense of: 1) exaggerated power consumption because of the potential direct path current throughout the precharge period; and 2) a reduced noise margin as a result of unprotected dynamic domino logic's outputs.

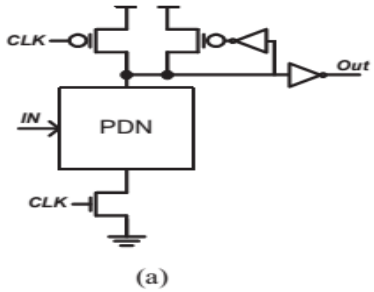

Fig. 1. Schematic of (a)dynamic domino logic with a footer transistor

II. EVOLUTION OF CD LOGIC

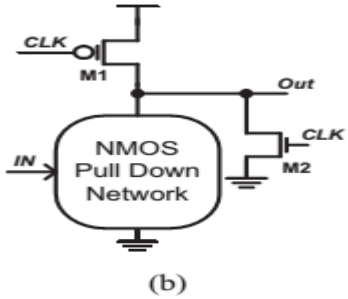

Fig.1.(b) FTL.

A.FTL Logic

FTL logic [Fig. 1(b)] in CMOS technology was 1st introduced in [16] and [17]. Its basic operation is as follows: once CLK is high, the predischarge amount begins and Out is force right down to GND through money supply. once CLK becomes low, M1 is on, M2 is off, and therefore the gate enters the analysis amount. If inputs (IN) area unit logic "1," Out enters the competition mode wherever money supply and transistors within the nMOS pull-down network (PDN) area unit conducting current at the same time. If PDN is off, then the output quickly rises to logic "1." during this

case, FTL's vital path is usually one pMOS semiconductor

B. CD Logic

To mitigate the above-named issues, CD logic is projected with a schematic shown in Fig. 3(a). Temporal arrangement block (TB) creates associate degree adjustable window amount to scale back the static power dissipation. Logic Block (LB) helps to scale back the unwanted flaw and additionally makes cascading CD logic possible. A buffer enforced in CD logic with schematics of TB and pound is shown in Fig. 3(b).

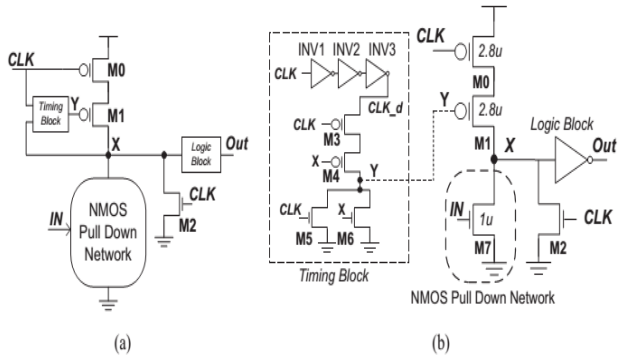

Fig. 3. CD logic (a) block diagram and (b) buffer.

1.CD Logic Operation:

Fig. four depicts the corresponding CD logic temporal arrangement diagram and flow sheet. For simplicity, we tend to assume that IN come back from dynamic domino logic gates. once CLK is high, CD logic predischarges each X and Y to GND. once CLK is low, CD logic enters the analysis amount and 3 eventualities will take place: specifically, the competition, C–Q delay, and D–Q delay modes. The competition mode happens once CLK is low whereas IN stay at logic "1." during this case, X is at a nonzero voltage level that causes intent on expertise a brief fault. The period of this fault is decided by the native window dimension,that is decided by the delay between CLK and CLK_d. once CLK_d becomes high, and if X remains low, then Y rises to logic "1," and turns off money supply. Therefore the competition amount is over, and therefore the temporary fault at Out is eliminated. C–Q delay mode takes places once IN create a transition from high to low before CLK becomes low. once CLK becomes low, X rises to logic "1" and Y remains at logic "0" for the complete analysis cycle. The delay is measured by the falling fringe of each CLK and Out: thence the name C–Q delay.

D–Q delay mode utilizes the pre-evaluated characteristic of CD logic to alter superior operations. during this mode, CLK falls from high to low before IN transit, thence X at first rises to a nonzero voltage level. As shortly as IN become logic "0," whereas Y continues to be low, then X quickly rises to logic "1." A race condition exists during this case between X and Y. If CLK_d rises a lot of sooner than X and Y can attend logic "1," shut down money supply, and end in a false logic analysis. If CLK_d rises slightly slower than X, then Y can at first rise (thus slightly turns off M1) however eventually settle back to logic "0." CD logic will still perform the right operation during this case, however, its performance is degraded as a result of M1's reduced current drivability

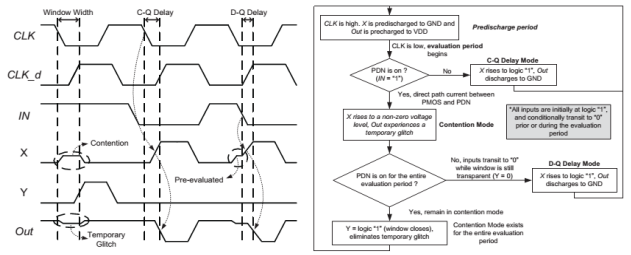

Fig. 4. Timing diagram and flowchart of the proposed CD logic

Compared to FTL, wherever the competition lasts for the complete analysis amount, TB effectively reduces CD logic's power consumption throughout the competition mode. The native window technique within the projected CD gate permits designers to customise the window breadth for various logic expressions to attain least power dissipation whereas not sacrificing the performance. as an example, a multiple input gate would require a extended window breadth than a NOR gate attributable to the larger internal capacitance as a result of the stacked Nmos transistors. Another advantage of CD logic is that the interior node (X) is usually connected to either VDD or GND, therefore creating the lustiness of CD logic such as static logic, except throughout the competition mode.

III. CD LOGIC DESIGN CONSIDERATIONS

A. CD Logic Sizing

The filler of INV1-3 and M3–M6 in Fig. 3(b) is near the minimum size so they are doing not produce a large space burden. The length of INV1-3 will be altered to rovide the specified temporal order window length supported designer's decisions. 1) CD Logic Versus Pseudo-nMOS: each pseudo-nMOS and CD logic ar magnitude relationed circuits that accept the proper pMOS to nMOS strength ratio to perform correct logic operations. pMOS semiconductor device dimension is usually designated to be concerning fourth part the strength of the nMOS PDN as a compromise between noise margin and speed in pseudo-nMOS . On the opposite hand, CD logic continually discharges X to GND once LK is high, therefore, CD logic will be optimized for low-to-high transition solely. Hence, pMOS clock transistors in CD logic will be upsized larger to produce a lot of speed, as long because the output flaw is maintained at a suitable level.

B. Output flaw

Fig. five depicts a simplified schematic of CD logic throughout the competition mode, wherever each transistors P1 and N1 ar on at the same time and induce a flaw voltage V1, that successively generates another smaller flaw V2. By design, V1 ought to be tiny [i.e., but the brink voltage (Vt)]. Hence, P1 operates within the saturation region whereas N1 is within the linear region. this equation is given as

$$\frac{1}{2}\mu_p C_{\text{ox}} \frac{W_{p1}}{L_{p1}} \left(V_{gsp1} - V_{tp}\right)^2 = \mu_n C_{\text{ox}} \frac{W_{n1}}{L_{n1}} \left[\left(V_{gsn1} - V_{tn}\right) V_{dsn1} - \frac{(V_{dsn1})^2}{2}\right]$$

where $\mu\ p$ and $\mu\ n$ are the hole and electron mobility of pMOS and nMOS transistors, respectively, Cox is the oxide

capacitance, W and L are the transistor width and length, respectively, and Vgs and Vds are the transistor gate-to-source and drain-to-source voltages, respectively.

C. Power Consumption

Data activity measures how frequent signals toggle and is defined as

$$\text{data activity} = \frac{\#\text{ of signal transitions}}{\#\text{ of signals} \times \#\text{ of clock cycles}}.$$

Static logic has associate degree empirical α of 0.1–0.2 associate degreed dynamic domino logic has an activity issue of 0.5. whereas CD logic's α is additionally 0.5, it invariably consumes power once it enters the analysis amount. throughout the analysis amount, CD logic invariably dissipates power via either dynamic power dissipation (X goes to VDD and Out is discharged to GND) or direct path current (contention mode). whereas CD logic consumes additional power, we tend to believe that CD logic remains a horny selection during a superior full-custom style because: 1) CD logic is merely supposed to exchange the important path; and 2) power management techniques like clock gating wherever the clock affiliation to idle module is turned off (gated), can considerably scale back CD logic's dynamic power consumption.

D. CD Logic Family

CD logic's pound [Fig. 3(a)] may be changed such the electrical converter is replaced by a static gate to attain even higher performance, since the electrical converter delay isn't wasted. we tend to sit down with such a variation as "compound CD logic" (CCD), analogous to the case of CDL of the dynamic domino logic. Another family of CD logic was planned in, wherever the output electrical converter is replaced by a dynamic domino logic. The analysis in shows that a 64-bit parallel-prefix adder using this type of logic is superior to its CDL-based counterpart, however, it needs further style issues thanks to the degraded noise margin.

IV. CD LOGIC CHARACTERIZATION

A.Noise Margin Versus Window Width

Noise margin is defined as the dc noise level at the input generating a false logic evaluation at the output of the same gate and can be computed based on the following formula:

$$\text{Noise Margin} = \left| V_{\text{original}} - V_{\text{noise}} \right|$$

B. CD Logic Performance

CD logic demonstrates superior performance, particularly for classy logic expressions, like Y = AB + C D (AOI22), within the D-Q mode thanks to the pre-evaluated characteristic. this is often emonstrated in Fig. 11, wherever CD logic is close to twofold quicker than dynamic domino logic. this is often contributed by: 1) the pre-evaluated characteristic; and 2) the less variety of transistors within the vital path (3N1P for dynamic, whereas solely 2P1N for CD logic). On the opposite hand, CD logic's performance is merely close to constant as or perhaps worse than that of dynamic domino logic throughout the C–Q mode. Therefore, it's advantageous to implement CD logic during a single-cycle period datapath as a result of then the pre-evaluated feature (D–Q delay) of CD logic is absolutely used. the ability consumption of CD logic at five hundredth knowledge activity is a minimum of three × and five × over that of static logic in AOI22 and therefore the remainder of logic expressions, severally. this means that CD logic ought to be used solely to interchange the vital path in any circuit block, since it's not energy economical to implement any system with CD logic solely. Table II summarizes the full junction transistor dimension of static, dynamic, and CD logic. Despite CD logic's extra junction transistor overhead, the common space of CD logic is thirteen smaller and four.5% larger than that of static and dynamic domino logic, severally.

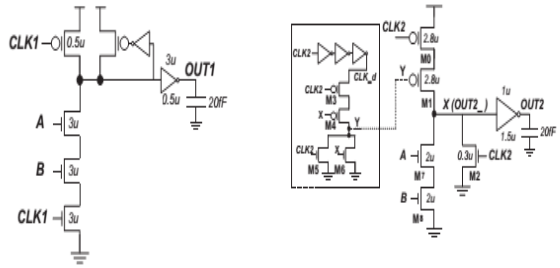

Fig. 11. Schematic and timing waveform of (a) dynamic and (b) CD logic.

V. CONCLUSION

A new superior logic vogue with CD characteristic and self-reset electronic equipment was projected. The pre-evaluated feature of CD logic makes it significantly appropriate in a very circuit block wherever a novel essential path exists and performance is that the primary concern. Performance analysis of 8-bit RCAs reveals that CD logic is thirty-nine and twenty third quicker than static and dynamic domino logic, severally. Simulation results of 32-bit CLAs show similar speed advantage of CD logic compared to static logic. during this setup, CCD logic achieves lowest PDP in any respect information activity except at 100%. Also, CCD logic achieves the most effective automatic data processing results, with 66% (37%) reduction compared to static logic at 50% (10%) information activity. The 6σ worst case flaw for CD and CCD logic at 110°C are 220.8 and 303.4 mV, severally. CD logic's benefits in terms of delay and automatic data processing were additionally incontestable in 8-bit Wallace tree multipliers. Compared to 32-bit adders, CD logic achieves an analogous delay improvement, however has a good higher automatic data processing reduction, primarily as a result of the ultimate adder that makes up the essential path of the number may be a comparatively little circuit block of the general electronic equipment. At 25% α, CD logic is 52, 25, and 37% additional EDP-efficient than static, dynamic, and pseudo-nMOS logic, severally.

REFERENCES

[1] R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," IEEE J. Solid-State Circuits, vol. 32, no. 7, pp. 1079–1090, Jul. 1997.
[2] N. Goncalves and H. De Man, "NORA: A racefree dynamic CMOS technique for pipelined logic structures," IEEE J. Solid-State Circuits, vol. 18, no. 3, pp. 261–266, Jun. 1983.
[3] C. Lee and E. Szeto, "Zipper CMOS," IEEE Circuits Syst. Mag., vol. 2, no. 3, pp. 10–16, May 1986.
[4] R. Rafati, S. Fakhraie, and K. Smith, "A 16-bit barrel-shifter implemented in data-driven dynamic logic (D3L)," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 53, no. 10, pp. 2194–2202, Oct. 2006.
[5] F. Frustaci, M. Lanuzza, P. Zicari, S. Perri, and P. Corsonello, "Lowpower split-path data-driven dynamic logic," Circuits Dev. Syst. IET, vol. 3, no. 6, pp. 303–312, Dec. 2009.
[6] N. Weste and D. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th ed. Reading, MA: Addison Wesley, Mar. 2010
[7] K. Bernstein, High Speed CMOS Design Styles, 1st ed. New York: Springer-Verlag, Aug. 1998.

