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MINIMUM DELAY ADDER FOR VLSI ARCHITECTURE

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Abstract: Adders are one of the most widely digital components in the digital integrated circuit design and are the necessary part of Digital Signal Processing (DSP) applications. With the advances in technology, researchers have tried and are trying to design adders which offer either high speed, low power consumption, less area or the combination of them. The addition of the two bits is very based on the various speed-up schemes for binary addition, a comprehensive overview and a qualitative evaluation of the different existing adder architectures are given in this thesis. In addition, their comparison is performed in the thesis for the performance analysis. In this paper, We will see at Ripple Carry adder, Carry look- ahead Adder, Carry Select Adder and Carry Save Adder in ISE XIILINX 10.1 by using HDL - Verilog and will simulate them in Modelsim 6.4a.

I. INTRODUCTION

The Addition is a fundamental operation for any digital system, digital signal processing or control system. A fast and accurate operation of a digital system is greatly influenced by the performance of the adders. Adders are also very important component in digital systems because of their extensive use in other basic digital operations such as subtraction, multiplication and division. Hence, improving performance of the digital adder would greatly advance the execution of binary operations inside a circuit compromised of such blocks. The performance of a digital circuit block is gauged by analyzing its power dissipation, layout area and its operating speed. ALU is the key element of digital processors like as microprocessors, microcontrollers, central processing unit etc. Every digital domain based technology depends upon the operations performed by ALU either partially or whole. [21] The ALU, or the arithmetic and logic unit is the section of the processor that is involved with executing operations of an arithmetic or logical nature. Arithmetic Logic Unit (ALU) is a critical component of a microprocessor and is the core component of central processing unit. The logic circuitry in this units is entirely combinational (i.e. consists of gates with no feedback and no flip-flops).The ALU is an extremely versatile and useful device since, it makes available, in single package, facility for performing many different logical and arithmetic operations. ALU can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. Arithmetic instructions include addition, subtraction, and shifting operations, while logic instructions include Boolean comparisons, such as AND, OR, XOR, and NOT operations.

II. ADDITION AND SUBTRACTION

These two tasks are performed by constructs of logic gates, such as half adders and full adders. While they may be termed 'adders', with the aid of them we can also perform subtraction via use of inverters and 'two's complement' arithmetic. A binary adder-substractor is a combinational circuit that performs the arithmetic operations of addition and subtraction with binary numbers. Connecting n full adders in cascade produces a binary adder for two n-bit numbers.

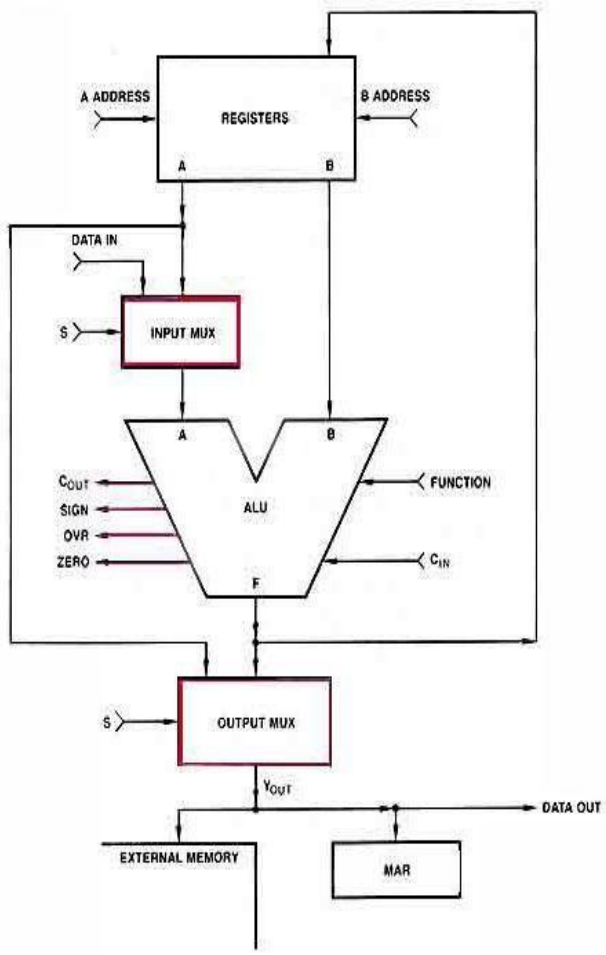

Figure 1.1: Basic Arithmetic logic unit

III. TYPES OF ADDERS

In electronics, an Adder is a device which will perform the addition, S, of two numbers. In computing, the adder is part of the ALU, and some ALUs contain multiple adders. Although adders can be constructed for many numerical representations, such as Binary-coded decimal or excess-3, the most common adders operate on binary numbers. Also addition is the most basic function performed on the two binary digits. The simple addition consists of the addition of two one bit numbers A and B, where possible addition is

0+0=0; 0+1=1; 1+0=1; 1+1=10. So we can say that the former three additions gives 1 bit result but when augend and addend both are 1 then the result or sum is 2 bit number where the higher significant bit is called as carry. When augend and addend contains more significant digits then the carry is added to the next higher order of significant bits. A Combinational circuit that performs the addition of the two bits is called HALF ADDER and digital circuit that performs the addition of the three bits (two significant bit and previous carry) is called the FULL ADDER. The name of the latter comes from the fact that it contains two half adder circuits. [1]

IV. PARALLEL ADDERS

Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N- bit parallel adder, there must be N number of full adder circuits. A parallel adder is an adder which adds all bits of two numbers in just one clock cycle. It has separate adder circuit for each bit. Therefore to add Two N bit numbers adder requires n separate adder circuits [26].

1) Ripple carry adder or carry propagate adder
2) Carry-Skip Adder
3) Carry-Look ahead Adder
4) Carry-Select Adder
5) Carry Save adders
6) Conditional sum adder

V. RESULT AND CONCLUSION

The four adders are synthesized i.e. Ripple Carry adder, Carry look- ahead Adder, Carry Select Adder, Carry Save Adder in ISE XIILINX 10.1 by using HDL - Verilog and simulated them in Modelsim 6.4a. By comparing them in terms of delay i have reached the conclusion that Carry Select adder has the lowest delay among them and hence it is fastest of them all. Also Ripple carry adder and Carry look ahead adder has the same and maximum delay but according to theory carry look ahead adder has less delay than Ripple carry adder because it does not calculate carry on each stage but uses the direct equations to calculate sum and carry. The number of slices used in carry look ahead adder is minimum and maximum in carry save adder. And number of Look Up Tables used is minimum in Ripple carry adder, and Carry look – ahead adder but maximum in carry save adder. Also number of IOB is less in carry select adder than others. Hence we reach to the conclusion that minimum delay among four is carry select adder. We are mainly doing this comparison based on the synthesis and simulation to get the minimum Delay possessing adder.

REFERENCES

[1] M. Morris Mano; “Digital logic and computer design”; Prentice hall of India Private limited (2003).
[2] Chip-Hong Chang, Jiangmin Gu, Mingyan Zhang, “A Review of 0.18-um Full adder Performances for Tree Structured Arithmetic Circuits,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 13, no. 6, pp. 686-695, June 2005.
[3] K. Ramu, B.N. Srinivasa Rao; “Implementation of Area Efficient 16bit Adder in SPARTAN-3 FPGA”
[4] May Phyo Thwal, Khin Htay Kyi, and Kyaw Swar Soe; “Implementation of Adder-Subtracter Design with Verilog HDL” World Academy of Science, Engineering and Technology Vol:2 , March 2008.
[5] T. RatnaMala, R. Vinay Kumar, T. Chandra Kala; “Design and Verification of Area Efficient High-Speed Carry Select Adder”, International Journal of Research in Computer and Communication technology, IJRCCT, ISSN 2278-5841, Vol 1, Issue 6, November 2012.
[6] Mark S. K. Lau, Keck Voon Ling, Yun Chung Chu, and Arun Bhanu; “Modeling of Probabilistic Ripple-Carry Adders”, School of Electrical and Electronic Engineering Nanyang Technological University Singapore 63979
[7] Santanu Maity, Bishnu Prasad De, Aditya Kr. Singh,”Design and Implementation of Low-Power High-Performance Carry Skip Adder” International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249 –8958,Volume-1, Issue-4, April 2012
[8] Fast Adder Architectures: Modeling and Experimental Evaluation; “Nuno Roma and Tiago Dias and Leonel Sousa”
[9] J. Sklansky; “The conditional sum logic” Electronic Computers, IRE Transactions on (Volume:EC-9 , Issue: 2) IEEE 1980.
[10] Kuo-Hsing Cheng, Shu-Min Chiang, and Shun-Wen Cheng; “The Improvement of Conditional Sum Adder for Low Power Applications” ASIC Conference 1998. Proceedings. Eleventh Annual IEEE International 1998.
[11] Burgess, N. (2011), “Fast Ripple carry adder in srtandard cell cmos VLSI”, 20th IEEE Symposium on Computer Arithmetic. pp. 103–111.

