International Journal For Technological Research In Engineering
Volume 3, Issue 10, June-2016 *ISSN (Online): 2347 - 4718*

A NOVEL DESIGN OF WIDEBAND TSPC DIVIDE-BY-32/33 DUAL MODULUS PRESCALER

Surya.S
PG Student, Dept. of Communication System, Dhanalakshmi Srinivasan Engineering College, Perambalur, Tamil Nadu, India

ABSTRACT: A high-speed CMOS TSPC divide-by-32/33 dual modulus prescaler is proposed. The speed of the prescaler is improved in two aspects. First, by adopting a new pseudo divide-by-4/5 prescaler, the minimum working period is effectively reduced by half a NOR gate's delay. Second, by changing the connection of TSPC D-Flip-Flops, the minimum working period is further reduced by half an inverter's delay. Simulation results show that the maximum operating frequency of the proposed circuit is improved & compared with conventional circuit. This Proposed System Implemented using Dsch and microwind Software.

I. INTRODUCTION

High-speed frequency divider design is crucial for frequency synthesizers, clock generators, clock and data recovery circuits and satellite communication systems. In the 1980s and 1990s, designers preferred to use high-fT technologies like GaAs and BiCMOS in order to divide signals at tens of GHz frequency . Afterwards, as the technology nodes went below 1 μm, it was possible to design multi-gigahertz speed frequency dividers in CMOS. The architectures of these CMOS dividers were commonly based on limited-outputswing current-mode-logic (CML) or LC injection-lock topologiesDual-modulus frequency prescaler plays an main role in phase-locked loop (PLL) designs[1]. In spite of fact that current-mode logic and inject locking prescaler can provide working frequency of hundreds/tens GHz with process of SoI CMOS or InP DHBTs and so on. TSPC dual-modulus prescaler is greatly utilized in several GHz with standard CMOS process[2],[3]. TSPC prescaler has the merits of single clock phase, low power, small area, and large output swing. Speed improvement is an important design issue for TSPC prescaler. In addition to the above, several techniques have been developed. At the transistor level decreasing the threshold voltage of nMOS transistors, forward body biasing technique can improve the speed, but it suffers from increased cost and decreased robustness as well as high minimum working frequency[4]. At the gate level, by adopting E-TSPC(extended-true single phase clock) flipflops can effectively improve the operating speed performance. But the serious is current leakage, thus the performance of the minimum working frequency is limited. At the RTL level, speed improvement of divide-by-2/3 prescaler can also increases in improving the speed of divide-by-16/17 prescaler. However, several TSPC circuit design rules are broken in these paper. It mainly leads to shrinking the range of frequency because these prescalers are not suitable for low frequency operation for longer time.

II. RELATED WORK

In the transistor level, forward body biasing technique can improve the speed by decreasing the threshold voltage of nMOS transistors. However, it suffers from high minimum working frequency as well as increased cost and decreased robustness.

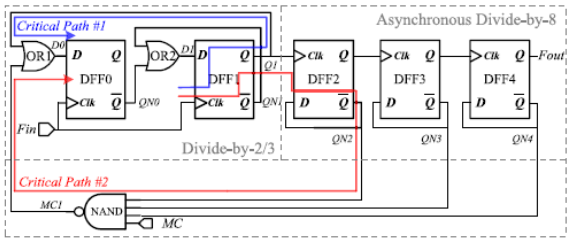

Fig: Schematic of conventional divide-by-16/17 prescaler

divide-by-16/17 prescaler. It consists of a pseudo divide-by-2/3 prescaler, an asynchronousdivide-by-8 divider, and a four-input AND gate. Compared with the conventional circuit, there are two main changes in the proposed divide-by-16/17 prescaler. First, a new pseudo divide-by-2/3 prescaler is adopted instead of conventional divide-by-2/3 prescaler. Timing diagram of proposed divider-by-16/17 prescaler. The pseudo divide-by-2/3 prescaler can exactly accomplish a single, but not continuous divide-by-3 operation. In addition, it is enough for divide-by-16/17 prescaler because it only needs less than one divide-by-3 operation in a cycle. By adopting the pseudo divide-by-2/3 prescaler, an OR gate is saved and there leaves only one AND gate in front of DFF0. As a result, the critical path #1 in conventional circuit is disappeared and the length of critical path #2 is reduced. Second, QN1 and QN2 node (instead of Q1 and Q2 node in conventional

circuit) of DFF1, DFF2, and DFF3, is connected to the input CLK node of DFF2, DFF3, and DFF4, respectively. The propagation delay of DFF1, DFF2, and DFF3 will all decrease from td−Q totd−QN. Thus, the length of critical path will be further reduced. The operation mode of proposed circuit is as follows. When MC = 1, MC1 changes its value according to (QN2, QN3, QN4). The pseudo divide-by-2/3 prescaler controlled by MC1 accomplishes seven times of divide-by-2 operations and one time of divide-by-3 operation in a cycle. The whole circuit operates in divide-by-17 mode. When MC = 0, MC1 keeps low and the pseudo divide-by-2/3 prescaler keeps on divide-by-2 operation. The whole circuit works in divide-by-16 mode. As well as the conventional circuit, the maximum working frequency of proposed prescaler is decided by its divide-by-17 operation

mode. In addition, the key operation in divide-by-17 mode is the divide-by-3 operation of pseudo divide-by-2/3 prescaler. Fig. 4 shows the timing diagram of this key operation of proposed circuit. In the first rising edge of Fin, QN1 and QN2 switch to high, then MC1 switches to high and holds for two periods. In the second rising edge, QN0 and D1 switch to low for two periods. In the third rising edge, QN1 switches to high and holds for two periods. From the second to the fifth rising edge of Fin, DFF1 outputs a divide-by-3 signal in node QN1 and the pseudo divide-by-2/3 prescaler accomplishes a divide by- 3 operation. After this, the pseudo divide-by-2/3 prescaler will carry out seven times divide-by-2 operation. A divide-by-17 signal will be obtained in node Fout. the MOSFET-level schematic of the proposed divide-by-16/17 prescaler. The whole circuit is realized in TSPC structure for high robustness and low static power. AND1 and AND2 are absorbed into the first stage of DFF0 and DFF1, respectively. Only normal MOSFETs are adopted in the circuit, the total cost can be saved. What's more, or the low voltage operation, the six cascaded MOSFETs may need to be split into several branches and each of that should have less number of cascoded MOSFETs. Thus, the correct function can be maintained. From the timing in the second rising edge of Fin, QN1 switches to low and then D1 switches to low no matter what the value of QN0 is. But QN0 has to be low in the third rising edge so that D1 can hold the low value for one more period. That means MC1 should switch to high at least before the third rising edge of Fin coming.

III. PROPOSED SYSTEM

A Conventional Dual-Modulus Prescaler 32/33 Circuit. It Receives A Clock Signal And Divides By 32 Or 33, Depending On The Value Of An External Control Signal Called Sm: When Sm Is At Low Logic Level, The Circuit Divides The Clock By 32 (N); When Sm Is At High Logic Level, It Divides The Clock By 33 (N+1). This Circuit Is Composed Of Two Counters, A Synchronous Counter And An Asynchronous Counter. In The Crosshatched Part We Find The Synchronous Counter That Carries Out The Counting Up To 4 Or 5, Depending On The Value Of The Signal Div8. The Synchronous Counter Constitutes The Critical Element For Good Performance In Terms Of Speed, Since It Receives As Its Clock The Signal From The Vco Output And, Thus, Works In The Highest Speed Of The System.The Asynchronous Part Is Composed Of Three D Type Flip-Flops (Dff) That Carry Out The Counting Up To 8. It Is The Synchronous Counter That Generates The Clock For The First D-Ff Of The Asynchronous Counter The Implementation Proposed Here For The Prescaler Is Based On A New Synchronous Counter Circuit. This Circuit Is In Fact A State Machine And, Similar To Any State Machine, It Can Be Implemented With The Fo-Data Chains Previously Defined. The Desired Output Of The Circuit, The Clock Divided By 4 Or 5, Is The State Machine Output And Will Be Produced By The Combination Of Two Other Signals, Which Are Generated With A Rate Equal To The Half Of The Clock Rate. The New Implemented Synchronous Counter Works As The State Machine Whose Diagram Is In Figure 5, And Its Clock, Clk/2, Has A Frequency Equal To The Half Of The Original Clock Frequency (The Clock That We Desire To Divide By 4 Or 5). The Output Is Formed From The Combination Of Signals A And B: A During The Phase Where Clk/2 Is High And B During The Phase Where Clk/2 Is Low. We Can Exemplify The Operation Analyzing The State Diagram Of When The Logic Value At The Div8 (Division Control Signal) Is Hig

There Are Two Possible Operations For The State Machine: To Be Moving Between States 000 And 110, Or Between 100 And 010. Let Us Consider The Case Of Moving Between 000 And 110. The Output Signal Will Have The Values Low, A, Low, B, High, A, And High, B (0011) During Each Half Cycle Of The Clk/2. If We Remember That The Circuit Works With Half Of The Original Clock Signal Rate, We Can See That The Ab Combination Is The Original Clock Signal Divided By 4. When The Logical Value In Div8 Is Low,The States Will Pass Through The Following States: 000, 110, 001, 010 And 101 And The Output Will Have The Values Low, A, Low, B, High, A, High, B, Low, A, Low, B, Low, A, High, B, High, A, And Low, B, (0011000110), During Each Half Cycle Of The Clk/2. In This Case We Can See That Ab Combination Is The Clock Signal Divided By 5.

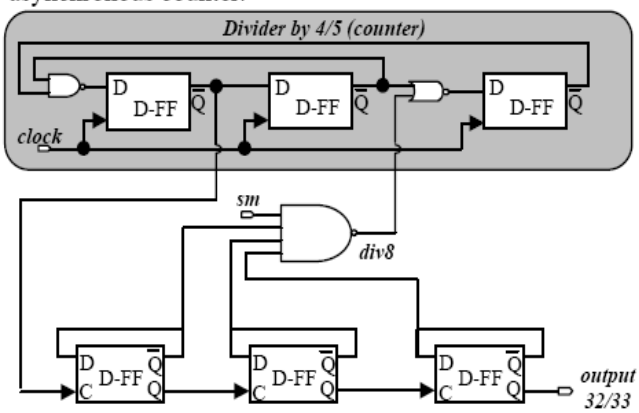

Fig: proposed 32/33 design

ADVANTAGES

- It has the merits of single clock phase, low power, small area, and large output swing
- These pre scalers are no longer suitable for low frequency operation
- Its Contains Multi signal like 2/3 and 4/5.
- It will be operate a multi Signal 16/17 and 32/33 so we can vary the Four Different Frequencies.
- Its contain Four Different Frequencies but occupying a same area like a 16/17 Prescaler.

IV. SIMULATION RESULTS

The complete layout of the dual-modulus prescaler 32/33 circuitnwas implemented in a 0.10 μm CMOS technology. Several simulations based on the netlist extracted from the layout were carried out. These simulations have been done through the program DSCH and micro wind

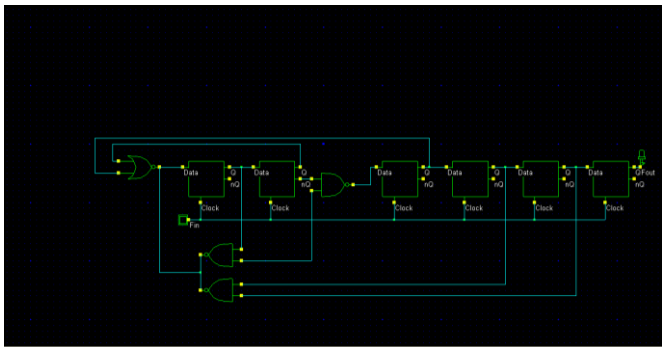

Fig:Digital schmatic diagram

LAYOUT:

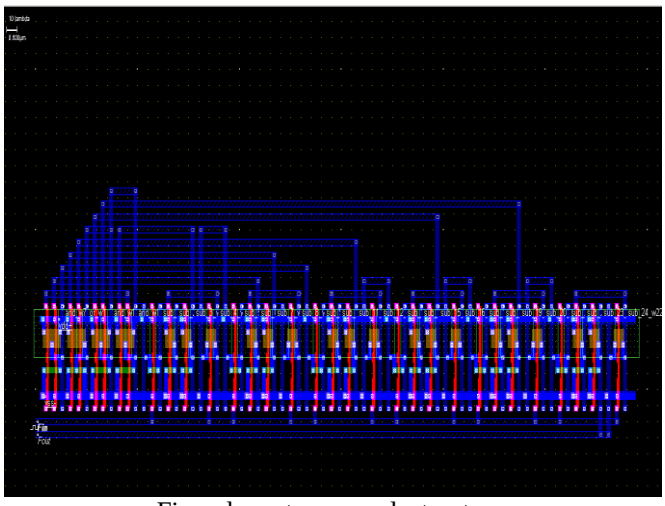

Fig: layout proposed structure

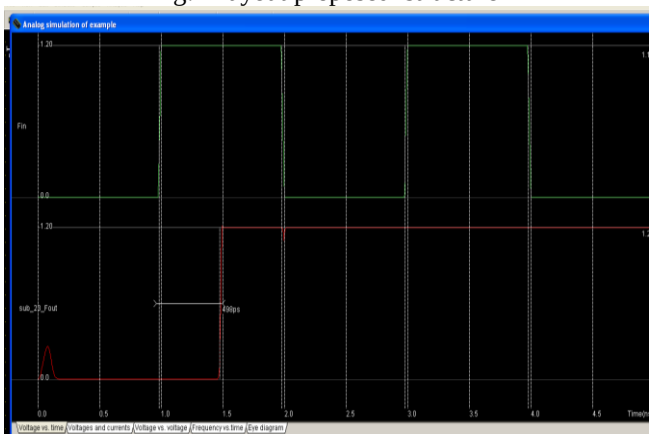

Fig: Voltage Vs Time:

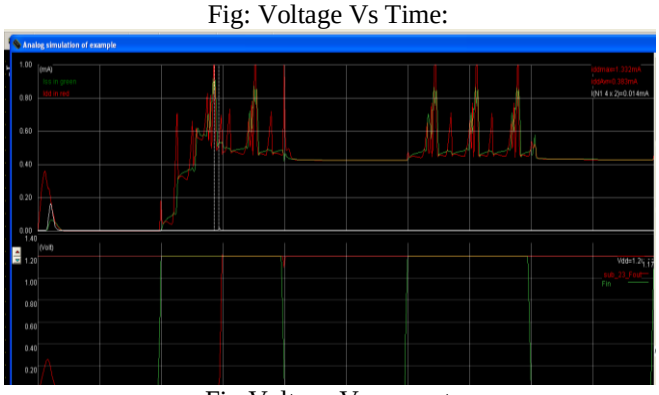

Fig:Voltage Vs current

V. CONCLUSION

This brief presents a novel high-speed TSPC divide-by-32 /33 ual modulus prescaler. The speed of the proposed circuit is improved in two aspects. First, by adopting a new pseudo divide-by-4/5 prescaler, pseudo divide-by-4/5 prescaler, the minimum working period is effectively reduced by half a NOR gate's delay. Second, by changing the connection of TSPC DFFs, the minimum working period is further reduced by half an inverter's delay. What's more, the minimum working frequency performance is not deteriorated at the same time. Finally did 32/33 Prescaler with the TSPC Flip-flop.

REFERENCES

[1] T. Shibasaki, H. Tamura, K. Kanda, H. Yammaguchi, J. Ogawa, and T. Kuroda, "A 20-GHz injection-locked LC divider with a 25% locking range," in Int. Symp. VLSI Circuits Dig. Tech. Papers, Jun. 2006, pp. 170–171.

[2] D. D. Kim, J. Kim, and C. Cho, "A 94GHz locking hysteresis-assited and tunable CML static divider in 65nm SOI CMOS," in IEEE ISSCC Dig. Tech. Papers, Feb. 2008, pp. 460–628.

[3] D. A. Hitko, T. Hussain, D. S. Matthews, R. D. Rajavel, I. Milosavljevic, and M. Sokolich, "State of the art low power (42 mW per flipflop) 50 GHz+ CML static divider implemented in scaled 0.2 m emitter-width InP DHBTs," in Proc. InP Rel. Mater. Conf., May 2006, pp. 85–88.

[4] B. Chang, J. Park, and W. Kim, "A 1.2 GHz CMOS dual-modulus prescaler using new dynamic D-type flip-flops," IEEE J. Solid-State Circuits, vol. 31, no. 5, pp. 749–752, May 1996.

[5] C.-Y. Yang, G.-K. Dehng, J.-M. Hsu, and S.-I. Liu, "New dynamic flip-flops for high-speed dual-modulus prescaler," IEEE J. Solid-State Circuits, vol. 33, no. 10, pp. 1568–1571, Oct. 1998.

[6] S. Kim and H. Shin, "An E-TSPC divide-by-2 circuit with forward body biasing in 0.25 µm CMOS," IEEE Microw. Wireless Compon. Lett., vol. 19, no. 10, pp. 656–658, Oct. 2009.

[7] H. Shin, "A 1-V TSPC dual modulus prescaler with speed scalability using forward body biasing in 0.18 µm CMOS," IEICE Trans. Electron., vol. E95-C, no. 6, pp. 1121–1124, Jan. 2012.

[8] M. V. Krishna, M. A. Do, K. S. Yeo, C. C. Boon, and W. M. Lim, "Design and analysis of ultra low power true single phase clock CMOS 2/3 prescaler," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 1, pp. 72–82, Jan. 2010.

[9] W.-H. Chen and B. Jung, "High-speed low-power true single-phase clock dual-modulus prescalers," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 58, no. 3, pp. 144–148, Mar. 2011.

[10] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits: A Design Perspective, 2nd ed. New York, NY, USA: Prentice- Hall, 2003, pp. 350–352.

[11] J. Yuan and C. Svensson, "High-speed CMOS circuit technique," IEEE J. Solid-State Circuits, vol. 24, no. 1, pp. 62–70, Feb. 1989.
[12] X. P. Yu, W. M. Lim, M. A. Do, X. L. Yan, and K. S. Yeo, "6.1 GHz 4.6 mW CMOS divide-by-55/56 prescaler," Electron. Lett., vol. 44, no. 24, pp. 1402–1403, Nov. 2008.
[13] Y. X. Peng,M. V. Do, W.M. Lim, K. S. Yeo, and J.-G. Ma, "Design and optimization of the extended true single-phase clock-based prescaler," IEEE Trans. Microw. Theory Tech., vol. 54, no. 11, pp. 3828–3835, Nov. 2006.
[14] V. K. Manthena, M. V. Do, C. C. Boon, and K. S. Yeo, "A low-power single-phase clock multiband flexible divider," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 20, pp. 376–380, Feb. 2012.

