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DESIGN AND IMPLEMENTATION OF ADIABATIC LOW POWER FREQUENCY DIVIDER AND DIVISION STAGES

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Abstract: ***The frequency division is the significant implementation. Frequency dividers composed of two D-latches in cascade and in a negative feedback configuration which can be used in PLL and Pre-scale ICs. The digital operation of this type of division provides the advantage of suppressing the sensitivity to waveform distortion. This paper presents a CMOS transmission gate and high speed diode free adiabatic logic based frequency division in incorporating a new high speed latch topology. The circuit is designed and simulated in a standard 0.18µm CMOS process technology. The architecture is primarily of transmission gates and diode free adiabatic inverter used as latches with negative feedback thus frequency division is achieved. The division stages necessary for the pre-scale IC is implemented in the cadence.***

Keywords: Transmission gate, DFAL inverter, frequency division, pre-scale IC, virtuoso, cadence.

I. INTRODUCTION

During the past 10 years, the connectivity features of electronic devices have seen a tremendous expansion and the electronics industry has been experiencing an unprecedented spurt in growth, thanks to the use of integrated circuits in computing telecommunications and consumer electronics. The ever-growing number of transistors integrated on a chip and the increasing transistor switching speed in recent decades has enabled great performance improvement in computer systems by several orders of magnitude. However, the increased functionality and high speed operation result in high power dissipation which eventually creates a need for low power design solutions. Different solutions both at the architectural and structural levels have been suggested. Such phenomenal performance improvements have been accompanied by an increase in power and energy dissipation of the systems. Higher power and energy dissipation in high performance systems require more expensive packaging and cooling technologies, increase cost, and decrease system reliability. Adiabatic logic style is more energy efficient than the other conventional CMOS logic style. Digital CMOS integrated circuits have been the driving force behind VLSI for high performance computing and other applications, related to science and technology. The demand for digital CMOS integrated circuits will continue to increase in the near future, due to its important salient features like low power, reliable performance and improvements in the processing technology. In this paper the frequency division of the signal which is generally used to supply for the peripherals in the microcontrollers and the microprocessors or the PLL circuits is achieved. The stages required to pre-scale division is implemented, this can be achieved by the transmission gate and the diode free adiabatic inverter acts as a combination of master salve flip-flops leads to the frequency division and the estimation of the pre-scale IC circuitry is proposed.

II. TRANSMISSION GATE

The transmission gate is an electronic element that will block or pass a signal level from the input to the output. The CMOS based switch in which PMOS passes a strong 1 but poor 0 and NMOS passes strong 0 but poor 1. The PMOS and NMOS work simultaneously. The two field effect transistors, an n-channel MOSFET and a P-channel MOSFET are connected in parallel however the drain and source terminals of two transistors are connected together. The gate terminals are connected to each other via a NOT gate to form the control terminal.

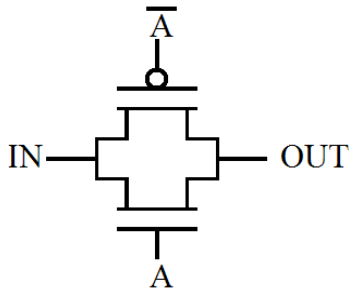

Fig 2.1: Transmission gate

When the control input is logic zero the gate of the n-channel MOSFET is also at a negative supply voltage potential. Inverter causes p-channel MOSFET as a positive terminal. Accordingly neither of the two transistors will conduct and the transmission gate turns off. When the control input is a logic one, so the gate terminal of the n-channel MOSFET is positive and the p-channel is at the negative supply voltage potential, whereby the transistor starts to conduct and the transmission gate switches on.

III. DFAL INVERTER

The adiabatic logic circuits suffer from amplitude degradation, large time delays and circuit complexity. The drawbacks of such adiabatic circuits can be eliminated by using DFAL style. The DFAL style removes the diode from the charging and discharging path to overcome the disadvantage. The circuit diagram and simulated waveforms verifying the operation of an inverter based on DFAL circuit.

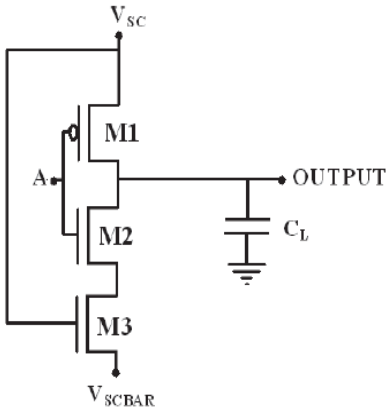

Fig 3.1: DFAL inverter

The attractive feature of proposed topology is that it is diode free there is not any diode in its charging or discharging path. One clock is in phase while the other is inverted. The voltage difference between the electrodes and consequently power dissipation is reduced. Split level clock charges/discharges the load capacitance comparatively slowly than the other adiabatic power clocks. The efficiency of adiabatic logic circuits depends upon how slowly the load capacitance is charged or discharged so power dissipation is minimized further. The schematic of DFAL resembles the static CMOS logic; however circuit operates in adiabatic manner. The nMOS transistor M3 in the pull down network adjacent to the M2 is used to replace the diode for the discharging. Power clock controls the turning ON and OFF of this transistor M3. The main power dissipation in reported adiabatic circuits in their discharging path occurs at the (MOS) diodes. Due to the threshold voltage drop whereas in our proposed circuit it is due to the ON resistance of channel of MOS transistor M3.

IV. NEED FOR LOW POWER DESIGN

Low power design is necessary for gaining and keeping market share. There are various interpretations of the Moore's Law that predicts the growth rate of integrated circuits. One estimate places the rate at 2X for every eighteen months. Others claim that the device density increases ten-fold every seven years. Regardless of the exact numbers, everyone agrees that the growth rate is rapid with no signs of slowing down. The new generations of processing technology are being developed while present generation devices are at very safe distance from the fundamental physical limits. A need for low power VLSI chips arises from such evolution forces of integrated circuits. The Intel 4004 microprocessor, developed in 1971, had 2300 transistors, dissipated about 1 watts of power and clocked at 1 MHz. Then comes the Pentium in 2001, with 42 million transistors, dissipating around 65 watts of power and clocked at 2. Another factor that fuels the need for low power chips is the increased market demand for portable consumer electronics powered by batteries. The craving for smaller, lighter and more durable electronic products indirectly translates to low power requirements Battery life is becoming a product differentiator in many portable systems. Being the heaviest and biggest component in many portable systems, batteries have not experienced the similar rapid density growth compared to the electronic circuits. The main source of power dissipation in these high performance battery portable digital systems running on batteries such as note-book computers, cellular phones and personal digital assistants are gaining prominence. An ICs total power consumption comprises two types, static and dynamic. Static power typically comes from the leakage current and dc current sources. Dynamic current consumption, which is frequency dependent, often determines the total power. It comes from the charging and discharging of capacitive nodes and the crowbar action of switching transistors connected between the supplies. For these systems, low power consumptions a prime concern, because it directly affects the performance by having effects on battery longevity. In this situation, low power VLSI design has assumed great importance as an active and rapidly developing field. Another major demand for low power chips and systems comes from the environmental concerns. Modern offices are now furnished with office automation equipments that consume large amount of power.

V. FREQUENCY DIVISION

Frequency dividers are useful in many communication applications such as Frequency synthesizers, Timing recovery circuits and clock generations. The design of frequency divider is an important factor in performance of PLL as it is in feedback path and so locking gets difficult. Basic gates and flip-flops can be used to design frequency dividers. One of the triggering flip-flops the D-flip-flops are implemented.

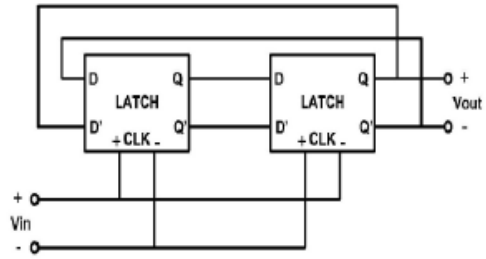

Fig 5.1: D-latch frequency divider block diagram

The D-latches connected in the cascade acts as a master and slave leads to the design of the circuit in which division of the frequency is achieved when the feedback output is inverted and supplied to the input. The fundamental components the transmission gates and the DFAL inverters are used to design the latches. Each latch contains a couple of inverter and the transmission. The fig 5.3 shows the master slave D-flip-flop. When the higher frequency division is necessary, a purely analog solution has to be taken into consideration. The two main solutions to multi-GHz frequency division are: master-slave latch divider, and injection-locking divider. The MS divider employs a two stage regenerative divider. The ILD solution, instead, exploits the injection pulling effect on a VCO tuned at a frequency the half of the injected one.

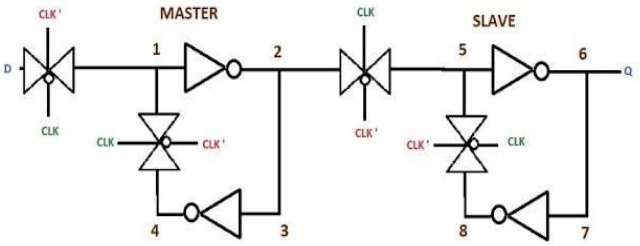

Fig 5.2: Master-slave frequency divider

The operation of the transmission gate based D-flip-flop must be analyzed considering the fig: 5.1, the two D-latches are connected in cascade and initially the D input is logic low and also the clock input is low leads to the path D-1-2-3-4. The transmission gate at the 4 acts as a open switch because of the inverting clock input compared to the transmission gate at the D input. The slave D-latch is ignored. When the clock is logic high causes the slave latches to logic high and leads to the Q output high where D-1-2-3-4 from the master and 2-5-6-7-8 enable themselves as a active paths. The clock is low slave latches D, any changes in D is seen in 4 and latches on to Q during the next positive edge.

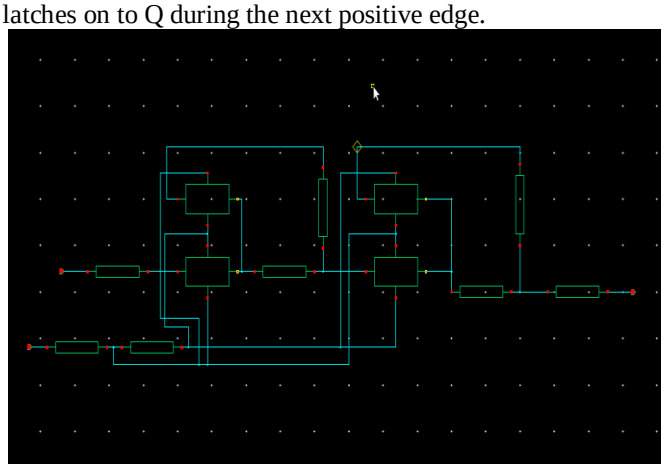

Fig 5.3: Schematic diagram of frequency divider

VI. PRESCALE DIVISION

The pre-scaler is an electronic counting circuit used to divide a high frequency electrical signal to a low frequency signal. Pre-scalers are typically used at very high frequency to extend the upper frequency range as frequency counters, phase locked loop synthesizers and the counting circuits. The pre-scale circuit consists of 4 stages of cascaded positive edge triggered D Flip-flops. The D Flip-flop design has been implemented using DFAL inverters and transmission gates by cascading two D latches with one clock and one input. The clock input is applied to subsequent flip flop comes from the output of its immediately preceding flip flop. For first or instance the output of the first register acts as the clock input to the second register and the output of the second register feed the clock input of third register. The second register can change state only after the output of first register can change its state. That is the second fact that it gets its own clock input from output of the first and not from the input clock. The pre-scaling circuit play an important role in the microprocessors, microcontrollers, PLLs and other design methodologies of the pre-scale ICs where the different peripherals enables on the different threshold frequencies in the device basically the division of the scale 2,4,8 and 12 are implemented.

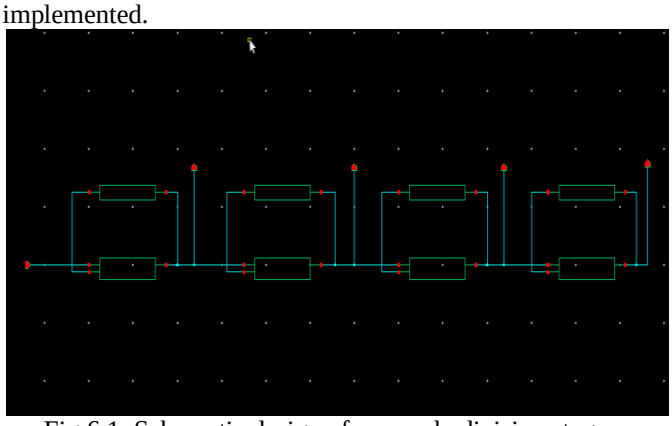

Fig 6.1: Schematic design of pre-scale division stages

VII. RESULTS

The feature of D-type flip-flop is as a binary divider, for frequency division. Here the inverted output terminal (NOT-Q) is connected directly back to the data input terminal d-in giving the device feedback as shown in the fig 7.1.

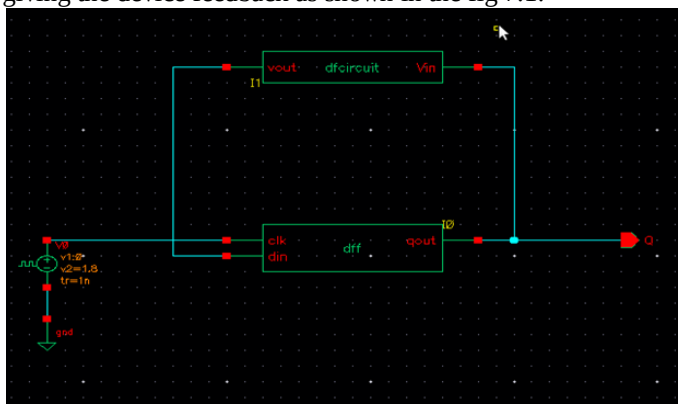

Fig 7.1: Schematic diagram of the frequency divider block diagram.

The frequency division waveform is shown in fig 7.2. The feeding back the output from NOT-Q to the input terminal D, the output pulses at Q has a frequency that exactly one half (f÷2) that of the input clock frequency. In other words the circuit produces frequency division as it now divides the input frequency by a factor of two.

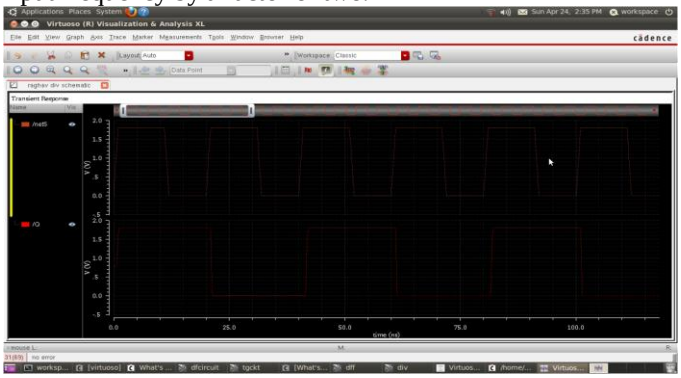

Fig 7.2: Output waveform of Frequency division by 2

The frequency divisions block are connected in cascade, with the respective feedbacks are given to the respective inputs as shown the schematic diagram of the pre-scale divider in the fig 6.1. The intermediate outputs are considered which gives the frequency division of stages. These type of frequency divider circuits are generally used in the PLL frequency division circuits. The division by the factor of 2,4,8,12 are implemented. The fig 7.3 shows the pre-scale division block diagram.

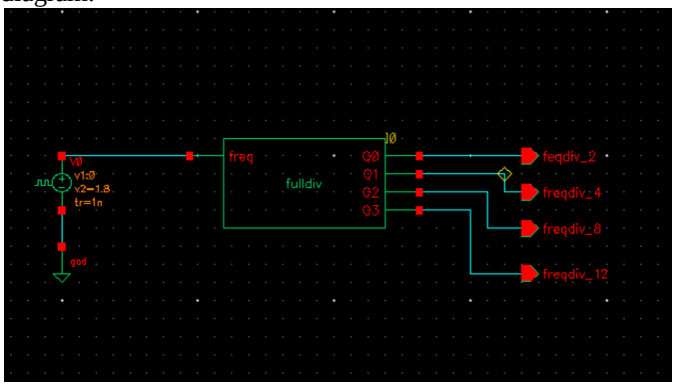

Fig 7.3: Pre-scale division block diagram

The fig 7.4 is the output waveform of the master-slave positive edge triggered D-flip-flop which is implemented by using the transmission gate and the DFAL inverter. For every rising edge of the clock frequency the output Q fetches the data from the input signal regard less of the falling edge of the clock, this feature make the division possible when the inverted output signal is feed backed to the input data as shown in the fig 7.1 with the usage of inverter.

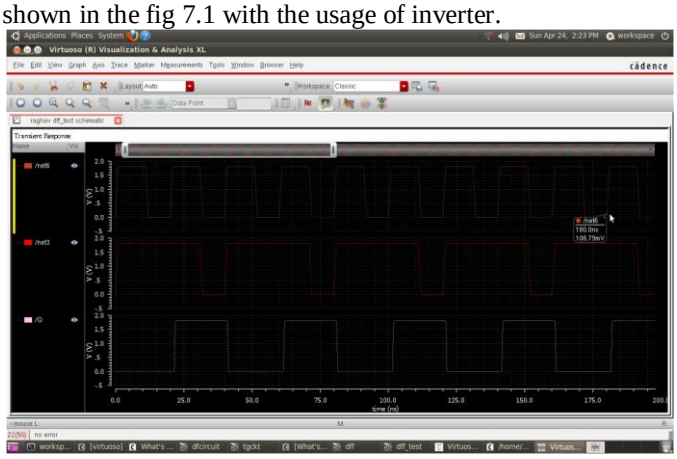

Fig 7.4: Output waveform of master slave D-latches

The fig 7.6 is the output waveform of the pre-scale divider circuit, where the given input signal of 100Hz is divided in to the factor of 2,4,8,12. The tabular column below in Fig 7.5 shows the obtained waveform frequencies of the different stages of pre-scale which are connected to the different peripherals of the devices with respect to the threshold voltage of the peripherals.

Input freq.	Factor 2	Factor 4	Factor 8	Factor 12
100 Hz	50 Hz	25 Hz	12.5 Hz	8.33 Hz
1 GHz	0.5 GHz	0.25 GHz	0.125 GHz	0.083 GHz

Fig 7.5: pre-scale division frequency Table.

In the fig 7.6 the input frequency of 100 Hz gives the frequencies with respect to the prescale stages by the factor of 2,4,8,12. Usually the input frequency is selected on the basis of the oscillator used and the prescale stages are enabled on the basis of the requirement of the peripherals which are used in the device or the circuitry.

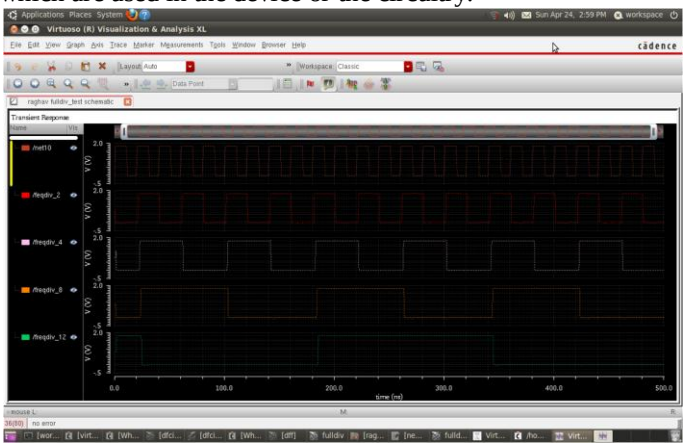

Fig 7.6: Output waveform of the pre-scale divider by the stage of 2,4,8,12.

VIII. CONCLUSION

The DFAL and TG fundamentals are efficient in implementation of the D-latch. The implementation of the DFAL inverter based frequency divider with the extension to implement the pre-scale division circuit for the f/2 , f/4 , f/8, f/12 stages which are implemented and the results are obtained in the wave forms and simulations. This technique will improve the performance of the circuit and also the operation speed. Since we used a master slave architecture will give a regenerating effect.

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