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DESIGN OF RELIABLE MULTIPLIER USING ADAPTIVE HOLD LOGIC

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Abstract: The semiconductor technology and therefore the decreasing of device geometries square measure increasingly increases: the ensuing processors square measure more and more changing into vulnerable to effects like aging and soft errors. As number ages, the semiconductor unit shift time can increase and its electrical characteristics scale back. Hence, supported the turnout of the number style, the general performance of the digital filters depends. Aging downside of semiconductor unit has important result on the performance of those digital systems and in long run, the system could fail attributable to delay issues. Hence, the processor or number cannot continue error free operation at an equivalent clock frequency and/or voltage that it had been originally designed. So, to scale back such effects, recent analysis proposes to supply processors with special electronic equipment that mechanically modify its circuit level temporal order properties. From the attitude of tasks running on these processors, by mistreatment over style approaches, aging result will be reduced, however these approaches ends up in space unskillfulness. And conjointly temporal order violations occur once mounted latency styles square measure used. This must be analyzed rigorously, notably within the context of laborious real time. during this paper we have a tendency to propose a reliable number mistreatment AHL during which, aging iatrogenic degradation and changes in temporal order properties of the processor, once planning laborious real time systems. particularly, by taking a time period constraint of the system into consideration we have a tendency to address the schedulability and task mapping downside. In alternative words, till a given minimum amount of your time (i.e., life time) the system style to be absolutely operational (i.e., meet all deadlines). The experimental results show that our planned design with thirty two ×32 and sixty four ×64 changed booth multipliers mistreatment AHL. The Verilog language is employed for coding; synthesis was done by mistreatment Xilinx ISE

Keywords: Adaptive hold logic (AHL), negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), reliable multiplier, variable latency.

I. INTRODUCTION

Due to aggressive scaling of device geometries continues to diminish with the developments in fabrication technology, the ensuing processors square measure progressively changing into vulnerable to effects like aging. moreover, negative bias temperature instability (NBTI) happens once a PMOS junction transistor is beneath negative bias, ends up in aging result. Aging result degrades junction transistor speed by increase in threshold voltage, which ends up in real time delay issues. The corresponding result on associate nMOS junction transistor is positive bias temperature instability (PBTI), that happens once associate nMOS junction transistor is beneath positive bias.

Integrated-circuit aging phenomena discovered in sub-90nm CMOS technologies square measure as follows:-

1.1. Hot Carrier Injection (HCI).
1.2. Time-Dependent insulator Breakdown (TDDB).
1.3. Bias Temperature Instability (BTI).
1.4. Electro-migration (EM).

1.1. Hot Carrier Injection (HCI)

Hot carriers square measure particles that get a awfully high K.E. from being accelerated in a very high field. These energetic carriers may be injected into `forbidden' region of the device like the gate compound, rather than following their meant mechanical phenomenon. once injected into such a vicinity they will get treed or cause the generation of interface states. These defects successively result in shifts within the electrical characteristics of the semiconductor unit like a shift of the Vth, this issue β and also the output electrical phenomenon go.

The degradation of integrated circuits as a result of Hot Carrier Injection (HCI) comes into existence as a result of the continual scaling of semiconductor unit dimensions while not related provide voltage reduction. The circuit operational voltage was born to scale back power consumption and stratified drain junctions were introduced to resolve dependability issues. Hence, HCI became less of a problem. HCI will still be a drag since provide voltage scaling is deceleration down due to the non-scalability of the sub-threshold slope. HCI is primarily a drag in nMOS devices. though pMOS devices square measure less sensitive to HCI, the result will enhance alternative aging effects like negative bias temperature instability (NBTI).

1.2 Time-Dependent Dielectric Break-down (TDDB)

The correct operation of a MOS semiconductor unit|electronictransistor|semiconductor device|semiconductor unit|semiconductor} depends on the insulating properties of the stuff layer below the gate conductor of the transistor. every stuff material encompasses a most field of force within which it will sustain. once a bigger field of force is applied, this ends up in arduous Breakdown (HBD). HBD is a particularly native development, characterised by a loss of the gate compound insulating properties and permitting an outsized gate current to flow. At lower electrical fields, the stuff will wear-out when a while and at last break down fully. this can be known as Time-Dependent stuff Breakdown (TDDB).

1.3 Bias Temperature Instability (BTI):-

Bias Temperature Instability (BTI) has gained plenty of attention because of its more and more adverse impact in nano-meter CMOS technologies. it's a threshold voltage (Vth) shift once a bias voltage has been applied to a MOS gate at elevated temperature. It causes threshold voltage (Vth) increments to the MOS transistors. Threshold voltage Vth increment during a exceedingly|in a very} pMOS semiconductor|electronic transistor|semiconductor device|semiconductor unit|semiconductor} that happens underneath the negative gate stress is remarked as Negative Bias Temperature Instability (NBTI) and therefore the one that occur in an nMOS transistor underneath positive gate stress is thought as Positive Bias Temperature Instability (PBTI). The NBTI or PBTI impact will become a lot of important reckoning on the material kind. For a MOS semiconductor unit, there square measure 2 BTI phases.

a. Stress part.

b. Relaxation part.

These 2 phases dissent by the gate biasing (i.e. VDD or –VDD) of the MOS transistors.

1.4. Electro-migration (EM)

Electro-Migration (EM) is associate degree aging impact going down in interconnect wires, contacts associate degreed vias in an computer circuit. The impact causes material transport by gradual movement of the ions during a conductor because of the momentum transfer between conducting electrons and therefore the diffusive metal atoms. EM is very important in applications wherever high electricity densities area unit used. These aging effects area unit caused because of scaling of transistors in VLSI chips. The device aging causes loss on circuit performance and lifelong that area unit the most factors within the responsibility degradation of VLSI circuit. Thus, to cut back this aging impact on CMOS, associate degree adaptive Hold Logic (AHL) circuit is based to be a lot of economical than different ways

II. LITERATURE SURVEY

A traditional technique to mitigate the aging impact is overdesign, together with such things as guard-banding AND circuit oversizing; but, this approach are often terribly hopeless and space and power inefficient.To avoid this drawback, several NBTI-aware methodologies are projected. associate degree NBTI-aware technology mapping technique to ensure the performance of the circuit throughout its time period. In, associate degree NBTI-aware sleep semiconductor device was designed to scale back the aging effects on pMOS sleep-transistors, and also the time period stability of the power-gated circuits into consideration was improved. Wu and Marculescu projected a joint logic restructuring and pin rearrangement technique, that is predicated on detective work practical symmetries and semiconductor device stacking effects. They conjointly projected associate degree NBTI improvement technique that thought-about path sensitization and, dynamic voltage scaling and body-basing techniques were projected to scale back power or extend circuit life. These techniques, however, need circuit modification or don't offer improvement of specific circuits. ancient circuits use important path delay because the overall circuit clock cycle so as to perform properly.

However, the likelihood that the important methods square measure activated is low. In most cases, the trail delay is shorter than the important path. For these noncritical methods, victimization the important path delay because the overall cycle amount can lead to important temporal arrangement waste. Hence, the variable-latency style was projected to scale back the temporal arrangement waste of ancient circuits. The variable-latency style divides the circuit into 2 parts: 1) shorter methods and 2) longer methods. Shorter methods will execute properly in one cycle, whereas longer methods want 2 cycles to execute. once shorter methods square measure activated oftentimes, the common latency of variable-latency styles is best than that of ancient styles. for instance, many variable-latency adders were projected victimization the speculation technique with error detection and recovery. a brief path activation operate rule was projected in to boost the accuracy of the hold logic and to optimize the performance of the variable-latency circuit. associate degree instruction planning rule was projected in [17] to schedule the operations on non uniform latency practical units and improve the performance of terribly Long Instruction Word processors. In [19], process-variation tolerant design for arithmetic units was projected, wherever the impact of process-variation is taken into account to extend the circuit yield. additionally, the important methods square measure divided into 2 shorter methods that might be unequal and also the clock cycle is about to the delay of the longer one. These analysis styles were ready to scale back the temporal arrangement waste of ancient circuits to boost performance, however they didn't think about the aging impact and will not modify themselves throughout the runtime. A variable-latency adder style that considers the aging impact was projected in [20]. However, no variable-latency number style that considers the aging impact and might modify dynamically has been done. Traditional circuits square measure supported mounted latency style. In mounted latency style, important path delay because the overall circuit clock cycle so as to perform properly. However, the likelihood that the important methods square measure activated is low. For these noncritical methods, victimization the important path delay because the overall cycle amount can lead to important temporal arrangement waste. Hence, the variable-latency style was projected to re-leader the temporal arrangement waste of ancient circuits. In variable- latency style, shortest methods square measure assigned to be dead among one cycle and longest methods among 2 or additional cycle. once shorter methods square measure activated oftentimes, the common latency of variable-latency styles is best than that of mounted latency styles. Main objective of the work is to style a digital filter victimization low power variable latency number with AH logic. Low power variable latency number is meant therefore on guarantee minimum performance degradation. because the processor ages, it now not ready to sustain the originally designed clock frequency: therefore the switch times of the semiconductor device will increase. a number of the

Hardware solutions to scale back such effects incorporates processors with on-chip monitors or sensors that live the temporal arrangement margin obtainable to circuits on the chip, or variations in their temporal arrangement behavior arising from changes in their electrical characteristics. The output from such monitors is as well as the clock generation circuit to regulate the clock frequency in response to changes within the signal propagation delay thanks to effects like aging. Such techniques have already been utilized in IBM's POWER7 design so as to mechanically modify the processor's clock frequency and voltage level, with the aim of saving energy. constant technique is additionally applicable to deal with the consequences of aging.

Our contributions:
In this paper, we tend to propose the look of reliable number with novel accommodative hold logic (AHL) circuit. The number is predicated on the variable-latency technique and may change the AHL circuit to attain reliable operation below the influence of NBTI and PBTI effects. To be specific, the contributions of this paper square measure summarized as follows:

1) Novel variable-latency number design with associate AHL circuit. The AHL circuit will decide whether or not the input patterns need one or 2 cycles and may change the decision making criteria to make sure that there's minimum performance degradation once right smart aging happens

2) A reliable number style methodology that's appropriate for giant multipliers. The previous numbers square measure designed with sixteen bit or thirty two bit multiplier. In planned model the number is regarding sixty four bit.

3)The existing system incorporates Column or Row bypassing number victimisation AHL and during this system is planned by victimisation changed Booth number which provides higher outturn.

III. PRELIMINARIES

Variable-Latency Design
The basic thought is to execute a shorter path employing a shorter cycle and longer path victimization 2 cycles. Since most ways execute in an exceedingly cycle amount that's abundant smaller than the essential path delay, the variable-latency style has smaller average latency. For example, Fig. four is AN 8-bit variable-latency ripple carry adder (RCA). A8–A1, B8–B1 area unit 8-bit inputs, and S8–S1 area unit the outputs.

Supposing the delay for every solfa syllable is one, and also the most delay for the adder is eight. Through simulation, it may be determined that the likelihood of the carry propagation delay being longer than five is low. Hence, the cycle amount is about to five, and hold logic is other to send word the system whether or not the adder will complete the operation among a cycle amount.

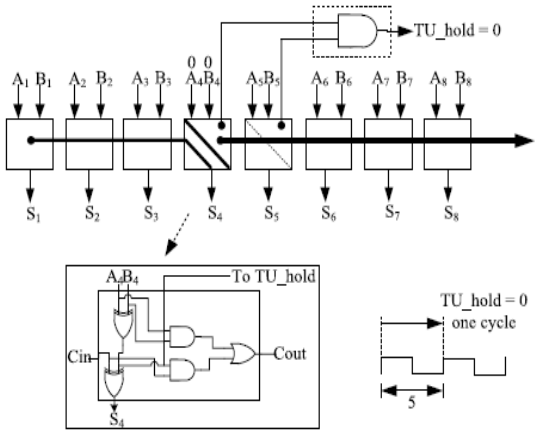


Fig. 1. 8-bit RCA with a hold logic circuit.

Fig. one shows the hold logic that's utilized in this circuit. The operate of the hold logic is (A4 XORB4)(A5 XORB5). If the output of the hold logic is zero, i.e., A4=B4orA5=B5, either the fourth or the fifth adder won't manufacture a carryout. Hence, the most delay are going to be but one cycle amount. once the hold logic output is one, this suggests that the input will activate ways longer than five, that the hold logic notifies the system that this operation needs 2 cycles to finish. 2 cycles square measure spare for the longest path to finish (5 * a pair of is larger than 8).
The performance improvement of the variable-latency style is calculated as follows: if the chance of every input being one is zero.5, the chance of (A4 XORB4) (A5 XORB5) being one is zero.25. the typical latency for the variable-latency style is zero.75∗5+0.25∗10=6.25. Compared with the straightforward fixed-latency RCA, that has a median latency of eight, the variable-latency style are able to do a twenty eighth performance improvement. The path delay distribution of a 16×16 AM and for each ancient|a standard|a conventional} column-bypassing and traditional row-bypassing multiplier factor with sixty five 536 indiscriminately chosen input patterns square measure shown. All multipliers execute operations on a set cycle amount. the most path delay is one.32 ns for the AM, 1.88 ns for the column-bypassing multiplier factor, and 1.82 ns for the row-bypassing multiplier factor. It is seen that for the AM, over ninety eight of the ways have a delay of<0.7 ns. Moreover, over ninety three and ninety eight of the ways within the FLCB and row-bypassing multipliers gift a delay of <0.9 ns, severally. Hence, victimization the most path delay for all ways can cause important temporal order waste for shorter ways, and redesigning the multiplier factor with variable latency will improve. Their performance Associate in Nursingother key observation is that the trail delay for an operation is powerfully tied to the amount of zeros within the numbers within the column-bypassing multiplier factor. Fig. half-dozen shows the delay distribution of the 16×16 column-bypassing multiplier factor below 3 totally different numbers of zeros within the multiplicands: 1) 6; 2) 8; and 3) ten. 3 thousand indiscriminately elect patterns square measure utilized in every experiment. It is seen because the variety of zeros within the multiplicands will increase, delay

distributions left shifted, and average delay is reduced. the rationale for this is often the number is employed because the choose line for column-bypassing multipliers, and if additional zeros exist within the, multiplicand, additional FAs are going to be skipped, and therefore the total bit from the higher solfa syllable is passed to the lower solfa syllable, reducing the trail delay. Note that similar experiments also are in hot water row-bypassing multipliers. However, as a result of the results square measure similar, they're not shown to avoid duplications. For a changed booth multiplier factor, the multiplicators square measure accustomed verify whether or not a pattern desires one cycle or 2 cycles to finish Associate in Nursing operation as a result of the multiplicator is employed because the choose line. This makes the multiplier factor glorious candidates for the variable latency style since we will merely examine the amount of zeros within the number or multiplicator to predict whether or not the operation needs one cycle or 2 cycles to finish.

Modified booth multiplier

Modified booth multiplier factor is employed to cut back the partial merchandise by [*fr1]. it'd cut back the amount of 1's in multiplier factor. The previous multipliers still have to be compelled to look ahead to the important path, e.g., the shift and add delay in sequent multiplier factor. thus it doesn't save speed.

Modified Booth to provide at the most n/2+1 partial merchandise.

- Algorithm: (for unsigned numbers)

1. Pad the LSB with one zero.
2. Pad the mutual savings bank with two zeros if n is even and one zero if n is odd.
3. Divide the multiplier factor into overlapping teams of 3-bits.
4. verify partial product multiplier factor from changed booth two cryptography table.
5. reckon the number Multiples
6. add Partial merchandise

allow us to contemplate the multiplication of 2's complement varietys X and Y with every number consisting of n=2k bits. The number Y will be described in changed Booth type. the fundamental plan is that rather than shifting and adding for each column of the multiplier factor term and multiplying by one or zero, we tend to solely take each second column , and multiply by +1, +2, or 0, to get same results.

The encoded output will be calculated by the below formula as shown in table

$Y_{j\,MB} = -2\,Y_{2j+1} + Y_{2j} + Y_{2j-1}$

Input				Encoded output		
Y_{2j+1}	Y_{2j}	Y_{2j-1}	Y_j^{MB}	sj	oj	2j
0	0	0	0	0	0	0
0	0	1	+1	0	1	0
0	1	0	+1	0	1	0
0	1	1	+2	0	0	1
1	0	0	-2	1	0	1
1	0	1	-1	1	1	0
1	1	0	-1	1	1	0
1	1	1	0	1	0	0

Table 1: Modified Booth Recoding Table

IV. PROPOSED RELIABLE MULTIPLIER (MODIFIED BOOTH MULTIPLIER) USING AHL

Proposed Architecture

Fig. 5 shows our Proposed Reliable Multiplier (Modified Booth Multiplier) using AHL architecture, which includes two m-bit inputs (mis a positive number), one 2m-bit output, one modified booth multiplier multiplier, 2m1-bit Razor flip-flops [27], and an AHL circuit.

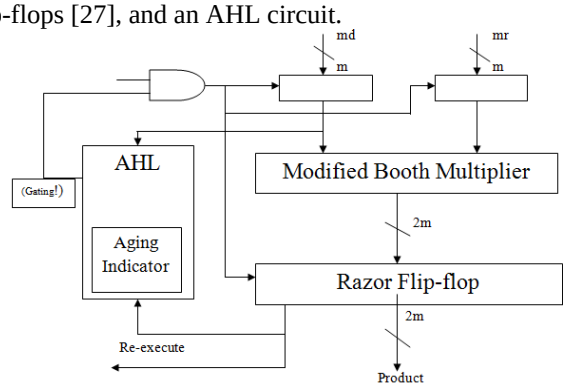


Fig. 2. Proposed architecture (md means multiplicand; mr means multiplicator).

Razor flip-flops can be used to detect whether timing violations occur before the next input pattern arrives.

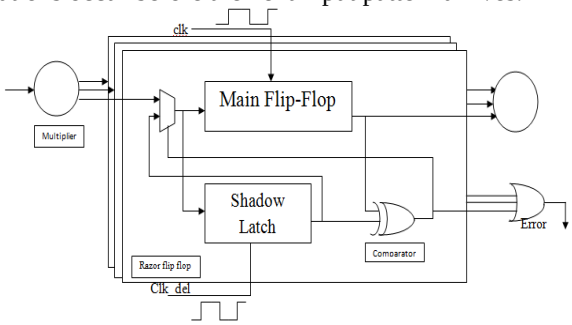


Fig. 3. Razor flip flops

Fig. three shows the main points of Razor flip-flops. A 1-bit Razor flip-flop contains a main flip-flop, shadow latch,XORgate, and mux. the most flip-flop catches the execution result for the mixture circuit employing a traditional clock signal, and therefore the shadow latch catches the execution result employing a delayed clock signal, that is slower than the conventional clock signal. If the fast little bit of the shadow latch is totally different from that of the most flip-flop, this implies the trail delay of the present operation exceeds the cycle amount, and therefore the main flip-flop catches AN incorrect result. If errors occur, the Razor flip-flop can set the error signal to one to inform the system to reexecute the operation and inform the

AHL circuit that a mistake has occurred. we tend to use Razor flip-flops to notice whether or not AN operation that's thought-about to be a one-cycle pattern will extremely end in an exceedingly cycle. If not, the operation is reexecuted with 2 cycles. though the reexecution could appear pricey, the value is low as a result of the reexecution frequency is low.

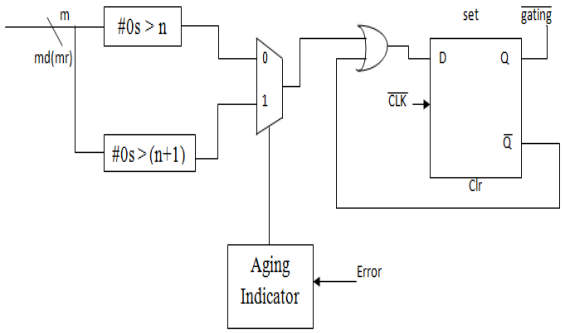


Fig. 4. Diagram of AHL (md means multiplicand; mr means multiplicator).

The AHL circuit is that the key element within the aging-ware variable-latency number. Fig. four shows the small print of the AHL circuit. The AHL circuit contains AN aging indicator, 2 judgment blocks, one mux, and one D flip-flop. The aging indicator indicates whether or not the circuit has suffered important performance degradation as a result of the aging result. The aging indicator is enforced in an exceedingly easy counter that counts the {amount|the quantity} of errors over a precise amount of operations and is reset to zero at the top of these operations. If the cycle amount is simply too short, the number isn't ready to complete these operations with success, inflicting temporal order violations. These temporal order violations are going to be caught by the Razor flip-flops, that generate error signals. If errors happen oftentimes and exceed a predefined threshold, it means that the circuit has suffered important temporal order degradation as a result of the aging result, and therefore the aging indicator can output 1; otherwise, it'll output zero to point the aging result continues to be not important, and no actions ar required. In existing system Row Bypassing number and Column Bypassing number victimisation AHL is employed to mitigate the delay and to extend the outturn of the device. By victimisation planned System i.e., changed Booth number victimisation AHL: far more delay and power are often reduced. thence reliable number is intended. The comparisons of delay of Row bypassing number victimisation AHL, Column bypassing number victimisation AHL and changed booth number victimisation AHL is shown in below graph (fig:5). Here the changed booth number victimisation AHL provides lesser delay compared to others. Here the delay in planned system of sixteen bit and thirty two bit is shrunken by twelve months and thirty first compared to the sixteen bit and thirty two bit column bypassing number victimisation AHL. Power is shrunken by 4 wheel drive and forty eighth. And space is inflated by thirty.4% and 33.7% severally. though the space will increase the reliable outturn is obtained and main constraints like delay and power ar satisfied.

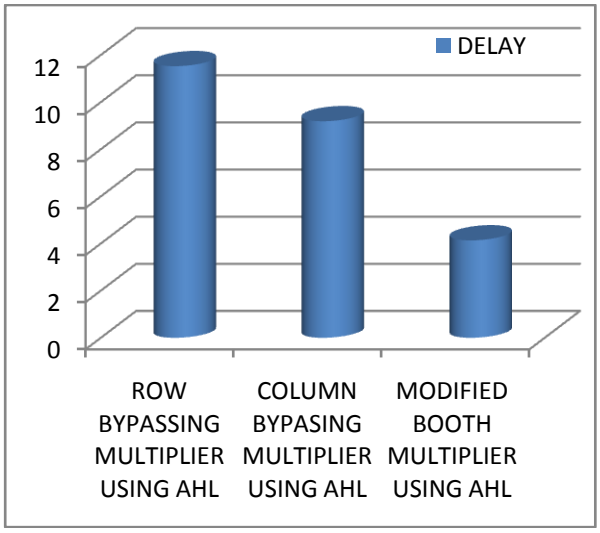


Fig 5: comparison of delays of Row bypassing multiplier using AHL, Column bypassing multiplier using AHL, Modified booth multiplier using AHL.

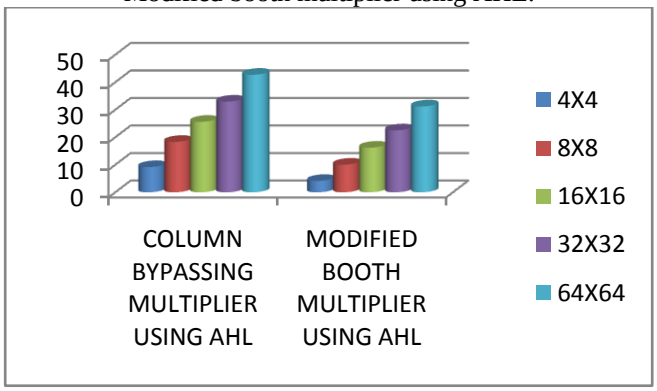


Fig 6: Comparison of delays of 4 bit, 8 bit, 16 bit, 32 bit, 64 bit Column bypassing multiplier using AHL with 4 bit, 8 bit, 16 bit, 32 bit, 64 bit Modified booth multiplier using AHL respectively

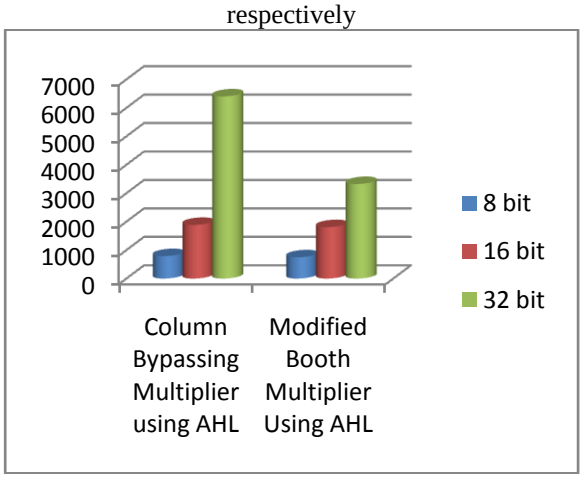


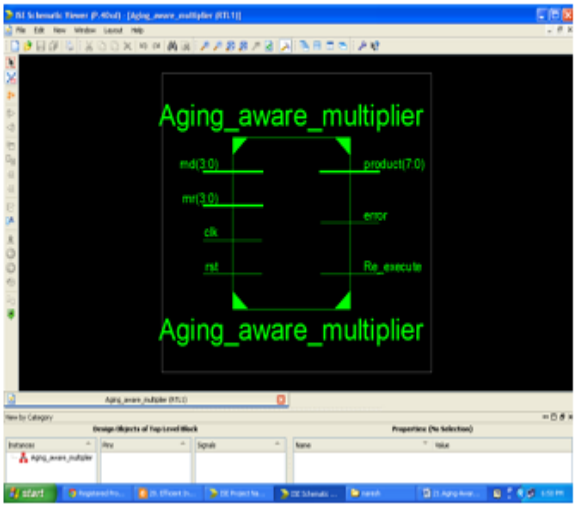
Fig 7: Comparison of Power of 8 bit, 16 bit, 32 bit Column bypassing Multiplier using AHL with 8 bit, 16 bit, 32 bit Modified booth multiplier respectively.

	COLUMN BYPASING MULTIPLIER USIING AHL 16 BIT	COLUMN BYPASSING MULTIPLIER USING AHL 32 BIT	MODIFIED BOOTH MULTIPLIER USING AHL 16 BIT	MODIFIED BOOTH MULTIPLIER USING AHL 32 BIT
DELAY (ns)	25.631	32.96	16.222	22.504
POWER (W)	1.88681	6.40384	1.80771	3.32382
AREA(Gate count)	1197	4706	1561	6295

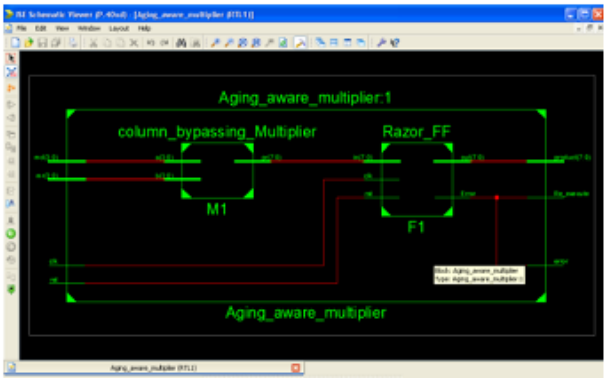
Table 2: Comparison of delay, power and area of 16 bit and 32 bit Column bypassing multiplier using AHL with 16 bit and 32 bit Modified booth multiplier using AHL

V. SIMULATION RESULTS

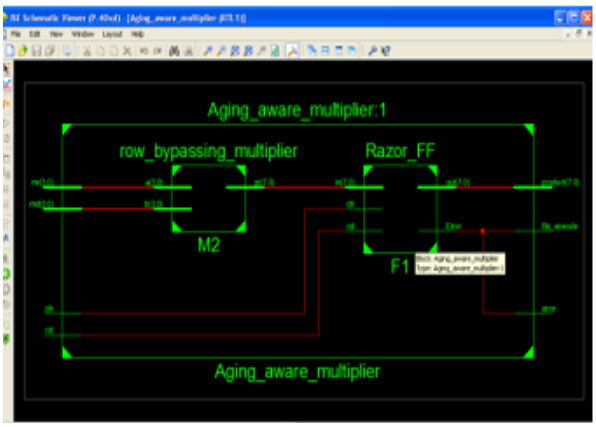
Block diagram



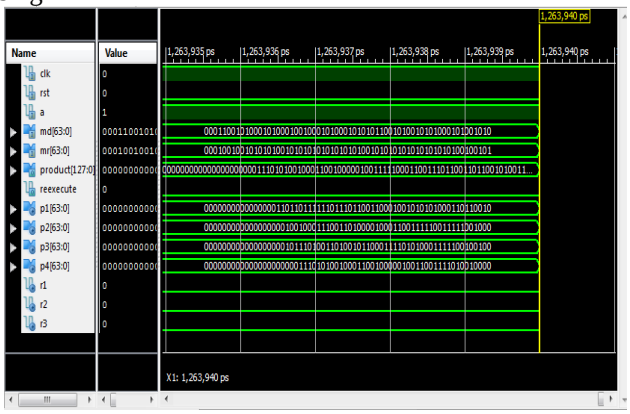
RTL Schematic diagram



Technology schematic



Simulation waveform of 64- bit modified booth multiplier using AHL



VI. CONCLUSION

This paper planned associate degree aging-aware variable-latency multiplier factor style with the AHL. the planning of Reliable multiplier factor victimisation AHL is planned. The multiplier factor is ready to produce higher output i.e., delay and power were minimized. The multiplier factor is ready to regulate the AHL to mitigate performance degradation because of redoubled delay. For reliable operation changed Booth multiplier factor is employed. Here the planned reliable multiplier factor i.e., sixty four bit changed booth multiplier factor victimisation AHL compared with sixty four bit column bypassing multiplier factor victimisation AHL the delay is minimized by twenty six.9%. And additionally power is minimized by 48%in thirty two bit multiplier factor severally.

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