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VLSI DESIGN OF A NOVEL LP-LFSR BASED PROGRAMMABLE PRPG ARCHITECTURE

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Abstract: ***This paper describes a low-power (LP) programmable generator capable of reducing pseudorandom take a look at patterns with desired toggling levels and increased fault coverage gradient compared with the best-to-date intrinsically self-test (BIST)- primarily based pseudorandom take a look at pattern generators. It's comprised of a linear finite state machine (a linear feedback register or a hoop generator) driving associate degree applicable section shifter, and it comes with variety of options permitting this device to supply binary sequences with preselected toggling (PRESTO) activity. We tend to introduce a technique to mechanically choose many controls of the generator providing straightforward and precise calibration. Identical technique is afterwards used to deterministically guide the generator toward take a look at sequences with improved fault-coverage-to pattern-count ratios. Moreover, this paper proposes associate degree disc take a look at compression technique that permits shaping the take a look at power envelope during an absolutely certain, accurate, and versatile fashion by adapting the PRESTO-based logic BIST (LBIST) infrastructure. The projected hybrid theme expeditiously combines take a look at compression with LBIST, wherever each technique will work synergistically to deliver top quality tests. Experimental results obtained for industrial styles illustrate the practicableness of the projected take a look at schemes and are rumored herein.***

I. INTRODUCTION

Although over successive years, the first objective of producing take a look at can stay ssentially an equivalent to confirm reliable and prime quality semiconductor merchandise conditions and consequently additionally take a look at solutions could endure a major evolution. The semiconductor –ctortechnology, style characteristics, and also the style method area unit among the key factors that may impact this evolution. With new sorts of defects that one can have to be compelled to concede to give the specified take a look at quality for successive technology nodes like 3D, it's applicable to create the question of what matching design-for-test (DFT) ways can ought to be deployed. Take a look at compression, introduced a decade agone, has quickly become the most stream DFT methodology. However, it's unclear whether or not take a look at compression are going to be capable of managing the fast rate of technological changes over successive decade. Curiously, logic integral self-test (LBIST), originally developed for board, system, and in-field take a look at, is currently gaining acceptance for production take a look at because it provides terribly strong DFT and is employed more and more usually with take a look at compression. This hybrid approach looks to be successive logical biological process step in DFT. It's potential for improved take a look at quality; it should augment the talents to run at-speed power aware tests, and it will scale back the price of producing take a look at whereas protective all LBIST[1] and scan compression benefits. Tries to beat the bottleneck of take a look at knowledge information measure between the take a look ater and also the chip have created the conception of mixing LBIST and test knowledge compression an important analysis and development space. particularly, many hybrid BIST schemes store settled indefinite quantity patterns (used to sight random pattern resistant faults) on the tester in an exceedingly compressed type, then use the prevailing BIST hardware to decompress these take a look at patterns Some solutions enter settled stimuli byvictimization compressed weights or by heavy pseudorandom vectors in numerous fashions varied schemes for power reduction throughout scan testing are devised Among them, there area unit solutions specifically planned for BIST to stay the common and peak power below a given threshold. As an example, the take a look at power will be reduced by preventing transitions at memory parts from propagating to combinable logic throughout scan shift. This is often achieved by inserting gating logic between scan cell outputs and logic they drive during this paper, we tend to propose a PRPG for record BIST applications. The generator primarily aims at reducing the switch activity throughout scan loading attributable to its preselected toggling (PRESTO) levels. This paper culminates in showing that the fast generator may also with success act as a take a look at knowledge decompressor, therefore permitting one to implement a hybrid take a look at methodology that mixes LBIST and ATPG-based embedded take a look at compression.

II. BASIC ARCHITECTURE

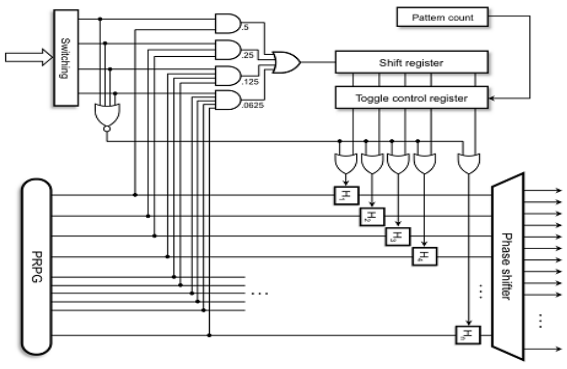

Fig.1.basic architecture of PRESTO generator.

Fig. one shows the fundamental structure of a fast generator. Associate n-bit PRPG connected with a part shifter feeding scan chains [2] forms a kernel of the generator manufacturing the particular pseudorandom check patterns. A linear feedback register or a hoop generator will implement a PRPG. a lot of significantly, however, n hold latches area unit placed between the PRPG and also the part shifter. Every hold latch is {individually|separately|singly|severally|one by one|on associate individual basis} management led via a corresponding stage of an n-bit toggle control register. As long as its alter input is declared, the given latch is clear for information going from the PRPG to the part shifter, and it's aforementioned to be within the toggle mode. Once the latch is disabled, it captures and saves, for variety of clock cycles, the corresponding little bit of PRPG, therefore feeding the part shifter (and probably some scan chains) with a relentless price. it's currently within the hold mode. it's price noting that every part shifter output is obtained by XOR-ing outputs of 3 completely different hold latches. Therefore, each scan chain remains in a very low-power [3] mode provided solely disabled hold latches drive the corresponding part shifter output. As mentioned antecedently, the toggle management register supervises the holdlatches. Its content contains 0s and 1s, wherever 1s indicate latches within the toggle mode, so clear for knowledge returning from the PRPG. Their fraction determines a scan shift activity. The management register is reloaded once per pattern with the content of an extra register. The change signals injected into the register area unit made in an exceedingly probabilistic fashion by mistreatment the first PRPG with a programmable set of weights. The weights area unit determined by four AND gates manufacturing 1s with the chance of zero.5, 0.25, 0.125, and 0.0625, severally. The OR circuit permits selecting possibilities on the far side straightforward powers of two. A 4-bit register shift is used to activate AND gates andpermits choosing a user-defined level of shift activity.
It will correspond to a precise level of toggling within the scan chains. With solely fifteen totally different shift codes, however, the offered toggling coarseness might render this answer too coarse to be invariably acceptable. Section III presents further options that build the fast generator absolutely operational in an exceedingly big selection of desired shift rates.

III. FULLY OPERATIONAL GENERATOR

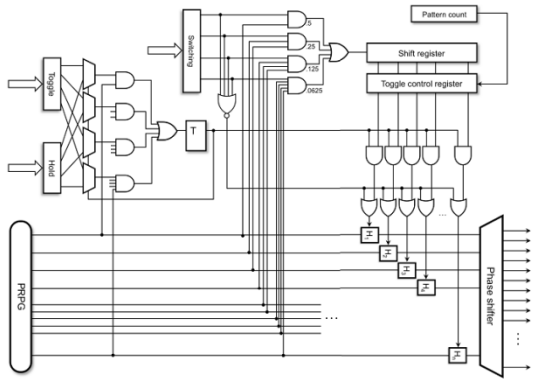

Fig. 2.Fully operational version of PRESTO.

Much higher flexibility in forming low-toggling take a look at patterns is achieved by deploying a theme given in Fig. 2. Basically, whereas conserving the operational principles of the fundamental resolution, this approach splits up a shifting amount of each take a look at pattern into a sequence of alternating hold and toggle intervals. To maneuver the generator back and forth between these 2 states, we have a tendency to use a T-type flip-flop that switches whenever there's a one on its knowledge input. If it's set to zero,

The generator enters the hold amount with all latches quickly disabled no matter the management register content. This is often accomplished by inserting AND gates on the management register outputs to permit freeze of all part shifter inputs. This property is crucial in SoC styles wherever solely one scan chain crosses a given core, and its abnormal toggling could cause regionally unacceptable cooling which will solely be reduced owing to temporary hold periods. If the T flip-flop is about to one (the toggle period), then the latches enabled through the management register will pass take a look at knowledge moving from the PRPG to the scan chains.

Two further parameters unbroken in 4-bit Hold and Toggle registers confirm however long the whole generator remains either within the hold mode or within the toggle mode, severally. To terminate either mode, a one should occur on the T flip-flop input. This weighted pseudorandom signal is created in a very manner just like that of weighted logic accustomed feed the register. The T flip-flop controls additionally four 2-input multiplexers routing knowledge from the Toggle and Hold registers. It permits choosing a supply of management knowledge which will be utilized in subsequent cycle to probably modification the operational mode of the generator. as an example, once within the toggle mode, the input multiplexers observe the Toggle register. Once the weighted logic outputs one, the flip-flop toggles, and as a result all hold latches freeze within the last recorded state. They’re going to stay during this state till another one happens on the weighted logic output. The random incidence of thisevent is currently associated with the content of the Hold register that determines once to terminate the hold mode.

A scan change profile once deploying the fast generator in a very hypothetic atmosphere with fifteen scan chains is shown in Fig. three for 2 take a look at patterns. Blue (0s) and red (1s) stripes frame the low power-toggling pattern, whereas grey areas correspond to periods of toggling. All-blue and all-red scan chains [7] area unit fed by the constant values solely. Note that their quantity doesn't amendment between patterns tho' they're not precisely the same in every case. As are often seen, check patterns area unit divided into hold and toggle intervals of random length, whereas LP scan chains stay still for the whole period of one check pattern [5]

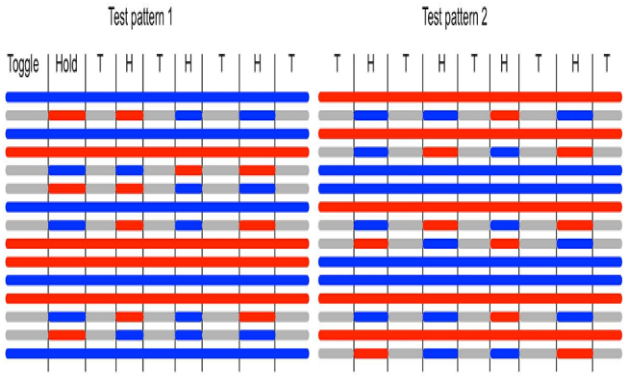

Fig.3. Switching activity in scan chains

IV. LP DECOMPRESSOR

In order to facilitate take a look at information decompression whereas protective its original practicality, the electronic equipment of Fig. two should be rearchitected. This is often shown in Fig. 8. The core principle of the decompressor [8] is to disable each weighted logic blocks (V and H) and to deploy settled management information instead. Particularly, the content of the toggle management register will currentlybe elect in an exceedingly settled manner attributable to a electronic device placed before of the register. What is more, the Toggle and Hold registers area unit utilized to alternately predetermine a 4-bit binary down counter, and so to work out durations of the hold and toggle phases. once this circuit reaches the worth of zero, it causes a passionate signal to travel high so as to toggle the T flip-flop. Constant signal permits the counter to own the input file unbroken within the Toggle or Hold register entered because the next state. Both the down counter and also the T flip-flop have to be compelled to be initialized each take a look at pattern. The initial worth of the T flipflop decides whether or not the decompressor can begin to work either within the toggle or within the hold mode, whereas the initial worth of the counter, any stated as associate degree offset, determines that mode's period. As will be seen, practicality of the T flip-flops remains constant as that of the disc PRPG (see Section III) however 2 cases. 1st of all, the cryptography procedure might utterly disable the hold part (when all hold latches area unit blocked) by loading the Hold register with associate degree applicable code, as an example, 0000. If detected (No Hold signal within the figure), it overrides the output of the T flip-flop by exploitation anextra logic gate, as shown in Fig. 8. As a result, the whole take a look at pattern goes to be encoded among the toggle mode solely. Additionally, all hold latches got to be properly initialized. Hence, an impression signal 1st cycle made at the tip of the ring generator data format part reloads all latches with the present content of this a part of the decompressor. Finally, external Ate channels (feeding the initial PRPG) permit one to implement a continual flow take a look at information decompression paradigm like the dynamic LFSR reseeding. Given the scale of PRPG[4], the amount of scan chains and also the corresponding part shifter, the shift code, the offset, furthermore because the values unbroken within the Toggle and Hold registers, the whole decompressor can manufacture settled (decompressed) take a look at patterns having a desired level of toggling provided the scan chains area unit balanced.[6]

Low power LFSR

The low power pattern generation algorithm is coded using Hardware Descriptive Language (HDL) labeled Verilog with initial seed vector loaded as pre-initial stage to the TPG. An 8-bit low power Test – Pattern Generator (TPG) composed of extrinsic XOR based Linear Feedback Shift Register (LFSR) along with an appended combinational logic to produce low power test vectors. Combinational logic consists of logic blocks andmultiplexers (MUX)connected to the output of D – Flip flops in LFSR. The internal architecture of logic block is very simple, it consists of an AND gate and an OR gate with their output connected to the inputs of MUX. The intent behind generating low power pattern is to reduce total number of bit flips between successive test patterns which avoids maximum transitions at the inputs of Circuit under Test (CUT) leading to slenderize switching activity inside CUT. The technique implies LFSR with an additional circuitry is utilized to accomplish the generation of low power [9] test vectors by inserting intermediate patterns between successive test vectors.

V. SIMULATION RESULTS

LP LFSR

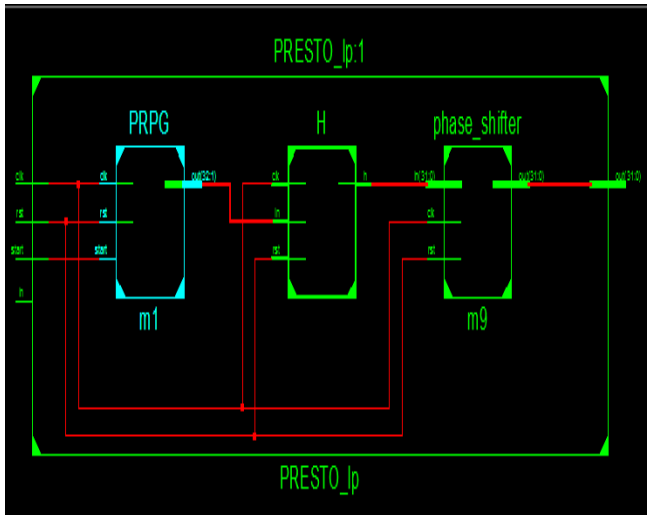

Fig. 4 RTL Schematic

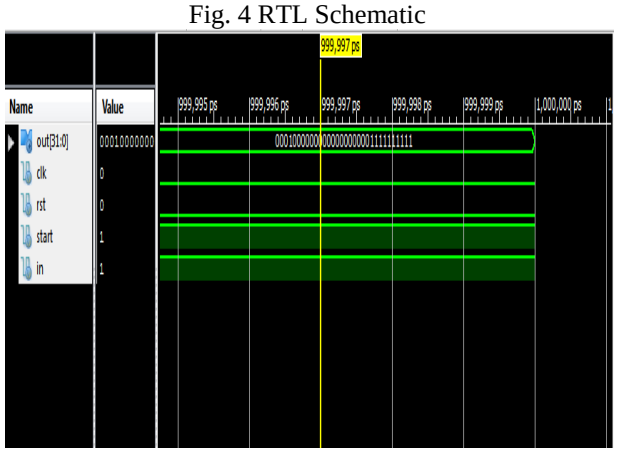

Fig.5 Simulation results

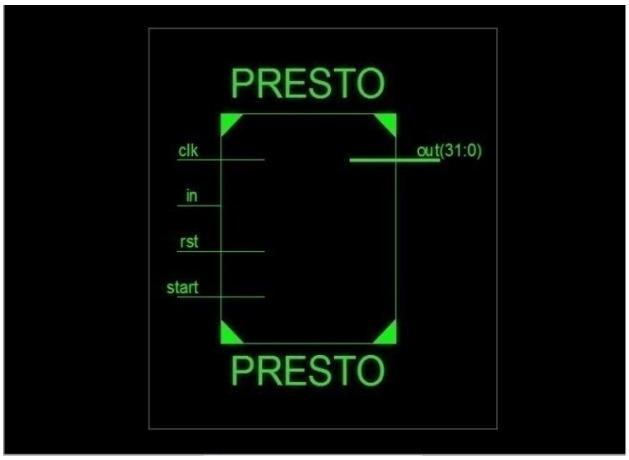

Fig. 6 Presto RTL block

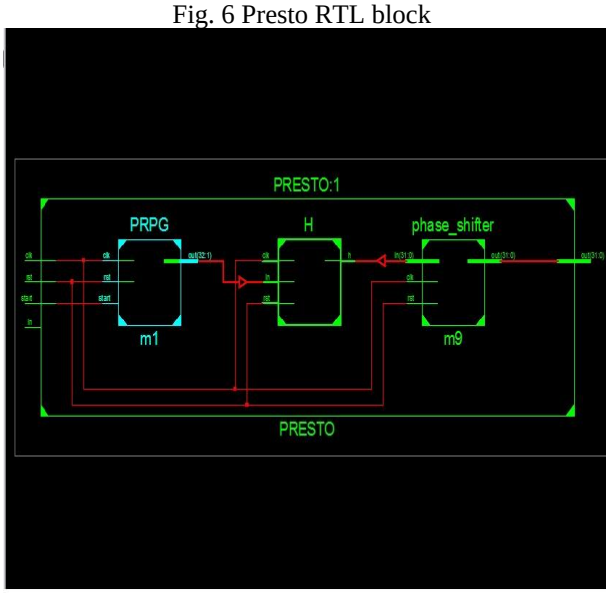

Fig.7 Presto Schematic

Fig.8 Simulation Result

VI. CONCLUSION

As shown within the paper, PRESTO—the phonograph record generator—can manufacture pseudorandom check patterns with scan shift-in shift activity exactly elite through machine-driven programming. Identical options are often wont to management the generator, in order that the resultant check vectors will either yield desired fault coverage quicker than the standard pseudorandom patterns whereas still reducing toggling rates all the way down to desired levels, or they'll supply visibly higher coverage numbers if run comparable check times. This phonograph record PRPG is additionally capable of acting as a totally useful check knowledge decompressor with the flexibility to regulate scan shift-in shift activity through the method of encryption. The planned hybrid answer permits one to with efficiency mix check compression with logic BIST, wherever each technique will work synergistically to deliver top quality check. it's so a really enticing phonograph record check theme that permits for trading-off check coverage, pattern counts, and toggling rates in an exceedingly} very versatile manner.

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