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VLSI IMPLEMENTATION OF HIGH SPEED VITERBI DECODER

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Abstract: Error correction is an integral part of any communication system and for this purpose, the convolution codes are widely used as forward error correction codes. For decoding of convolution codes, at the receiver end Viterbi Decoder is being employed. The parameters of Viterbi algorithm can be changed to suit a specific application. The high speed and small area are two important design parameters in today's wireless technology. In this paper, a high speed feed forward viterbi decoder has been designed using hybrid track back and register exchange architecture and embedded BRAM of target FPGA. The proposed viterbi decoder has been designed with Matlab, simulated with Xilinx ISE 8.1i Tool, synthesized with Xilinx Synthesis Tool (XST), and implemented on Xilinx Virtex4 based xc4vlx15 FPGA device. The results show that the proposed design can operate at an estimated frequency of 107.7 MHz by consuming considerably less resources on target device to provide cost effective solution for wireless applications.
Keywords: Viterbi Decoder, Trace Back, Register Exchange, FPGA, VHDL,Xilinx, XST, Virtex4

I. INTRODUCTION

Viterbi algorithm is being widely used in many wireless and mobile communication systems for optimal decoding of convolutional codes. Convolutional encoding with Viterbi decoding is a Forward Error Correction technique that is particularly suited to a channel in which the transmitted signal is corrupted mainly by additive white Gaussian noise (AWGN). The purpose of forward error correction (FEC) is to improve the capacity of a channel by adding some carefully designed redundant information to the data being transmitted through the channel [1]. The Viterbi algorithm essentially performs maximum likelihood decoding to correct the errors in received data which are caused by the channel noise; however it reduces the computational load by taking advantage of special structure in the code trellis [2]. The Viterbi algorithm (VA) is a recursive optimal solution to the problem of estimating the state sequence of a discrete time finite- state Markov process. Viterbi decoding has the advantage that it has a fixed decoding time and it is well suited to hardware decoder implementation [3]. The requirements for the Viterbi decoder, which is a processor that implements the Viterbi algorithm, depend on the application in which it is used.Viterbi Algorithm is effective in achieving noise tolerance, but the cost is an exponential growth in memory, computational resources and power consumption. This paper proposes high performance and low power architecture for developing a viterbi decoder using hybrid track-back and register exchange architecture and implemented on Xilinx Virtex4 based xc4vlx15 FPGA device for various digital receivers.

II. DESIGN ALGORITHM

The Viterbi algorithm proposed by A.J. Viterbi in 1967 is a computationally efficient technique for determining the most probable path taken through a Markov graph [1]. The decoding procedure can be explained by a trellis diagram. The trellis requires 2K−1 states at each stage, where K is the constraint length in convolutional encoding [3]. The stage is given by the length in bits of the message to be decoded. This algorithm calculates a measured distance between the received symbol and all possible paths at a certain stage in the trellis diagram. The viterbi decodingflowchart is given in Fig.1

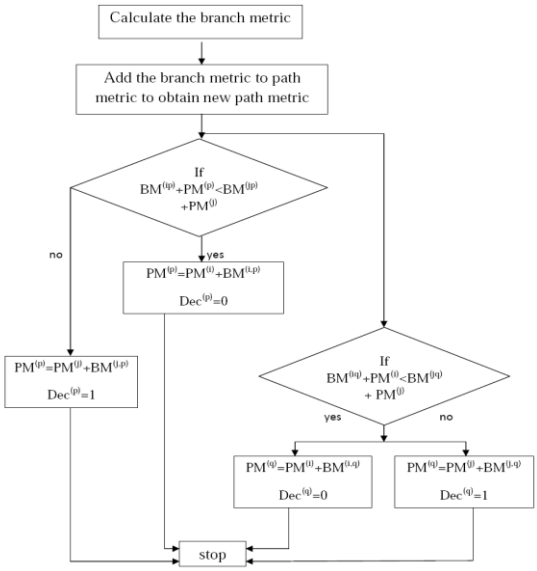

Figure 1. Viterbi Decoding Flowchart

The Viterbi algorithm applies the maximum-likelihood principle. The most common metric used is the Hamming distance metric. This is just the dot product between the received codeword and the allowable codeword. These metrics are cumulative so that the path with the largest total metric is the final winner. The selection of survivors lies at the heart of the Viterbi algorithm and ensures that the algorithm terminates with the maximum likelihood path. The algorithm terminates when all of the nodes in the trellis have been labelled and their entering survivors are determined.

III. VITERBI DECODER ARCHITECTURE

The general structure of Viterbi decoder is shown in Fig.2, which mainly consists of 3 parts: BMU (branch metric unit), ACSU (add compare select unit), and SMU (survivor management unit) [4].

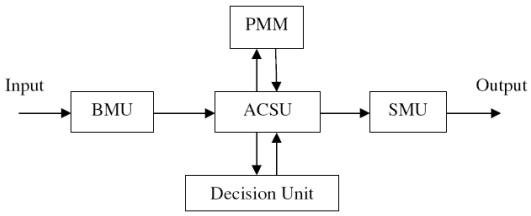

Fig. 2 Block Diagram of Viterbi Decoder

A. Branch Metric Unit

BMU calculates all the Branch Metrics (BMs) from the received symbols. BMU is transition metric unit and its function is to generate corresponding merit of skip branch according to the input code sequence. The generated sequence merit is delivered to ACS unit, completing the process as bit calculation.

B. Add Compare Select Unit

ACSU recursively computes path metrics and outputs decision bits for each state transition. The ACS module not only receives the code sequence from the branch merit module, but needs the path merit of last state and information related to state shift. It is necessary to calculate the sum of branch merit and path merit firstly, and then select the smallest path merit. For a given code with rate 1/n and total memory M, the number of ACS required to decode received sequence of length L is L×2M.

C. Survivor-path memory unit

It is responsible for keeping track of the information bits associated with the surviving paths. SMU uses these bits to find the final survivor path and decode the source bits. The arbitral bit which is generated from the ACS module will be saved in the survival path memory and will be used to search the surviving path. There are two basic approaches for searching survival path. One is named register-exchange (RE) and the other is called Trace-Back (TB). Register Exchange (RE) is the most straight forward method to extract the information bits from the encoded bits stream. It has the lowest decoding latency and simple control circuit. RE is implemented by the connection of multiplexers and registers according to the trellis diagram, and its memory requirement is NL bits registers.As decoding, all NL bits are read and written, and it requires high memory access bandwidth. It consists of a two dimension register array with multiplexers between each two columns. RE is attractive in terms of the regularity of circuit structure and decoding latency [5].

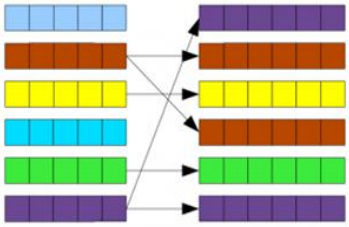

Figure 3. Register Exchange method

However, in practical applications, when VD dealing with convolutional codes with large constraint length K (i.e., K ≥ 7), RE becomes impractical due to its high power consumption and large routing overhead. Therefore it is not suited for low power applications such as wireless communications systems. One the other hand, Trace Back(TB) traces back the maximum likelihood path starting from the best state. It traces back the survivor path after the entire code word has been received and generates the decoded output sequence [6]. It is a combinational block and is active during only one clock cycle In TB method, only N decision bits are written in each cycle, and RAM can be utilized here. The power consumption of the TB architecture is much more efficient than RE when we have large constraint lengths [10].

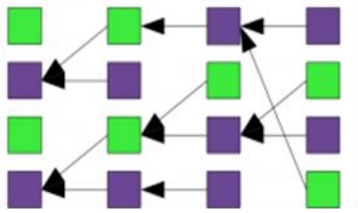

Figure 4. Trace Back method

Therefore trace-back architecture is well suited for low power applications. Trace-back memory stores the history of decision bits from ACS operation. This memory is a two dimensional circular buffer, with rows and columns. The number of rows is equal to the number of states N = 2 K-1 where K is the constraint length. Each column stores the results of N comparisons corresponding to incoming coded bits at each time interval. The number of columns is equal to the Trace back depth [7].

Our method is a hybrid of the register-exchange and the trace-back method. Instead of saving the best single-step to get to a given state, we save the best two-step path to get to that state. We thus get 256bit in two cycles, which can be written 128b/cycle. This hybrid approach can be extended to larger values, but the register-exchange doesn't scale very well.

Two-steps is a good choice as it is tractable, and provides the required amount of performance.

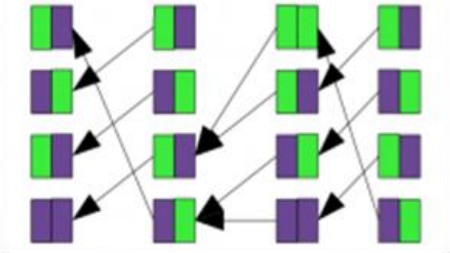

Figure 5. Hybrid RE and TB method

Further, it makes it easy to address the RAM.This hybrid method has the advantage that the FPGA block rams' mixed port widths can be used. The 2bit values contain exactly the information needed, and can be easily accessed by correct addressing of the RAM. This allows the 128:1 muxes to effectively be merged into the RAMs. This comes at a cost of extra registers and 2:1 muxes on the right side which are used to implement the register exchange. In terms of implementation, we ended up using the RAMB16 primitives. The XST manual seemed to indicate that we couldn't just infer the mixed-width rams.

IV. HARDWARE IMPLEMENTATION RESULTS

To observe the speed and resource utilization, RTL is generated, verified and synthesized using Xilinx Synthesis Tool (XST) and implemented on Xilinx Virtex4 based xc4vlx15 FPGA device. The benefits associated with FPGA such as flexibility, shorter time to market and re-configurability make them a very attractive choice for implementing the designs. The user programmability gives the user access to complex integrated designs without the high engineering costs associated with application specific integrated circuits. The benefits of clock gating are very much clear from the results since clock gating helps in switching off the parts of the circuit when not in operation, hence helping in power saving and increasing the speed of the circuit, because the clock will not be propagatingthrough those parts of the circuit. Table.1 shows the device utilization summary report.

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	1887	6144	30%
Number of Slice Flip Flops	1250	12288	10%
Number of 4 input LUTs	3482	12288	28%
Number of bonded IOBs	8	240	3%
Number of FIFO16/RAMB16s	2	48	4%
Number of GCLKs	1	32	3%

Table 1. Device Utilization Summary

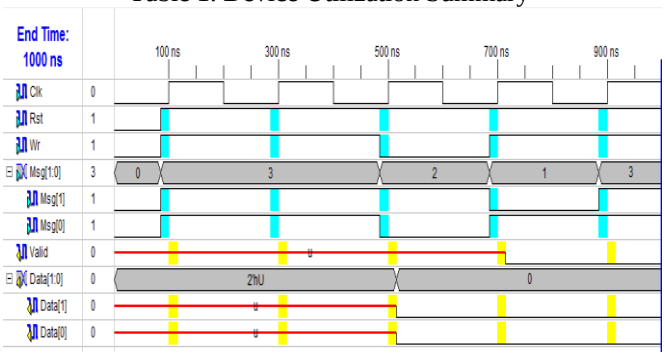

Figure 6. Simulation result of top entity of 2 bit input Viterbi decoder.

	Trace Back Method	Register Exchange Method	Existing Hybrid Method	Proposed Hybrid Method
Max. Frequency	343.525MHZ	158.983MHZ	74.914MHZ	253.891MHz
Max. Output Required Time after clock	35.829ns	23.829ns	9.338ns	3.921ns
Number of Slice Flip Flop	97	1910	446	3482

Figure 5.12: comparison among TB, RE, Hybrid

V. CONCLUSION

In this paper a high speed Viterbi decoder has been proposed. The embedded BRAM and LUTs of target FPGA have been efficiently utilized to enhance the speed of the developed decoder. The designed Viterbi decoder has been simulated using Xilinx ISE 8.1i Tool, synthesized with XST and implemented on Virtex4 based xc4vlx15 target FPGA device. The results show that proposed design can work at an estimated frequency of 86.6 MHz by using considerable less resources of target FPGA to provide high performance cost effective solution for wireless communication applications.

REFERENCES

[1] A. J. Viterbi, "Error Bounds for Convolutional Codes and an Asymptotically Optimum Decoding Algorithm", IEEE Trans. Inform. Theory, vol. IT-13, pp. 260-269, Apr. 1967.

[2] Viterbi, A., "Convolutional codes and their performance in communication systems", IEEE Trans. Commun. Techno,VOl.Com 19, no, 5, Oct.1971, pp.715-772.

[3] John G. Proakis, "Digital Communication", McGraw Hill, Singapore. pp 502-507, 471-475, 2010.

[4] Yun-NanChang, "Design of soft output Viterbi decoders with hybridtrace-backprocessing"Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on Publication Year: 2003 , Page(s): II-69 - II-72 vol.2

[5] Y. Gang, A. T. Erdogan, and T. Arslan, "An efficient pre-traceback architecture for the Viterbi decoder targeting wireless communication applications", IEEE Trans. Circuits Syst. I, Reg. Papers, vo1. 52, no. 6, June 2005, pp.1148– 1156.

[6] Muhammad B.A., Zanna M.A., Mohammed, D.A., DajabDanjuma D., "Low complexity FPGA implementation of Register Exchange Based Viterbi decoder", Emerging &Sustainable Technologies for Power & ICT in a Developing Society (NIGERCON), 2013 IEEE International Conference on Publication Year: 2013 , Page(s): 21 - 25

[7] Black P.J. MengTeresa H.-Y., " Hybrid survivor path architectures for ViterbidecodersAcoustics", Speech, and Signal Processing, 1993. ICASSP-93., 1993 IEEE International Conference on Publication Year: 1993, Page(s): 433 - 436 vol.1.

[8] Cheng Zhan, Sami Khawam, TughrulArslan, Iain Lindsay, "Efficient Implementation of Trace-back Unit in a Reconfigurable Viterbi Decoder Fabric", IEEETransaction paper,2005.

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