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HIGH SPEED MULTIPLIER AS IIR FILTER DESIGN USING VEDIC MATHEMATICS

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Abstract: Digital signal processing operation utilizing Vedic mathematics which performs the signal handling operation like convolution, circular convolution, cross correlation, auto-correlation and filter design. Digital signal processing (DSP) operations are vital part of engineering and medical field. Outlining of DSP operations have numerous methodologies. This configuration procedure gives the analysis of signals to enhance the accuracy of the mathematical calculations. It encourages the time sharing for all signals to process mathematical operations all the while. Vedic mathematics is the ancient math which has a unique method of mental calculation with the assistance of basic rules and standards based on sutras. The utilization of multiplier has demonstrated the efficiency of Urdhva-Tiryakbhayam method for multiplication which conveys a distinction in the real procedure of multiplication itself. The configuration of IIR filters utilizing Urdhva-Tiryakbhayam sutra. This calculation is performed in Xilinx and compare with MATLAB operation of IIR filter respectively.
Keywords: Vedic Mathematics, Multiplier, DSP, IIR Filter, Urdhwa Tiryagbhyam Sutra,MATLAB 8.1,Xilinx 14.5 ISE.

I. INTRODUCTION

Multipliers are basic building blocks of any processor design and normally we called as heart of DSPs [4]. Modern multipliers speed of computation decreases as the inputs increase. There are many multipliers available today like Combinational multiplier, array multiplier, serial and parallel multiplier and many more. Thus building high speed multipliers for processor design is done using Vedic. In DSPs, Filtering is normally used and is applied to many applications like speech processing etc. Digital Signal Processing operations like convolution, Fast Fourier Transform, DFT calculation. Frequency sampling etc method is being used in many applications. Filtering is a method which is used for removing unwanted signal frequencies by being sensitive to the wanted signal frequencies. Digital audio or video when it is transmitted through the communication channel, noisy is added to the original signal. So,at receiver side filtering is must in order to get original one. Basically, filters are Classified into 4 types depending upon the pass band and stopbands.FIR and IIRare two types of filter designed in this paper. Digital signal processing have to perform operations like frequency domain filtering (FIR, IIR) and frequency transformations like DFT, FFT, and DCT. For these operation multiplication is an essential hardware component[2,12] .Thus the performance of the multiplier is a key element in determining the performance of the entire system. This is because the multiplier is the slowest and most time consuming element in the system. Thus the optimization of the multiplier speed and area is a major challenge for the system designers. This challenge can be successfully overcome by the use of ancient Vedic mathematics.

II. LITERATURE REVIEW

The word 'Vedic' is derived from the word 'Veda' which means the store-house of all knowledge. Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc. These Sutras along with their brief meanings are enlisted below alphabetically[3,5].

1. (Anurupye) Shunyamanyat – If one is in ratio, the other is zero
2. Chalana-Kalanabyham – Differences and Similarities.
3. Ekadhikina Purvena – By one more than the previous one
4. Ekanyunena Purvena – By one less than the previous one
5. Gunakasamuchyah – The factors of the sum is equal to the sum of the factors
6. Gunitasamuchyah – The product of the sum is equal to the sum of the product
7. Nikhilam Navatashcaramam Dashatah – All from 9 and the last from 10
8. Paraavartya Yojayet – Transpose and adjust.
9. Puranapuranabyham – By the completion or non-completion
10. Sankalana-vyavakalanabhyam – By addition and by subtraction
11. Shesanyankena Charamena – The remainders by the last digit
12. Shunyam Saamyasamuccaye – When the sum is the same that sum is zero
13. Sopaantyadvayamantyam – The ultimate and twice the penultimate
14. Urdhva-Triyakbhyam – Vertically and crosswise
15. Vyashtisamanstih – Part and Whole
16. Yaavadunam – Whatever the extent of its deficiency

The study of these formulae is a field of diverse study. The proposed design uses only Urdhva-Triyakbhyam method hence the detailed description of other formulae is beyond the scope of this project.

Sri Bharti Krishna Tirthaji (1884-1960) proposed the theory of Vedic mathematics after his eight years of research on Atharva Vedas [14]. This branch of mathematics depend on sixteen sutra. Vedic mathematics is a very interesting field and presents some effective algorithms that can be applied to various branches of engineering such as computing and digital signal processing. Associating multiplication with Vedic Mathematics techniques would result in the saving of computational time.

III. PROPOSED SYSTEM

Following are the series of steps involved in the propose method of high Speed Multiplier Design Using Vedic Mathematics.

A Vedic mathematic multiplier is designed using the Urdhva Triyakbhyam sutra. Apply the multiplier to a IIR filter design. Implement and simulate the developed IIRfilter in MATLAB. Compare the simulated results of these proposed FIR Filter with normal multiplies and derive a conclusion based on these comparisons.

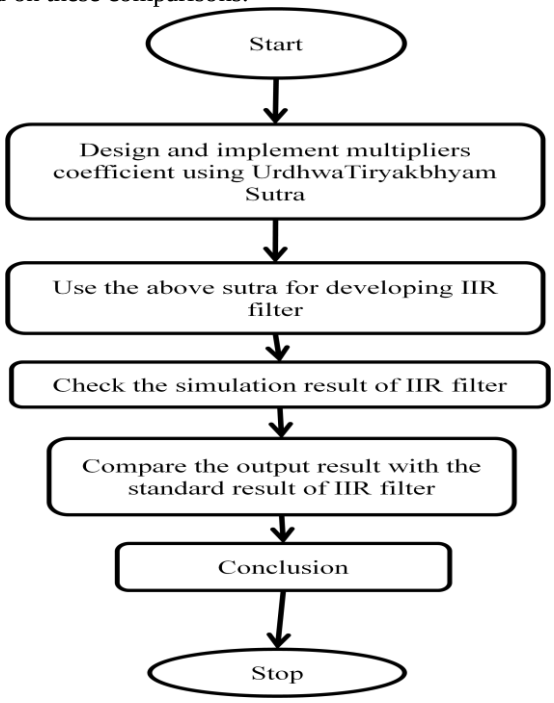

Fig. 3.1 high Speed Multiplier Design Using Vedic Mathematics

IV. METHODOLOGY

A.VEDIC MULTIPLIER

The use of Vedic mathematics is to reduces the typical calculations in conventional mathematics to very simple one. Because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. Vedic Mathematics is a methodology of arithmetic rules that allow more efficient speed implementation. It also provides some effective algorithms which can be applied to various branches of engineering such as computing. A. Urdhva Tiryakbhyam Sutra The proposed Vedic multiplier is based on the "Urdhva Tiryagbhyam" sutra (algorithm)[5]. These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. It is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and Crosswise"[9]. It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel and the multiplier is independent of the clock frequency of the processor. Due to its regular structure, it can be easily layout in microprocessors and designers can easily circumvent these problems to avoid catastrophic device failures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure[6]. Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other conventional multipliers.

B. URDHVA TIRYAKBHAYAM SUTRA FOR BINARY NUMBER SYSTEM

In this section this Sutra is extended to binary number system [10]. To illustrate the multiplication algorithm, consider the multiplication of two binary numbers a3a2a1a0 and b3b2b1b0. As the result of this multiplication would be more than 4 bits, let it be as …r3r2r1r0. Line diagram for multiplication of two 4-bit numbers is shown in Fig. 2 which is nothing but the mapping of the Fig. 1 in binary system. For the sake of simplicity, each bit is represented by a circle. Least significant bit r0 is obtained by multiplying the least significant bits of the multiplicand and the multiplier. The process is followed according to the steps shown in Fig. 2. As in the last case, the digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result (rn) and a carry (say cn). This carry is added in the next step and hence the process goes on. If more than one line are there in one step, all the results are added to the previous carry. In each step, least significant bit acts as the result bit and the other entire bits act as carry. For example, if in some intermediate step, we get 110, then 0 will act as result bit and 11 as the carry (referred to as cn in this text). It should be clearly noted that can may be a multi-bit number. Thus the following expressions are coming:

r0 = a0b0; (1)
c1r1 = a1b0 + a0b1; (2)
c2r2 = c1 + a2b0 + a1b1 + a0b2; (3)
c3r3 = c2 + a3b0 + a2b1 + a1b2 + a0b3; (4)
c4r4 = c3 + a3b1 + a2b2 + a1b3; (5)
c5r5 = c4 + a3b2 + a2b3; (6)
c6r6 = c5 + a3b3 (7)

With c6r6r5r4r3r2r1r0 being the final product.

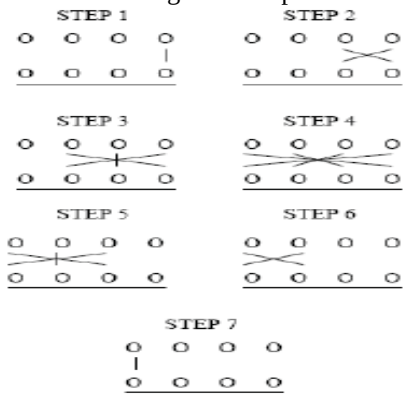

Fig 3.1: Line diagram for multiplication of two numbers

C. IIR FILTER

IIR filters are digital filters with vast motivation reaction. Dissimilar to FIR filters, they have the feedback and are called recursive digital filters [4].

IIR filters are digital filters with infinite impulse response. Unlike FIR filters, they have the feedback (a recursive part of a filter) and are known as recursive digital filters. Therefore for this reason IIR filters have much better frequency response than FIR filters of the same order[10]. Unlike FIR filters, their phase characteristic is not linear which can cause a problem to the systems which need phase linearity. For this reason, it is not preferable to use IIR filters in digital signal processing when the phase is of the essence.Otherwise, when the linear phase characteristic is not important, the use of IIR filters is an excellent solutionThe IIR filters have vastly improved frequency reaction than FIR filters of the same request (order)[9]. Dissimilar to FIR filters, their stage trademark (phase characteristics) is not direct which can bring about an issue to the frameworks which need stage linearity. For this reason, it is not desirable over utilization IIR filters in digital signal when the phase is of the substance. FIR filters can have straight phase trademark that is certainly not of IIR filters. When it is important to have straight phase trademark, FIR filters are the main accessible arrangement. In different situations when straight phase trademark is redundant, for example, FIR filters, speech signal processing is bad arrangement. IIR filters ought to be utilized. The subsequent filter request is significantly lower for the same frequency reaction. The IIR filter transfer function is a proportion of two polynomials of complex variable z-1.The numerator characterizes area of zeros, though the denominator characterizes area of poles of the subsequent IIR filter transfer function.

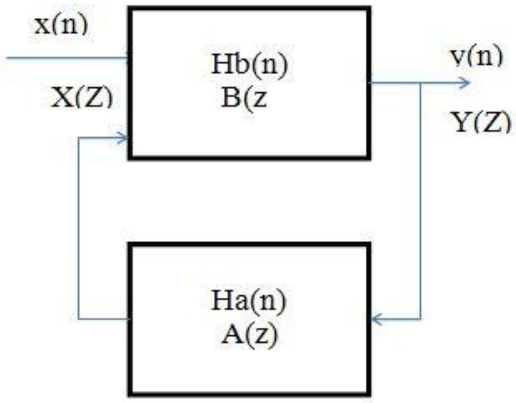

Fig 4.1. IIR Filter

V. CONCLUSION

The proposed structure of IIR filters utilizing Urdhva Tiryagbhyam sutra of Vedic mathematics. This proposed design is performed in XILINX 14.5 ISE version. The sutras of Vedic mathematics are much more effective than customary mathematics. The Urdhva Tiryagbhyam sutra is faster than the customary method of multiplication. Thus IIR filter based on Vedic sutra taking less average processing time as compared to conventional methods[10].

VI. FUTURE SCOPE

The work will be done by using the harn Carlson adder; which require less gate as compare to the reversible gates adder or ripple carry adder or carry look ahead adder.

Any real time signal processing unit consists of math operations is a multiplier. With the use of proposed IIR filter multiplication based on Vedic mathematics signal processing can be made faster and efficient. Thus this kind of IIR filter multiplication can be used in embedded signal processing unit.

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