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DESIGN AND IMPLEMENTATION OF FRONT-END CONVERTER WITH HIGH EFFICIENCY, HIGH POWER DENSITY FOR HIGH VOLTAGE CAPACITOR CHARGER

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ABSTRACT: Capacitor charging system has been widely used for the commercial, medical and military applications. Recently, its technology has been taken attention again due to the World events and the concerns about the environmental problems as well. Furthermore, the capacitor charging system is being actively studied for the future tactical weapon system. In this thesis, the specific application for the tactical armor system was introduced, and its specifications were given. Also, the distributed power system (DPS) for the capacitor charger was presented.In this thesis, a distributed power system (DPS) for the capacitor charger is introduced for the application of the active armor system. A design methodology is also presented for the front-end converter to achieve the high power density as well as the high efficiency. Design parameters are identified, and their impact on the design result is studied. Finally, the optimal operating point is determined based on the loss comparison between different operating points.In order to further improve the power density utilizing the unique operation mode i.e. pulse power operation, transformer with an amorphous-based core is designed and the result is compared with that using ferrite-based core. A 5 kW prototype converter is built up and the experimentation is performed to verify the design.

I. INTRODUCTION

A plug-in hybrid electric vehicle (PHEV) is a hybrid vehicle with rechargeable batteries that can be restored to full charge by connecting the vehicle plug to an external electric power source. In recent years, PHEV motor drive and energy storage technology has developed at a rapid rate in response to expected market demand for PHEVs. Battery chargers are another key component required for the emergence and acceptance of PHEVs. For PHEV applications, the accepted approach involves using an on-board charger [1]. An onboard 3.3 kW charger can charge a depleted 16 kWh battery pack in PHEVs to 95% charge in about four hours from a 240 V supply. The most common charger power architecture includes an AC-DC converter with power factor correction (PFC) [2] followed by an isolated DC-DC converter. Selecting the optimal topology and evaluating power loss in power semiconductors are important steps in the design and development of these battery chargers [3]. In this paper a two stage battery charger is presented, including an AC-DC converter with an interleaved boost PFC followed by a PWM ZVS full-bridge DC-DC converter. The charging solution presented achieves a peak efficiency of 93.6%, while maintaining the ability to operate over a wide output voltage variation of 200V to 450V. The solution achieves a compact size of 5.46 L, 6.2 kg in weight and 273×200×100 mm in dimension. This paper presents the operation, design and experimental results of the battery charging solution proposed.

II. THE PROPOSED TWO STAGE BATTERY CHARGER

The two stage battery charger configuration is illustrated in Fig. 1. In this configuration, an interleaved boost PFC circuit is used for the front-end converter, which is followed by an isolated full-bridge DC-DC converter.

A.Front-End First Stage AC-DC PFC Rectifier

The interleaved PFC consists of two CCM boost converters in parallel, which operate 180° out of phase [4-6]. The input current is the sum of the inductor currents in LB1 and LB2. Since the inductor ripple currents are out of phase, they tend to cancel each other and reduce the input ripple current. The maximum input inductor ripple current cancellation occurs at 50% duty cycle. The output capacitor current is the sum of the two boost diode currents less the dc output current.

Interleaving reduces the output capacitor ripple current as a function of the duty cycle [7]. As the duty cycle approaches 0%, 50%, and 100% duty cycle, the sum of the two diode currents approaches dc. At these points, the output capacitor only has to filter the inductor ripple current.

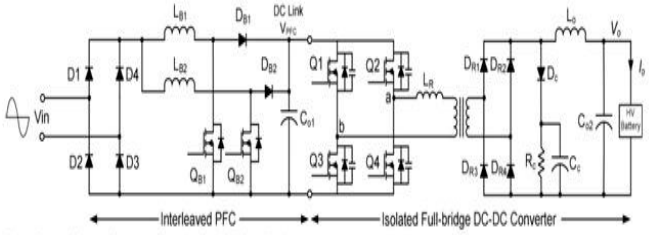


Fig. 1. Proposed battery charger configuration for a PHEV application.

The interleaved boost converter inherently takes advantage of paralleled semiconductors to reduce conduction loss. Furthermore, by having the converters switched out of phase, it doubles the effective switching frequency, therefore reducing the input current ripple, resulting in a reduction of the size of the input EMI filter.

In order to design the interleaved PFC converter, it should be treated as two conventional boost PFC converters with each operating at half of the load power rating. With this approach, all equations for the inductor, switch and diode in the conventional PFC remain valid, since the stresses are unchanged with the only exception being the reduced ripple current through the output capacitors.

B.Second Stage ZVS Full-Bridge DC-DC Converter The full-bridge zero-voltage switching (ZVS) converter [811],

behaves like a traditional hard-switched topology, but, rather than driving the diagonal bridge switches simultaneously, the lower switches (Q3 and Q4) are driven at a fixed 50% duty cycle and the upper switches (Q1 and Q2) are pulse width modulated on the trailing edge [12].

As shown in Fig. 1, the power semiconductor switches have been modeled with parallel diodes and parasitic capacitances. All parasitic capacitances in the circuit including winding and heatsink capacitance have been lumped together as switch capacitance. The output rectifiers are considered ideal and the external resonant inductor also includes the transformer leakage inductance. The beginning of the cycle, shown in Fig. 2, is arbitrarily set as having switches Q1 and Q4 on and Q3 and Q4 off. This is a power transfer period and the primary current flows through Q1transformer primary-LR-Q4. This power transfer period terminates when switch Q1 turns off as determined by the PWM signal. As the current flowing in the primary cannot be interrupted instantaneously, it finds an alternate path and flows through the parasitic switch capacitance of Q3 and Q1 which discharges the node b to 0V and then forward biases the body diode D3.

The primary resonant inductor LR, maintains the current which circulates around the path of D3-transformer primaryLR-Q4. When switch Q1 opens, the output inductor current free-wheels through all four output diodes, DR1-DR4. During this switch transition, the output inductor current assists the resonant inductor in charging the upper and lower bridge FET capacitance. At the end of the free-wheeling period, Q3 and Q4 toggle. The actual timing of this toggle is dependent on the resonant delay which occurs prior to Q2 turning on. The ZVS transition occurs during this resonant delay period after Q3 and Q4 toggle and before Q2 turns on. The required resonant delay is 1/4 of the period of the LR×C resonant frequency of the circuit formed by the resonant inductor and the parasitic capacitance. The resonant transition may be estimated by (1),

$$\tau = \frac{\pi}{2}\frac{1}{\sqrt{\frac{1}{L_R \times C} - \frac{R^2}{4\times(L_R)^2}}} \qquad \text{……..(1)}$$

whereτ is the resonant transition time, L_R is the leakage inductance, C is the parasitic capacitance, and R is the equivalent resistance in series with L_R and C.

When Q3 and Q4 toggle, the primary current that was flowing through Q4 now finds an alternate path and it charges/discharges the parasitic capacitance of switches Q4 and Q2 until the body diode of Q2 is forward biased. If the resonant delay is set properly, switch Q2 will be turned on with ZVS at this time. The output inductor does not assist this transition. It is purely a resonant transition driven by the resonant inductor.

The second power transfer period commences when Q2 turns on and primary current flows through Q2-L_R-transformer primary-Q3. The rest of the circuit operation can be explained in a similar manner.

A clamp network consisting of D_C, R_C and C_C is needed across the output rectifier to clamp the voltage ringing due to diode junction capacitance with the leakage inductance of the transformer. This DC-DC converter also suffers from duty cycle loss as illustrated in Fig. 2. Duty cycle loss occurs for converters requiring inductive output filters when the output rectifiers commutate enabling all of the diodes conduct, which effectively shorts the secondary winding [12]. This causes a decrease in the output voltage and thus a higher transformer turns ratio is needed, which increases the primary peak current.

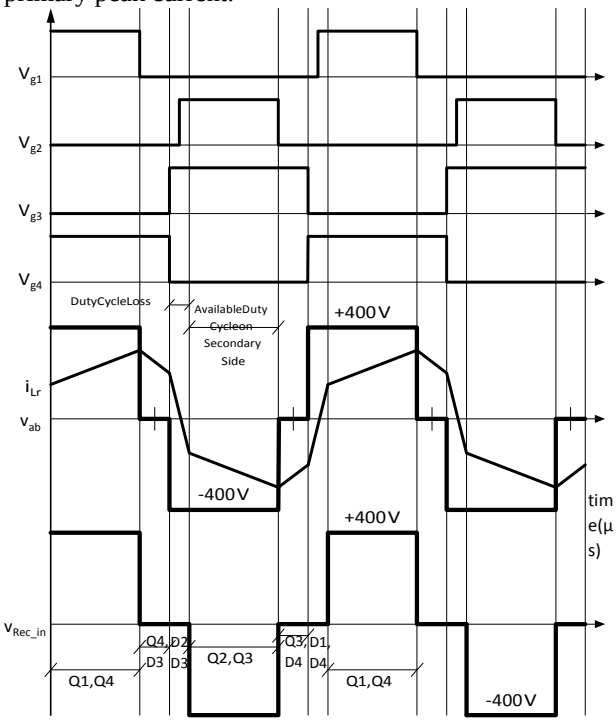


Fig. 2. Typical operating waveforms to illustrate the operation of the ZVS Full-Bridge converter.

III. SPECIFICATIONS AND DESIGN OF THE PROPOSED CHARGER

This section provides the design details for the two stage 3.3kW battery charger [13], which was designed to meet the specifications given in Table I.

The full-bridge DC-DC converter was designed to operate at a PFC bus voltage (V_{PFC}) of 400V and an output voltage (Vo) of 400V at full load. Initially, a peak-to-peak output ripple (ΔI_O) of 1A was assumed. Accounting for dead-time and duty cycle loss, an initial duty ratio of *Deff = 0.75* was assumed.

Then the transformer turns ratio is given by [14]:

$$n_t = \frac{D_{eff} \times V_{in}}{V_o} = 0.75 \qquad \text{……(2)}$$

A custom planar type ferrite transformer was designed using turns ratio of 12(Np):16(Ns).

An inductor value of 400 µH was selected using (3):

$$L_o = \frac{(\frac{V_{in}}{n_t} - V_o) \times D_{eff}}{\Delta I_d \times 2 f_s} \qquad \text{……(3)}$$

TABLE I: DESIGN SPECIFICATIONS OF THE PROPOSED CHARGER

Parameters	Value[Units]
Input AC Voltage	85 – 265 [V]
Maximum Input AC Current	16 [A]
Power Factor @ F.L. and 240 V in	99 [%]
AC Input Frequency	47 – 70 [Hz]
THD at F.L. and 240V in	< 5 [%]
Overall Efficiency	Up to 94 [%]
Output DC Voltage Range	200 to 450 [V]
Maximum Output DC Current	11 [A]
Maximum Output Power	3.3 [kW]
Output Voltage Ripple	< 2 [Vp-p]
PFC Switching Frequency	70 [khz]
DC-DC Switching Frequency	200 [kHz]
Cooling	Liquid
Dimensions	273 x 200 x 100 [mm]
Mass/Volume	6.2 [Kg] / 5.46 [L]
Operating Temperature	-40°C to +105°C Ambient
Coolant Temperature	-40°C to +70°C

A toroidal, iron powder core was used in the design for the resonant inductor. An 8µH inductor was selected using (4):

$$L_R = \frac{n_t \times V_{in}(1-D_{eff})}{4\,\Delta I_d \times f_s} \approx 8\mu H \quad \text{.....(3)}$$

A toroidal (iron powder core) inductor was used to obtain 6µH and an additional 2µH was obtained using the transformer leakage inductance.

A 600V, 80 mΩRdson, 450 pF Cds (parasitic capacitance) MOSFET with a fast body diode was selected for the four primary switches. A 12A silicon carbide diode was selected for the four output rectifier diodes. A 33 µF/500V electrolytic capacitor was selected for output ripple current filtering.
For the PFC section, a 600 V, 99 mΩRdson was selected for each channel of the interleaved PFC. A 600 V, and 6 A silicon carbide diode was selected for PFC boost diode. Gapped ferrite cores were used to obtain 400 µH inductances for each of the PFC inductors. A standard two-phase interleaved CCM PFC controller from Texas Instruments, UCC28070, was used to implement the control for the PFC front end.

IV. EXPERIMENTAL RESULTS

The internal component organization of the battery charger is provided in Fig. 3. The AC input power is fed through the top left connector which then feeds the inrush current protection circuit followed by the EMI filter. The inrush protection and EMI filter circuit is placed in a shield to meet stringent FCC Class B conducted and radiated emission requirements.

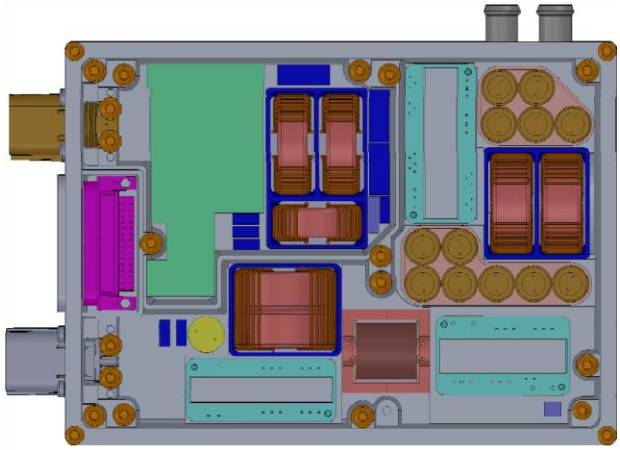


Fig. 3. The internal component organization of the charger.

The interleaved PFC circuit consists of the PFC block where the AC rectifier diodes, boost MOSFET's and diodes are mounted. There are two boost inductors and 12×82 µF/450V PFC bus capacitors. The 400V DC from the PFC output is fed to the HV primary block on which the fullbridge MOSFET's and resonant inductor are mounted. The HV transformer is placed in between the primary and secondary block. The output rectifier diodes and the clamp resistor RC is mounted on the secondary block. The output filter inductor and capacitor are also shown. Finally the HV DC output power is delivered through the bottom left connector. All of the power components and blocks are connected to the base plate of the chassis for cooling through the liquid channels. Fig. 4 illustrates the mechanical packaging of the charger.

Fig. 4. The mechanical packaging of the charger.

Waveforms of the input voltage, input current and PFC bus voltage of the charger are provided in Fig. 5 for the following test conditions: Vin = 240 V, Iin = 15 A, Po = 3300 W, Vo = 300 V, fsw = 70 kHz (PFC) and 200 kHz

(DC-DC). The input current is in phase with the input voltage, and its shape is nearly perfectly sinusoidal, as expected.

The HV output voltage and current is also shown in Fig. 6 for Vo = 400 V and Io = 8 A. As seen the HV output is a low frequency ripple free output. This is very favorable for charging the electric vehicle batteries.

Power factor is another useful parameter to show the quality of input current. The charger input AC power factor is provided in Fig. 7 for the entire load range at 120 V and 240 V input. The power factor is greater than 0.99 from half load to full load.
Curves of the input current total harmonic distortion are provided in Fig. 8 for full load at 120 V and 240 V input. It is noted that the input current THD is less than 5% from half load to full load.

In order to verify the quality of the input current in the proposed topology, its harmonics up to the 39th harmonic are given and compared with the IEC 1000-3-2 standard in Fig. 9 for 120 V and 230 V input. All converter harmonics are well below IEC standard, which is required for PHEV chargers.

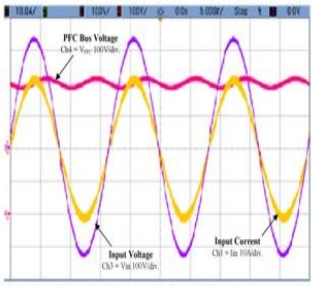
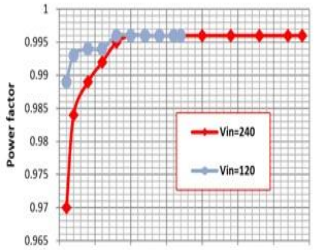


Fig. 5. Experimental waveforms of input current, input voltage and PFC Bus voltage of an interleaved boost converter at Vin = 240 V and Full



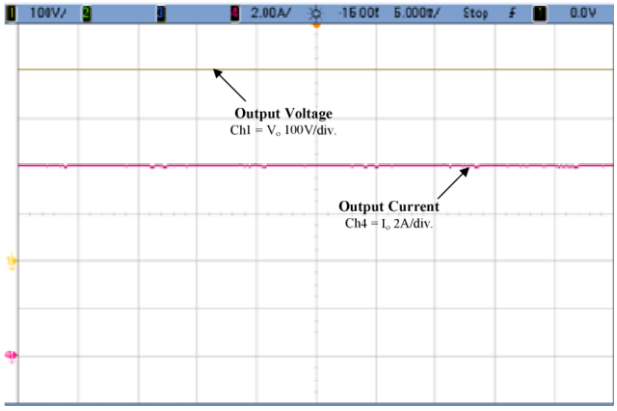


Fig. 6. Experimental waveforms of HV output voltage and current.Ch1= Vo 100V/div. Ch4= Io 2A/div.

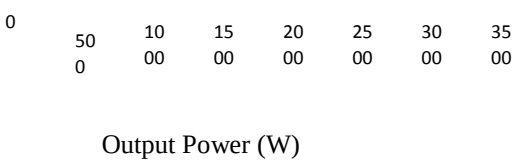


Fig. 7. Experimental measured PF as a function of output power at 240 V and 120 V input.

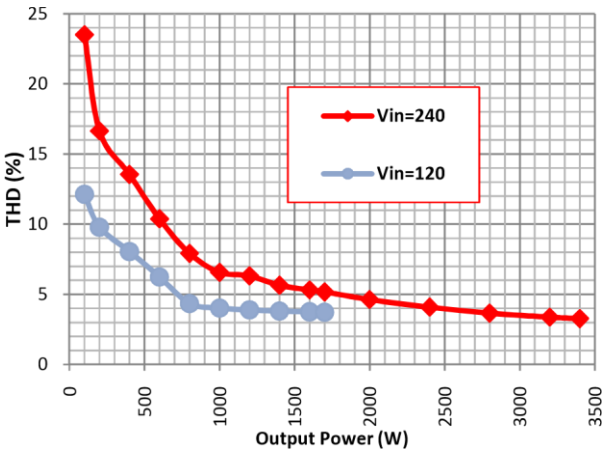


Fig. 8. Experimental measured THD as a function of output power at 240 V
and 120 V input.

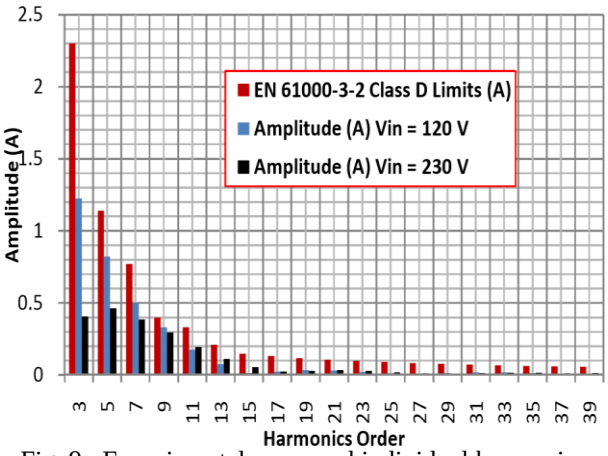


Fig. 9. Experimental measured individual harmonics as a function of harmonic number for at 120 V, 1700 W and 230 V, 3300 W.

Figs. 10 and 11 illustrate zero voltage turn-on for MOSFETs Q1 and Q3 respectively, at 300 V output voltage and 3.3 kW load.

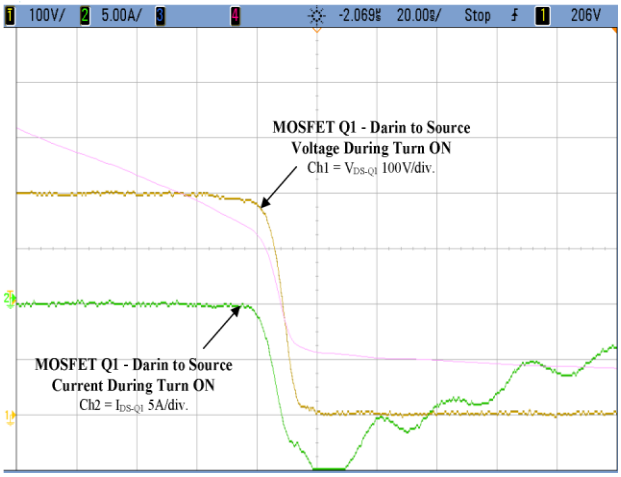


Fig. 10. Experimental waveforms of MOSFET Q1 voltage and current during Turn-ON at Vo = 300 V and Io = 11 A. Ch1= VDS-Q1 100V/div. Ch2= IDS-Q1 5A/div.

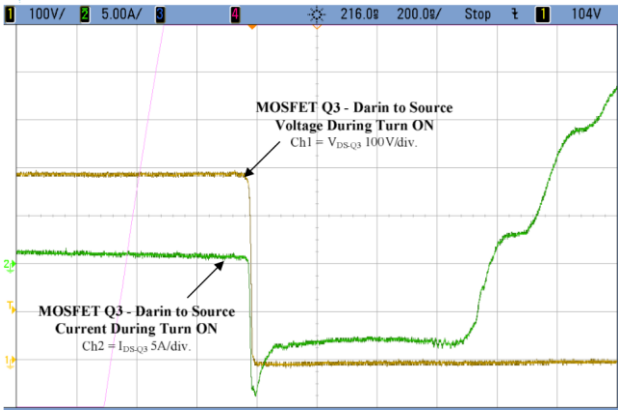


Fig. 11. Experimental waveforms of MOSFET Q3 voltage and current during Turn-ON at Vo = 300 V and Io = 11 A. Ch1= VDS-Q3 100V/div. Ch2= IDS-Q3 5A/div.

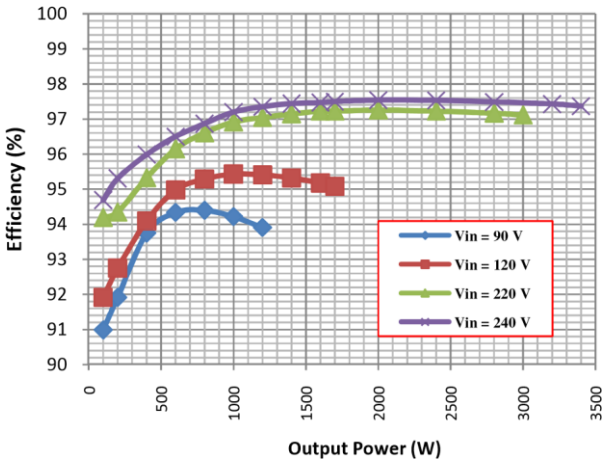


Fig. 12. Experimental measured efficiency as a function of Efficiency versus output power at different input voltages for interleaved PFC boost converter.

The efficiency of the PFC stage, the DC-DC stage and the overall efficiency for the battery charger are illustrated in Figs. 12-14, respectively.

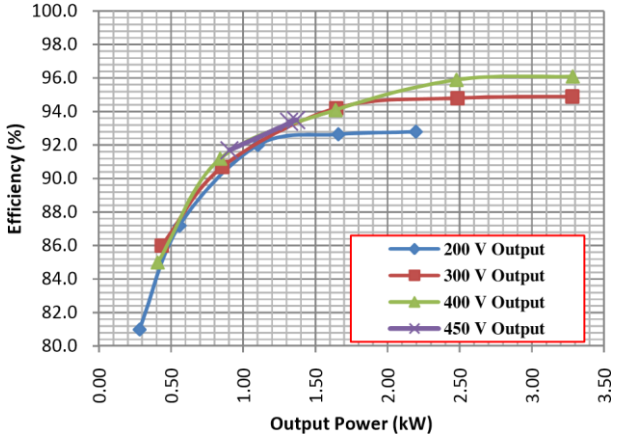


Fig. 13. Experimental measured efficiency as a function of Efficiency versus output power at different output voltages DC-DC converter.

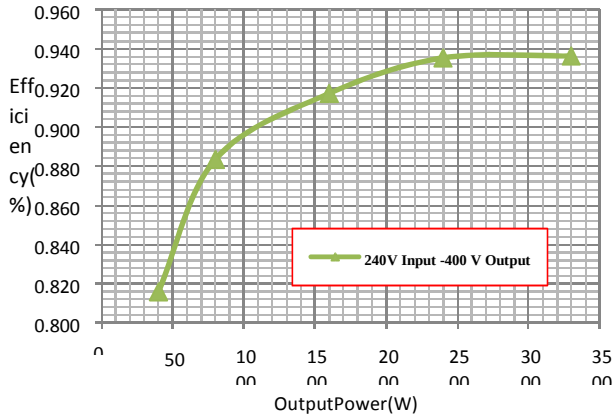


Fig. 14. Experimental measured efficiency of the charger as a function of output power at 240 V input and 400 V output voltages.

With the proposed charging solution a peak charger efficiency of 93.6 % was reached at 240 V input and 3.3 kW output power. High efficiency over the entire load range is achieved with this solution. Furthermore, high efficiency means that more of the limited input power is available to charge the batteries, reducing charging time and electricity costs.

V. CONCLUSIONS

A high performance two stage AC-DC battery charger topology has been presented in this paper for PHEV battery charging application. The detailed operation, design and performance characteristics of the proposed converter are presented. Experimental results presented include waveforms, and efficiency and input current harmonic data. The input current harmonics at each harmonic order were compared with the IEC 1000-3-2 standard limits. The input current THD is less than 5% from half load to full load and the converter is compliant with the IEC 1000-3-2 standard. The charger power factor was also provided for the full load power range at 120 V and 240 V input. The power factor is greater than 0.99 from half load to full load. The proposed charger achieved a peak efficiency of 93.6 % at 70 kHz and 200 kHz switching frequency for PFC and DC-DC stages respectively, 240 V input and 3.3 kW output power.The converter meets all required design specifications. It operates over a wide output voltage range of 200V to 450V and is packaged in a compact size of 5.5L.

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