IMPLEMENTATION OF AMBA AHB BUS ARBITER USING CONFLATION ALGORITHM

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ABSTRACT: Today electronic device are getting smaller and thin, but the performance and their operation range is increase. This possible only because of System on chip design mythology in this mythology number of block are integrated in as single chip. As many blocks are integrated in single IC they required a powerful communication architecture which can able to fulfill their demand. This demand is fulfill by ON CHIP BUS Architecture. As today many On Chip Bus architecture by different company are available in market but one of most popular On Chip Bus architecture is AMBA by ARM. It has an advantage that it is an open specification. The problem arises when numbers of master are trying to sense a single data bus and the resolution become a big issue. The system performance depends upon an ability to resolve this resolution problem. The AMBA protocol use logical assignment of chance to different masters according to their priority to take over the bus for data transmission. AMBA architecture defines three specifications. They are advance high performance bus, advance peripheral bus and advance system bus. Among all three specification AHB have high bandwidth and this make AHB as first choice for system designer. Arbiter is a digital circuit and working of it depends upon the arbitration algorithm. According to arbitration algorithm arbiter decide that which master get access to bus. In this project we design arbitration algorithm, according to it arbiter give grant to different masters.
KEYWORDS: SoC, On-chip bus, AMBAAHB, arbitration algorithm

I. INTRODUCTION

1.1 System on Chip
In current scenario semiconductor industry make impressive improvement, due to VLSI technology very high density of component in a single chip can be achieved. In 21st century demand of market is increased due to which complexity is also increased. System on chip (SOC) is one of the immerging techniques. In SOC number of block are integrate in a single chip. In this technique microprocessor, DSP processor, memory or other block are integrated in a single chip. The processor can be standard or custom as per demand. In every day electronic device, we can see the example of SOC technique like mobile, laptop etc.

1.2 On Chip Bus Architecture
In IC, integration of number of blocks likes microprocessor, memory or other peripheral device. Increase the circuit complexity as well as communication complexity hence an efficient communication medium is required to fulfill the

demand. This demand is fulfilled by on chip bus architecture (OCBA).In OCBA, all block/peripheral device are interconnected. In such a way that communication complexity can be minimized. The performance of overall SOC system is based on the performance of OCBA. The main operational duty of OCBA is to provide communication medium between different block and also to satisfy all interface behavior of each device.

1.3 AMBA BUS
AMBA from ARM is an open specification protocol, which describes number of bus and interface. Advance system bus is the first version of AMBA version and in its second version it defines AMBA2.0 which is a high performance bus. Advance high performance bus is a single clock edge protocol.
Three specifications are define by AMBA -
Advanced High- Performance Bus (AHB).
Advanced System Bus (ASB).
Advanced Peripheral Bus (APB).
All three specifications are widely used in many applications. ASB is oldest and to support high performance.AHB is being introduced later. The APB is generally used as secondary bus.
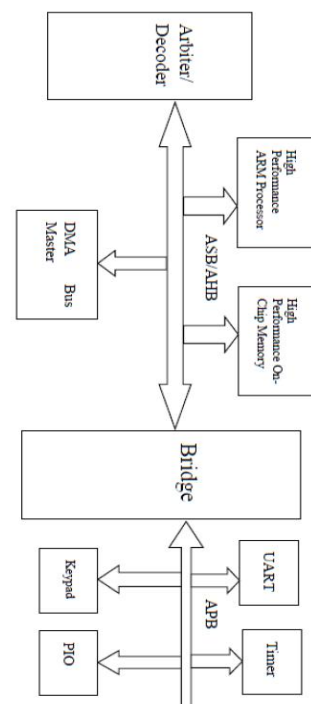

Fig 1 Advanced Microcontroller Bus Architecture

1.4 Advanced High Performance Bus

AMBA 2.0 defines the advanced high performance bus.AHB have high bandwidth which make AHB is best choice among ASB and APB. The property required for high performance, high clock frequency systems are as follows.

- Burst transfers (4/8/16 beat burst)
- Split transactions
- Bus master handover in single cycle
- Single clock edge operation

1.5 Property of AMBA AHB

To under the proper functioning of AHB it is compulsory to understand the properties of AHB bus system.

- AHB support burst transfers.
- Split transaction by split capable slave is also support by AHB.
- AHB provide single-cycle bus master handover.
- Single-clock edge operation is done in AHB.
- Non-tristate implementation is done in AHB.
- Wider data bus configurations it support 64 and 128 bits.

1.6 Arbiter

Arbiter is digital circuit and it main operation is to grant access to master to share resources. In OCBA, arbiter play a important role, in SOC design number of master are integrated and connected, and they all try to access the bus. The problem arises when two or more master raises the requests to access the bus at same time. Then it arbiter duty to given access to buses to one master and force the other master to remain ideal. To do so arbiter uses the arbitration algorithm. The efficiency of arbiter to handle the request from all master and slave make it a important block in SOC design. It arbiter duty to fulfill the demand of master, as in some application master request real time or it request the some specified bandwidth. The arbiter ensure that ,transaction accomplished in fixed number of cycle for real time requirement and for fixed between requirement it ensure that master must occupy a fixed fraction of bandwidth of bus. In arbiter, arbitration algorithm could be implementing in two ways they are centralized and distributed. In distributed arbitration algorithm slave side arbitration is absent where as in centralized algorithm it is present. The choice of algorithm is to optimize the arbiter operation and for particular application, power utilization by arbitration technique varies significantly.

II. PROPOSED AMBA AHB ARBITER ARCHITECTURE

In SOC design, number of block are integrated, in a single chip, for better performance of chip ,use of right OCBA is very important and in OCBA role of arbiter is very important. Arbiter is digital circuit which handles the entire request generated by all master and slave, if it is not working properly then overall performance of SOC system suffer. The working of arbiter is to share resource i.e. when number of master are connected to slave and some of them request to access bus at a same time, then arbiter give grant to only One master and force the other master to remain ideal. Fig 2 show the round robin algorithm

Round Robin scheme
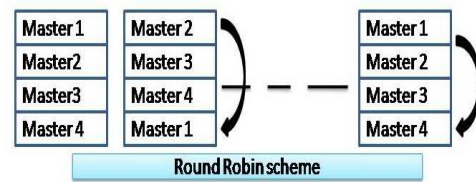
In round robin algorithm master1 as shown in fig 2 have grant to access the share bus. In clock1,after data done signal master 1 move to the bottom and in next clock ,grant is given to master 2,this process continue till all the master get grant to access bus. After fourth clock master1 is again in top position have grant to access the bus. In fig 3 the working of fixed priority algorithm is shown, here working is different from round robin. In fixed priority algorithm in clock1 the grant is given to master 1 and in next clock cycle it first check the request of master1 if Master1 have not generated any request then only it check the next master and give grant to it, here the priority of every master is fixed. Where as in round robin algorithm the priority of master is not fixed.
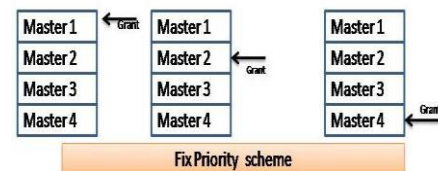

Fix Priority scheme

Figure 3 fixed priority algorithm

In proposed architecture combination of fixed priority and round robin algorithm is used. In proposed architecture shown in figure 3 there are sixteen priority logic with encoder, priority shift block, controller, counter, 16:1 grant mux. . Main objective of interface block is to follow the protocol Figure 4 show proposed architecture
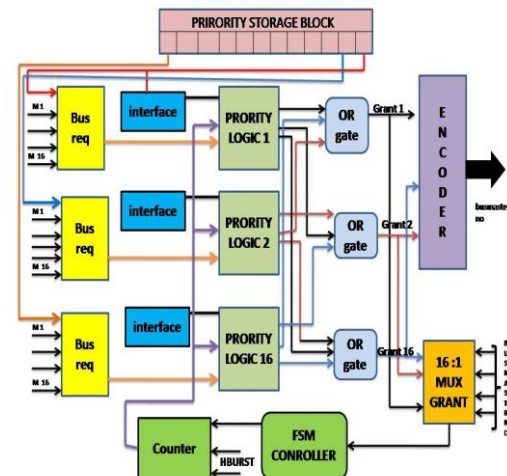

Figure 4 proposed architecture

2.1 Proposed Methodology

When number of master generate request at a same time then arbiter use arbitration algorithm to give grant to master. Arbitration algorithm use round robin scheme to choose next bus master. Round robin arbitration is overridden when master has locked the bus and retain highest priority. for next bus master, arbiter monitor all the bus request and choose high priority request; if arbiter not find any request it give grant to different master to access the bus for next transaction. The controller which is nearly state machine

kept track of all transaction of all different stations and it first state is start state it check the grant signal and if it is high then it make necessary signal high for further block interface. One of sixteen priority logic is enable at a time based by priority storage block. Initial the pin one of priority storage block is make high. it shift to next block when the data done is make high block, when it shift to next block, it disable the current working priority logic block and high the next priority logic block. All the sixteen bus request are received by enable box and then based on priority storage box enable high it pass it to suitable priority logic block. Interface block is providing to delay in order to maintained proper synchronization. When priority logic block received all bus request it now start scan all the request and when it found the highest priority it give grant to that master. The output of all priority logic block is OR gate and pass to encoder circuit. Encoder block encode all it input and output the bus master number, which serve as a selection line for 16:1 mux. Master when get grant will send address, and BURST signal, which define type of transfer. The output of 16:1 mux is given to controller which generate necessary signal to counter block. Then counter block depending upon the number of clock cycle required to complete transaction released data done signal, which further shift the priority storage block enable pin to next box. The given algorithm use logic of both fixed and round robin algorithm.sub priority box are arrange in fixed priority algorithm, pattern where as the suffering of priority among the priority logic block is done in round robin manner.

III. RESULT AND SIMULATION

Devices utilization summary
Implementation is done in Xilinx using vetex4 IC number xc4vfx12 and Synthesis and simulation done in MODELSIM 6.5. The speed of device is 9.516ns and max frequency 105.092MHZ.

main_arbiter Project Status			
Project File:	arbiter4.0.xise	Parser Errors:	No Errors
Module Name:	main_arbiter	Implementation State:	Synthesized
Target Device:	xc4vfx12-12sf363	•Errors:	No Errors
Product Version:	ISE 14.5	•Warnings:	486 Warnings (486 new)
Design Goal:	Balanced	•Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	•Timing Constraints:	
Environment:	System Settings	•Final Timing Score:	

Device Utilization Summary (estimated values)				[-]
Logic Utilization	Used	Available	Utilization	
Number of Slices	2183	5472		39%
Number of Slice Flip Flops	858	10944		7%
Number of 4-input LUTs	3779	10944		34%
Number of bonded IOBs	64	240		35%
Number of GCLKs	2	32		6%

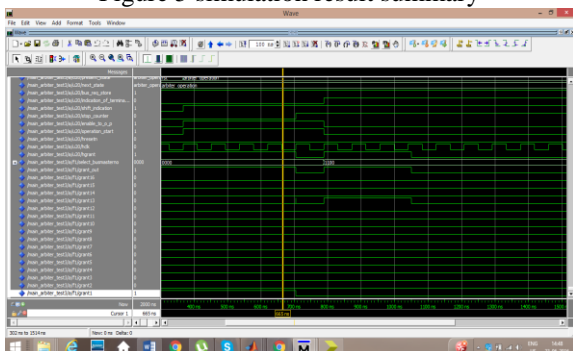Figure 5 simulation result summary

Figure 6 simulation result summary

IV. CONCLUSION AND FURTHER WORK

AMBA AHB proposed arbiter is capable to perform arbitration process based on the combination of round robin and fixed priority algorithm. The proposed AHB Arbiter is design using vetex4 IC no.xc4vfx12. In reference paper four masters is used where as proposed arbiter can handled the request of sixteen masters hence over all device utilization is increased respectively in different manner. The proposed arbiter give grant to master according to the arbitration algorithm. from the simulation result it is found that the overall speed of device is 9.516ns and maximum frequency 105.092mhz. The proposed AHB Arbiter is capable of handling the requested of sixteen master. The arbitration algorithm is combination of Round Robin and Fixed Priority algorithm. The further research work can be done as there are nine possible combination of arbitration for example combination of Fixed Priority algorithm and Dynamic Priority algorithm, combination of Round Robin algorithm and Dynamic Priority algorithm etc

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