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18-NM LOW-POWER CASCADED DESIGN OF PENTA MTJ-BASED DIGITAL CIRCUITS USING CLOCK GATING

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ABSTRACT: Advanced computing systems embed spin tronic devices to improve the leakage performance of conventional CMOS systems. High speed, low power, and infinite endurance are important properties of magnetic tunnel junction (MTJ), a spintronic device, which assures its use in memories and logic circuits. This paper presents a Penta MTJ-based logic gate, which provides easy cascading, self-referencing, less voltage headroom problem in pre charge sense amplifier and low area overhead contrary to existing MTJ-based gates. PentaMTJ is used here because it provides guaranteed disturbance free reading and increased tolerance to process variations along with compatibility with CMOS process. The logic gate is validated by simulation at the 45-nm technology node using a Verilog A model of the PentaMTJ.
Key words: spintronics, magnetic tunnel junction, nonvolatile logic, magnetic logic.

I. INTRODUCTION

The spintronics is under research going on the process such as the nonvolatile and low power. The spin has the store in information and charge that processing and potential to replace CMOS memory logic and memory. The sub micrometer has scalling of CMOS analysis the leakage power to another these power components. But digital of signal is represented on the conventional CMOS depents upon the logic function by absence and presence of the charge voltage or ground. The digital signal is coming up and down spin of electron. The principle of magnetic tunnel junction is the tunnel magneto resistance. The Magnetic tunnel junction are two level ferromagnetic layer and oxide layer which processes to improve the performance of CMOS logic circuits analysis for power dissipation. The logic gates of MTJ are storing process function to analysis for reduced the part of memory and interconnects power, delay to data in memory. The drawback of magnetic tunnel logic gate is power and delay as come the reported magnetic logic function. The magnetic tunnel junction comparing magnetic XOR gate and six of MTJ, but area requirement is less then increase the number of MTJ. Logic gate is required convert the voltage signal to current signal of magnitude for writing MTJ. The logic gates have only one of Magnetic tunnel junction can reduce the part of logic operation. Example for operating voltage and initial state. Friedman proposed implemented logic operation of linear function like NAND and NOR. Nonlinear function is the two input XOR/XNOR to be implemented using NAND/NOR gate operation. Horwitz and hill proposed to spin diode logic and CMOS logic gate but also CMOS based leakage power dissipation are constant voltage supply of the spin diode. The PentaMTJ is the two pin used to ferromagnetic layer and one free layer. It insulating oxide are used to magnesium oxide layer. The two resistance of state like conventional MTJ one is parallel state and other to anti parallel state. It is used to the realization of memory. Huda and sheikholeslami has proposed a novel Penta MTJ based spin transfer torque magnetic random access memory for disturbance free reading. It is also presented to a Penta MTJ based ternary content addressable memory and less delay. The process of Penta MTJ realization digital circuits has much advantage. First, magnetic logic gates based Penta MTJ is require to self-referencing circuits and due the presence of contrary to MTJ. Second, extra hardware is doing not needed for complementary output and presence of precharge sense amplifier sensing. Third, output of spintronics is direct sensed on the precharge sense amplifier. It is also no need to initialize the state of the output MTJ for sensing. The power consumption of sensing power is reduced power and speed of enhanced to use of Precharge sense amplifier.

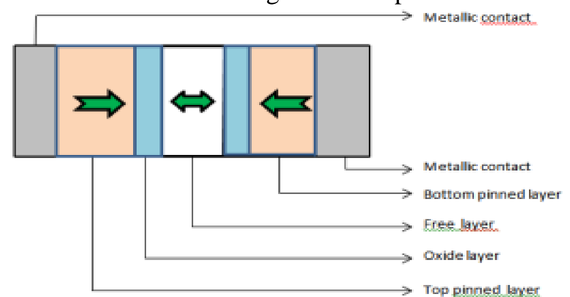

Fig. 1: Structure of PentaMTJ

II. STRUCTURE OF PENTA MTJ

The PentaMTJ is structure of two pinned layer such as top pinned layer and bottom pinned layer. The two pinned layer of magnetic process is opposite direction and then layer are fixed. The two states is assigned parallel to free layer. It is proposed to the PentaMTJ structure the less current of writing as compared the conventional MTJ. This is process of converting antiparallel to parallel state for one stack and another stack automatic come to anti parallel state.

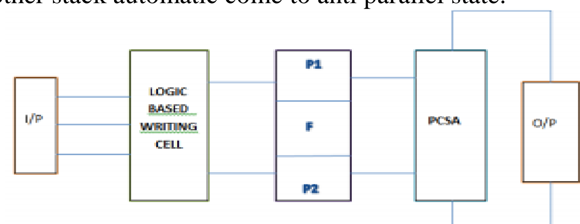

Fig. 2: Block diagram of logic gate based PentaMTJ

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There are the process of one stack null and another contrary to two different MTJ. The data is double barrier always assumed to that single barrier is model also valid for TMR ratio of double barrier. This two pinned layer and single free layer structure of PentaMTJ have already verified the macromagnetic simulation process. The pentaMTJ have low resistance of the conventional MTJ and it well of small value of oxide thickness analysis on MTJ. Perpendicular magnetic anisotropy based the spin transfer torque is the redudced switching voltage. While most modern computing technologies utilize Si complementary metal-oxide-semiconductor (CMOS) transistors and the accompanying CMOS logic family, alternative devices and logic families exhibit significant performance advantages. Though heretofore impractical, diode logic allows for the execution of logic circuits that are faster, smaller, and dissipate less power than conventional architectures. In this paper, magneto resistive semiconductor hetero junctions are used to produce the first complete logic family based solely on diodes. We utilize the diode magneto resistance states to create a binary logic family based on high and low currents in which a full range of logic functions is executed. The diode is used as a switch by manipulating its magneto resistance with current-carrying wires that generate magnetic fields. Using this device structure, we present basis logic elements and complex circuits consisting of as few as 10% of the devices required in their conventional CMOS counterparts. This diode logic family is therefore an intriguing potential replacement for CMOS technology as Si scaling reaches its inherent limits.Continued reduction in transistor size has provided the technological basis for marked circuit performance improvements, making possible billion transistor integrated circuits operating at gigahertz frequencies. This approach requires only the free layer magnetization to be reversed for a write operation. We also investigate InPlane Anisotropy (IPA) and Perpendicular-to-Plane Anisotropy (PPA) versions of the proposed device.

RECENT DEVELOPMENTS IN MAGNETIC TUNNEL JUNCTION MRAM

We summarize our progress on Magneto resistive Random Access Memory (MRAM) based on Magnetic Tunnel Junctions (MTJ). We have demonstrated MTJ material in the 1–1000 k- m2 range with MR values above 40%. The switching characteristics are mainly governed by the magnetic shape anisotropy that arises from the element boundaries. The switching repeatability, as well as hard axis selectability, is shown to be dependent on both shape and aspect ratio. MTJ memory elements were successfully integrated with 0.6 m CMOS technology, achieving read and program address access times of 14 ns in a 256 2 MRAM.Magneto resistive Random Access Memory (MRAM) based on integration of Magnetic Tunnel Junction (MTJ) and CMOS has the potential to be competitive with existing semiconductor memories. Key attributes of MRAM technology are nonvolatility and unlimited read and write endurance. In addition, it is anticipated that MRAM could operate at high speed and low voltage, with comparable densities. Controlling the resistance uniformity, switching behavior of magnetic bits, and integration of MTJ with CMOS are some of the key challenges to successful implementation of this technology.

MAGNETICALLY ENGINEERED SPINTRONIC SENSORS AND MEMORY

The discovery of enhanced magneto resistance and oscillatory interlayer exchange coupling in transition metal multi layers just over a decade ago has enabled the development of new classes of magnetically engineered magnetic thin-film materials suitable for advanced magnetic sensors and magnetic random access memories. Magnetic sensors based on spin-valve giant magnetoresistive (GMR) sandwiches with artificial antiferromagnetic reference layers have resulted in enormous increases in the storage capacity of magnetic hard disk drives. The unique properties of magnetic tunnel junction (MTJ) devices has led to the development of an advanced high performance non volatile magnet random access memory with density approaching that of dynamic randomaccess memory(RAM) and read-write speeds comparable to static RAM. Both GMR and MTJ devices are examples of spintronic materials in which the flow of spin-polarized electrons is manipulated by controlling, via magnetic fields, the orientation of magnetic moments in inhomogeneous magnetic thin film systems. More complex devices, including three-terminal hot electron magnetic tunnel transistors, suggest that there are many other applications of spintronic materials.

MAGNETIC ADDER BASED ON RACETRACK MEMORY

The miniaturization of integrated circuits based on complementary metal oxide semiconductor (CMOS) technology meets a significant slowdown in this decade due to several technological and scientific difficulties. Spintronic devices such as magnetic tunnel junction (MTJ) nanopillar become one of the most promising candidates for the next generation of memory and logic chips thanks to A magnetic processor based on spintronic devices is then expected to overcome the issue of increasing standby power due to leakage currents and high dynamic power dedicated to data moving. The proposed multi-bit MA circuit promises nearly zero standby power, instant ON/OFF capability, and smaller die area. By using an accurate racetrack memory spice model, we validated this design and simulated its performance such as speed, power and area, etc.

III. EXISTING SYSTEM

Advanced computing systems embed spintronic devices to improve the leakage performance of conventional CMOS systems. High speed, low power, and infinite endurance are important properties of magnetic tunnel junction (MTJ), a spintronic device, which assures its use in memories and logic circuits. This paper presents a PentaMTJ-based logic gate, which provides easy cascading, self-referencing, less voltage headroom problem in precharge sense amplifier and low area overhead contrary to existing MTJ-based gates. PentaMTJ is used here because it provides guaranteed disturbance free reading and increased tolerance to process variations along with compatibility with CMOS process.

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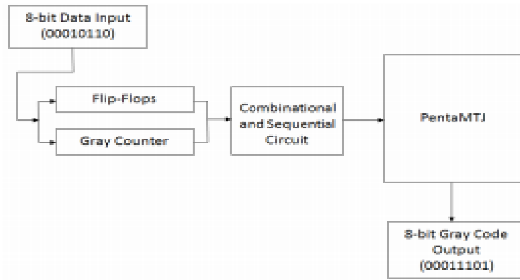

Fig 3: Proposed method block diagram

Tunnel magneto resistance (TMR) is a magneto resistive effect that occurs in a magnetic tunnel junction (MTJ), which is a component consisting of two ferro magnets separated by a thin insulator. If the insulating layer is thin enough typically a few nanometers, electrons can tunnel from one ferro magnet into the other. Since this process is forbidden in classical physics, the tunnel magneto resistance is a strictly quantum mechanical phenomenon. Magnetic tunnel junctions are manufactured in thin film technology. On an industrial scale the film deposition is done by magnetron sputter deposition; on a laboratory scale molecular beam epitaxy, pulsed laser deposition and electron beam physical vapor deposition are also utilized. The junctions are prepared by photolithography.

IV. PROPOSED SYSTEM

Logic gates act as basic building blocks for both combinational and sequential circuits. The basic structure of PentaMTJ-based logic gate is divided into three parts. Fig. 4 shows the PentaMTJ-based XOR/XNOR logic gates. For different logic gates, different writing circuitry is required but the sensing portion remains identical. Therefore, the information is stored in the pinned layers using series or parallel combinations of transistors as per the logic. Storing logic in PentaMTJ is designed such that for storing 1, all logic combinations with high output are combined and the net expression is evaluated using K -map and for storing 0, the complement of the expression is evaluated. Fig. 5 shows the simulation results of logic gates with both normal and complementary outputs. A and B are the two inputs, 0 output corresponds to the discharging of PCSA whereas 1 means no discharging for normal output. The evaluation phase begins after precharging the outputs of the PCSA to VDD using the clock CLK.

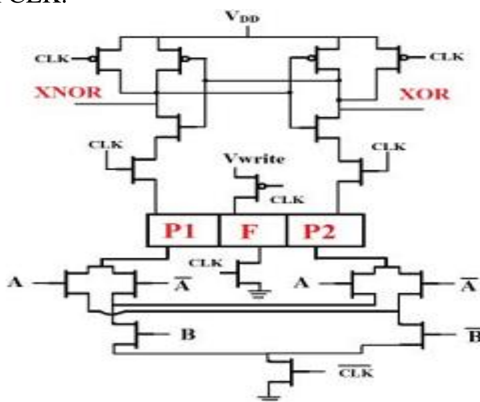

Fig. 4. XOR/XNOR gates using PentaMTJ

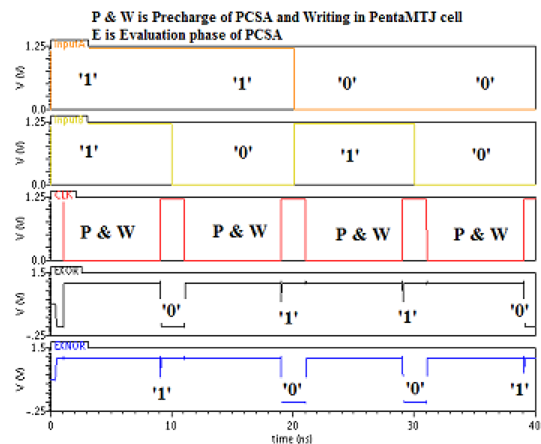

Fig. 5. Simulation result of XOR/XNOR gate

3-bit GRAY COUNTER

Sequential logic circuits differ from combinational logic circuits as the output of a sequential logic circuit depends upon both the previous output (present state) and the present input. A 3-bit Gray counter is a sequential circuit whose successive states differ in only one digit. The present state in a sequential circuit like Gray counter is stored in flip-flops, which is very power consuming under standby condition. Use of MTJ/PentaMTJ in a sequential circuit is beneficial because in case of unintentional shutdown, the counter can be restored from its previous state instead of its initial state. The previous state is restored from PentaMTJ within few hundred picoseconds. In the Gray counter, PCSA is used for sensing to generate the next state, PentaMTJ for present state storage and the writing circuitry to assign the next state to the present state.

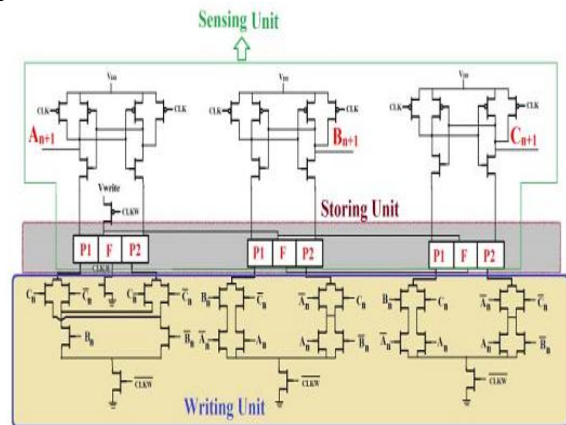

Fig. 6. Circuit diagram of 3-bit Gray counter using PentaMTJ.

Fig. 6 shows the circuit diagram of a 3-bit Gray counter comprising of three PentaMTJs for storage, three PCSAs for sensing, and a writing circuit according to the characteristic (1). An, Bn, and Cn are the stored outputs (present state) whereas An+1, Bn+1, and Cn+1 signify the next state which is to be stored in a PentaMTJ. It starts operating by writing in PentaMTJ using the clock CLKW with a pulsewidth of 1.5 ns. To accomplish the writing in PentaMTJ in 1.5 ns, a clock CLKW with 2-ns time period and 1.5-ns pulsewidth is

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generated. The precharging and then sensing are performed when CLKW is high (500 ps) using a short duration low CLK (300 ps) pulse followed by a short duration high CLKR pulse (200 ps). The same process is repeated until the counter stops. It may be noted that nMOS MN2 and MN3, as shown in Fig. 2, are not used in the Gray counter because the writing and precharging are not done simultaneously. The writing is done according to the previous state and, therefore, precharging and writing are not done at the same time. Fig. 6 shows the simulation results with A n+1 being the least significant bit and Cn+1, the most significant bit

$$A_{n+1} = \overline{B_n \oplus C_n}$$
$$B_{n+1} = A_n \overline{C_n} + \overline{A_n} B_n$$
$$C_{n+1} = A_n C_n + \overline{A_n} B_n.$$

RESULTS

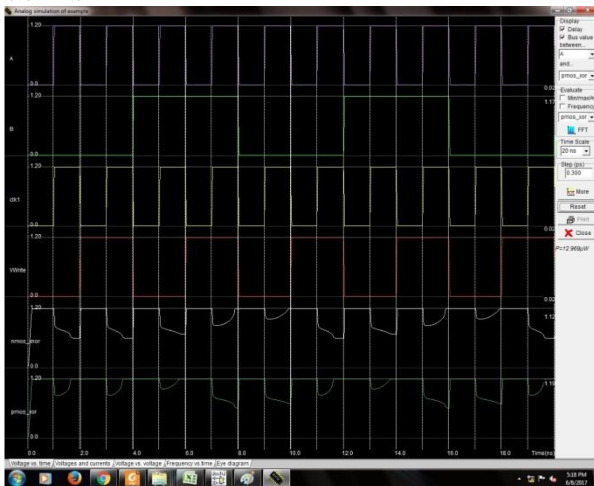

Fig. XOR/XNOR Gate Simulation

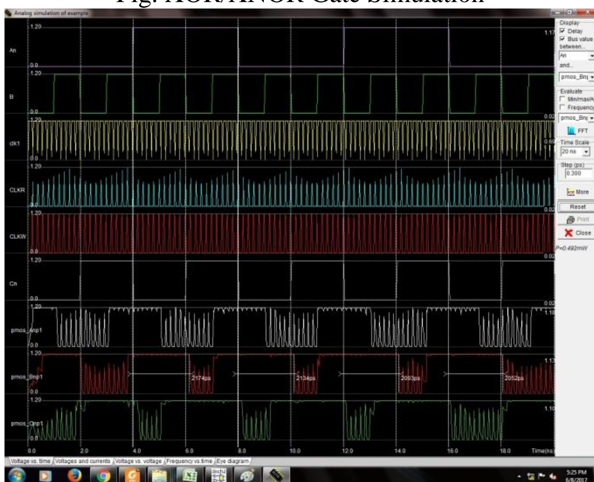

Fig. Gray Counter Simulation

V. CONCLUSION

It is low power, short interconnect delay and nonvolatile and the pentaMTJ of logic reduced area based logic function. The future scope of this pentaMTJ is increase the switching speed and the reduced current density required for switching.The attractive features of MTJ/PentaMTJ-based CMOS logic are low static power, short interconnect delay, and effective power gating because of nonvolatility. PentaMTJ-based logic decreases the area overhead by removing the intermediate circuitry needed for conversion of voltage to current or current to voltage. Moreover, no initial condition is required for performing the logic operation and self referencing property removes the extra MTJs used for referencing. PentaMTJ also provides guaranteed disturbance free reading and increased tolerance to process variations due to its differential nature.

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