

DCT WITH VEDIC MULTIPLIER

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Abstract: Multiplier is an important fundamental functional unit in arithmetic operations. Multiplication-based on operations of conventional methods takes long time to find the result of the respective functions thereby decreasing the efficiency of the processors. Intensive Arithmetic Multiplication functions are currently implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform(FFT), filtering and in microprocessors in its arithmetic and logic unit. Since multiplication dominates the execution time of most DSP algorithms, so there is a need of high speed multiplier. Multiplication is an important and impacting factor in evaluating the processing of instructions processed per unit in all types of DSP processor. The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications. Therefore an efficient throughput processor is required for getting the desired performance in most of the Digital signal processing applications. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Multipliers using vedic mathematics calculates the required multiplication in less time thereby consuming less Gates, LUTs & IOBs. Employing this technique in the computation algorithms will reduce the complexity, execution time, power etc.

Keywords: Vedic Multiplier, DCT, Reversible Gate, Vedic Mathematics, FPGA, Xilinx

I. INTRODUCTION

VEDIC MATHEMATICS

The word 'Vedic' means the store-house of all knowledge derived from the word 'veda'. It was introduced by Jagadguru Swami Sri Bharati Krishna Tirthaji Maharaja as Vedic Mathematics. Vedic mathematics consists of 16 Vedic Sutras.

VEDIC SUTRAS

Vedic mathematics consisting of 16 Sutras deals with various branches of mathematics like arithmetic, algebra, geometry etc. Below are the 16 Sutras definitions:-

- 1) (Anurupyeh) Shunyamanyat – The work of it is if the one is in ratio; then other is zero
- 2) Chalana-Kalanabyham – It means differences and similarities.
- 3) Ekadhikina Purvena – It means by one more than the previous one
- 4) Ekanyunena Purvena – It means by one less than the previous one
- 5) Gunakasamuchyah – It means the factors of the sum is

equal to the sum of the factors

- 6) Gunitasamuchyah – It means the product of the sum is equal to the sum of the product
- 7) Nikhilam Navatashcaramam Dashatah – It means all from 9 and the last from 10
- 8) Paraavartya Yojayet – It means Transpose and adjust.
- 9) Puranapuranyam – It means by the completion or noncompletion
- 10) Sankalana-vyavakalanabhyam – It means by addition and by subtraction
- 11) Shesanyakena Charamena – It means the remainders by the last digit
- 12) Shunyam Saamyasamuccaye – It means when the sum is the same that sum is zero
- 13) Sopaantyadvayamantyam – It means the ultimate and twice the penultimate
- 14) Urdhva-tiryakbyham – It means Vertically and crosswise
- 15) Vyastisamanstih – It means Part and Whole
- 16) Yaavadunam – It means Whatever the extent of its Deficiency

II. URDHVA-TIRYAKBYHAM SUTRA

The working of this multiplier is based on an algorithm Urdhva Tiryakbyham (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbyham Sutra is a common multiplication formula which is applicable to all cases of multiplication. Its literal meaning is "Vertically and crosswise". It is based on the principle through which the generation of all partial products can be done with the concurrent addition of these partial products. The generation of partial products and their summation is obtained using Urdhva Tiryakbyham explained in fig 2.1. The generalized form of the algorithm can be for $n \times n$ bit number. In this the partial products and their sums are calculated in parallel. Apart from it the multiplier is independent of the clock frequency of the processor. Therefore the multiplier will require the same amount of time to calculate the product and all the partial products and hence it is independent of the clock frequency. Therefore it can be said that the advantage of vedic multiplier is that that it reduces the need of microprocessors to operate at increasingly high clock frequencies. While a higher clock frequency generally results in increased processing power, its disadvantage is that it also increases power dissipation which results in higher device operating temperatures. By using the Vedic multiplier, microprocessors the designers can easily find a way around the problems to avoid fatal device failures.

MULTIPLICATION OF TWO DIGIT NUMBER 341×562

Let's have an example of multiplication of 2 three digit number using vedic mathematics UT sutra.

- 1) Step 1 - 1's digit: $2*1 = 22$ Step 2 - 10's digit: $2*4+6*1 = 8+6 = 14$ (write a 4, carry a 1)
- 3) Step 3 100's digit: $2*3+4*6+5*1 = 6+24+5 = 35$ (write a 5, carry a 3) observe at this point that we have reached the end of the top number, that is to say, 2 cannot be multiplied by anything else, as there are no more digits. Therefore, it can be said that for the thousands digit we shall multiply 6 and 3 first, and then for the ten thousands digit, 5 and 3. (read on for the steps)
- 4) Step 4 1000's digit: $6*3 + 5*4 = 18+20 = 38$ (write an 8, carry a 3)
- 5) Step 5 10,000's digit: $5*3 = 15$ (since it is the end of the multiplication, so simply write 15 rather than carry a 1)
- 6) At the end all the carries are added to produce the final answer: 191642

it should be noted that the 2 numbers need not have the same number of digits. For e.g, if a 2-digit number were to be multiplied by a 3-digit number, use the formula for 3-digit by 3-digit multiplication and do zero padding for the missing digits.

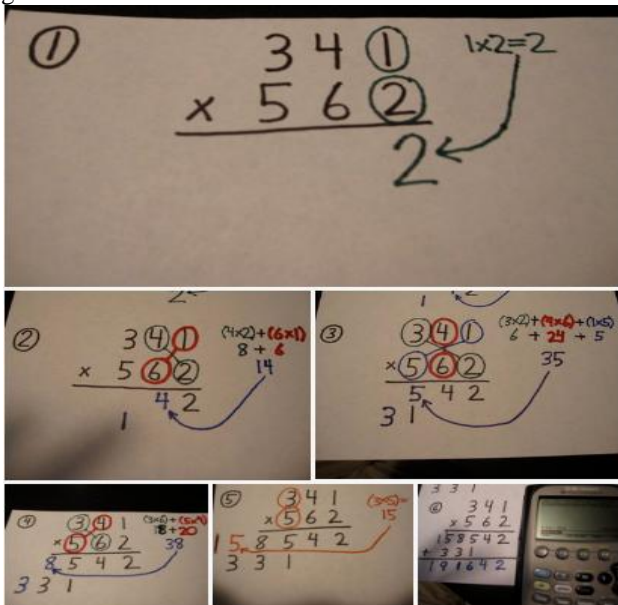


Fig. Vedic Multiplication Example of 341*562

III. ALGORITHM FOR VEDIC MULTIPLIER

The Vedic Multiplication Method as per follow:
 Following methods aids for the faster Multiplication, reduces time and increases the throughput via Digital Logic which compare with DCT process from DSP[10] with input factor as pixel values which gives better and faster result.
 Vedic Mathematics works on the 16 algorithms or sutras developed and derived from ancient Vedic texts. This particular method for fast multipliers used in digital image and signal processing techniques is named Urdhva Triyakbhyam is more efficient and which consume less time and improves the speed and performance. This method performs multiplication in crosswise and vertically manner it makes all the numeric computations faster by generating partial product and sum in single iteration[4]. The vedic multipliers calculates faster than the conventional multipliers. This gives a scheme for hierarchical multiplier design. The

design is faster, consumes smaller area and has less power consumption as compared to the conventional multipliers.

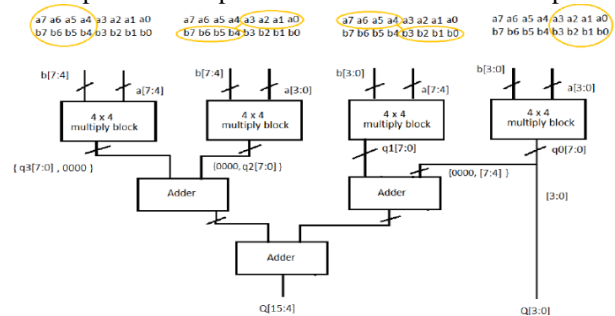


Fig Block diagram of 16x16 UT Multiplier

IV. PERFORMANCE ANALYSIS

The conventional multiplier requires more gates and so the processor using simple conventional multipliers speed becomes slow. The Table 1 and Table 2,3 gives the summary of the maximum path delay and number of Slices, LUTs and IOBs for both conventional multiplier and Reversible Gates [vedic maths] multipliers. The tables clearly shows that reversible gates are more efficient than conventional multiplier as uses less number of LUTs, Slices, IOBs ; thereby making the processor speed fast using reversible gates [vedic math's].

Table 1: Comparison of speed using various multipliers

Technology used	Maximum Path Delay
4x4 conventional multiplier	13.201 ns
4x4 multiplier using reversible gates	12.972 ns
8x8 conventional multiplier	26.177 ns
8x8 multiplier using reversible gates	24.484 ns
16x16 conventional multiplier	45.183 ns
16x16 multiplier using reversible gates	40.214 ns

Table 2: 16x16 multiplier conventional multiplier

Number of Slices:	525 out of 704 (74% utilized)
Number of 4 input LUTs:	923 out of 1408 (65% utilized)
Number of bonded IOBs:	105 out of 108 (97% utilized)

Table 3: 16x16 multiplier using reversible gates[vedic maths]

Number of Slices:	510 out of 704 (72% utilized)
Number of 4 input LUTs:	893 out of 1408 (63% utilized)
Number of bonded IOBs:	65 out of 108 (60% utilized)

An application of 8x8 multiplier using reversible gates can be used in image processing of DCT algorithm.

DCT algorithm without reversible gates input and output information

Input – force clock

Leading edge – 1

Trailing edge – 0

Period – 100 to 10000

lastout1-lastout63 – decoder outputs

The output of input pixel values using DCT gets decompressed by +/- 5 of pixel values using Verilog which is hardly recognizable by a human eye and its computation becomes very fast when implemented using Vedic multiplier.

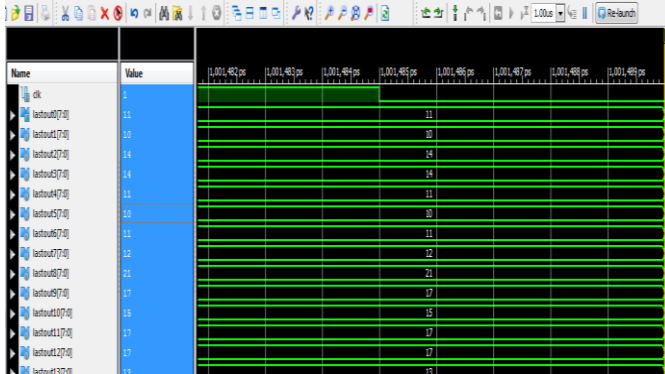


Figure1:- DCT output using Vedic multiplier

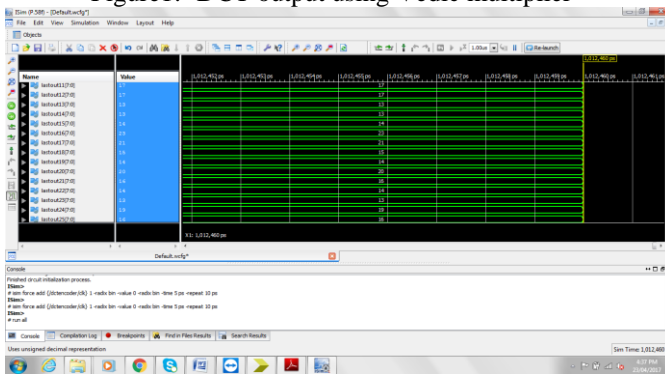


Figure2:- DCT output using Vedic multiplier

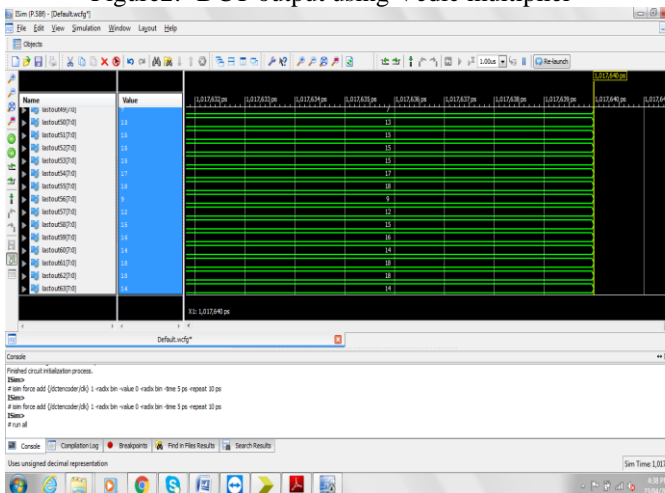


Figure3:- DCT output using Vedic multiplier

This is a remarkable result as DCT algorithm using Vedic mathematics gives nearly 87.17 % of efficiency. Therefore the DCT algorithm using Vedic Mathematics can be used vastly in Image Processing due to its high efficiency.

V. CONCLUSION

Thus an efficient Vedic multiplier with high speed, low power and consuming little bit wide area was designed and implemented on device Spartan and simulated using ISE simulator. It was found that the multiplier based on vedic sutras had execution delay of almost half of that of binary multiplier.

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