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DESIGN OF LOW POWER DYNAMIC FEEDBACK CONTROL SINGLE-ENDED 8T -SRAM CELL

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Abstract: Aggressively scaling the supply voltage of SRAMs greatly minimizes their active and leakage power, a dominating portion of the total power in modern ICs. Hence, energy constrained applications, where performance requirements are secondary, benefit significantly from an SRAM that offers read and write functionality at the lowest possible voltage. However, bit-cells and architectures achieving very high density conventionally fail to operate at low voltages. This paper describes a high density SRAM in 65 nm CMOS that uses an 8T bit-cell to achieve a minimum operating voltage of 350 mV. Buffered read is used to ensure read stability, and peripheral control of both the bit-cell supply voltage and the read-buffer's foot voltage enable sub- write and read without degrading the bit-cell's density. The plaguing area-offset tradeoff in modern sense-amplifiers is alleviated using redundancy, which reduces read errors by a factor of five compared to device up-sizing. At its lowest operating voltage, the entire 256 kb SRAM consumes 2.2 W in leakage power.

Index Terms: Cache memories, CMOS memory circuits, leakage currents, low-power electronics, redundancy, SRAM chips.

I. INTRODUCTION

Aggressive scaling of transistor dimensions with each technology generation has resulted in increased integration density and improved device performance. Leakage current increases with the scaling of the device dimensions. Increased integration density along with the increased leakage necessities ultralow-power operation in the present power constrained design environment. The power requirement for battery-operated devices such as cell phones and medical devices is even more stringent. Reducing the supply voltage reduces the dynamic power quadratically and leakage power linearly to the first order. Hence, supply voltage scaling has remained the major focus of low-power design. This has resulted in circuits operating at a supply voltage lower than the threshold voltage of a transistor [1]. However, as the supply voltage is reduced, the sensitivity of the circuit parameters to process variations increases. Process variations limit the circuit operation in the sub threshold region, particularly the memories. Embedded cache memories are expected to occupy 90% of the total die area of a system-on-a-chip (SoC). Nanoscaled SRAM bit cells having minimum-sized transistors are vulnerable to inter-die as well as intra-die process variations. Intra-die process variations include random dopant fluctuation (RDF) and line edge roughness (LER), etc. This may result in a threshold voltage mismatch between the adjacent transistors in a memory cell [4]. Coupled with inter-die and intra-die process variations, lower supply voltage operation results in various memory failures, i.e., read failure, hold failure, access time failure, and write failure [4]. Memory failure probability is predicted to be higher in the future technology nodes [5]. Adaptive circuit techniques such as source biasing, and dynamic have been proposed to improve the process variation tolerance [6]. Self-calibration techniques to achieve low-voltage operation while keeping the failure probability under control have also been proposed [7]. The 6-transistor (6T) cell which uses a cross-coupled inverter pair is the de facto memory bit cell used in the current SRAM designs. Different types of SRAM bit cells have been proposed to improve the memory failure probability at a given supply voltage. For a stable SRAM bit cell operating at lower supply voltages, the stability of the inverter pair should be improved. None of the aforementioned bit cells has a mechanism to improve the stability of the inverter pair under process variations. We propose a Schmitt trigger based differential bit cell having built-in feedback mechanism for improved process variation tolerance.

In particular:

1) We have proposed a novel Schmitt trigger based, differential, 10-transistor SRAM bitcell with built-in feedback mechanism. It requires no architectural change compared to the 6T cell architecture. It can be used as a drop-in replacement for present 6T based designs.

2) We have demonstrated that with respect to 6T cell, the proposed Schmitt trigger based bitcell gives better read stability, better write-ability, improved process variation tolerance, lower read failure probability, low-voltage/low power peration, and improved data retention capability at ultralow voltage.

3) We have fabricated a test chip in 0.13 m logic process technology and validated the proposed technique. An SRAM array containing the proposed memory bitcell is functional at 160 mV of supply voltage. To maintain the clarity of the discussion, the "10T cell" is referred as the memory cell reported. The proposedSchmitt Trigger (ST) based 10T memory cell is referred as the "ST bitcell" hereafter. The rest of this paper is organized as follows. In Section II, the proposed ST bitcell operation is described. In Section III, comparison is made among 6T/8T/10T/ST bitcells for various SRAM metrics.

II. EXISTING SYSTEM

An SRAM cell has three different states: standby (the circuit is idle), reading (the data has been requested) or writing (updating the contents). SRAM operating in read mode and write modes should have "readability" and "write stability", respectively. The three different states work as follows:

Standby
If the word line is not asserted, the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross-coupled inverters formed by M1 – M4will continue to reinforce each other as long as they are connected to the supply.

Reading
In theory, reading only requires asserting the word line WL and reading the SRAM cell state by a single access transistor and bit line, e.g. M6, BL. Nevertheless, bit lines are relatively long and have large parasitic capacitance. To speed up reading, a more complex process is used in practice: The read cycle is started by precharging both bit lines BL and BL, i.e., driving the bit lines to a threshold voltage (midrange voltage between logical 1 and 0) by an external module (not shown in the figures). Then asserting the word line WL enables both the access transistors M5 and M6, which causes the bit line BL voltage to either slightly drop (bottom NMOS transistor M3 is ON and top PMOS transistor M4 is off) or rise (top PMOS transistor M4 is on). It should be noted that if BL voltage rises, the BL voltage drops, and vice versa. Then the BL and BL lines will have a small voltage difference between them. A sense amplifier will sense which line has the higher voltage and thus determine whether there was 1 or 0 stored. The higher the sensitivity of the sense amplifier, the faster the read operation.

Writing
The write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL to 1 and BL to 0. This is similar to applying a reset pulse to an SR-latch, which causes the flip flop to change state. A 1 is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. This works because the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself so they can easily override the previous state of the cross-coupled inverters. In practice, access NMOS transistors M5 and M6 have to be stronger than either bottom NMOS (M1, M3) or top PMOS (M2, M4) transistors. This is easily obtained as PMOS transistors are much weaker than NMOS when same sized. Consequently when one transistor pair (e.g. M3 and M4) is only slightly overridden by the write process, the opposite transistors pair (M1 and M2) gate voltage is also changed. This means that the M1 and M2 transistors can be easier overridden, and so on. Thus, cross-coupled inverters magnify the writing process.

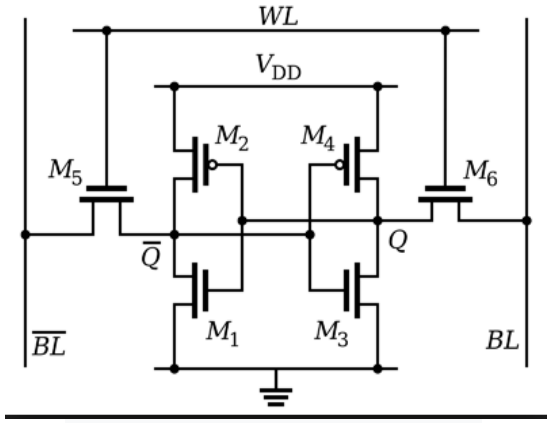


Fig 1: 6-Transistor CMOS SRAM cell

III. PROPOSED SYSTEM

To make a cell stable in all operations, single-ended with dynamic feedback control (SE-DFC) cell is presented in Fig.2. The single-ended design is used to reduce the differential switching power during read–write operation. The power consumed during switching/ toggling of data on single bit line is lesser than that on differential bit-line pair. The SE-DFC enables writing through single nMOS in 8T. It also separates the read and write path and exhibits read decoupling. The structural change of cell is considered to enhance the immunity against the process–voltage–temperature (PVT) variations. It improves the static noise margin (SNM) of 8T cell in sub threshold/near-threshold region. The proposed 8T has one cross coupled inverter pair, in which each inverter is made up of three cascaded transistors. These two stacked cross-coupled inverters: M1–M2–M4 and M8–M6–M5 retain the data during hold mode. The write word line (WWL) controls only one nMOS transistor M7, used to transfer the data from single write bit line (WBL). A separate read bit line (RBL) is used to transfer the data from cell to the output when read word line (RWL) is activated. Two columns biased feedback control signals: FCS1 and FCS2 lines are used to control the feedback cutting transistors: M6 and M2, respectively.

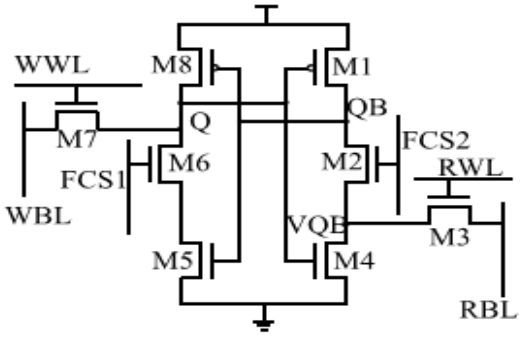


Fig. 2. Proposed 8T. (a) Schematic.

Write Operation
The feedback cutting scheme is used to write into 8T. In this scheme, during write 1 operation FCS1 is made low which switches OFF M6. When the RWL is made low and FCS2 high, M2 conducts connecting Complementary Q (QB) to the ground. Now, if the data applied to word bit line (WBL) is 1

and WWL is activated (Table II), then current flows from WBL to Q and creates a voltage hike on Q via M7-writing 1 into the cell. Moreover, when Q changes its state from 0 to 1, the inverter (M1– M2–M4) changes the state of QB from 1 to 0. To write a 0at Q, WWL is made high, FCS2 low and WBL is pulled to the ground. The low going FCS2 leaves QB floating, which can go to a small negative value, and then the current from pull-up pMOS M1 charges QB to 1. The WT is measured as the time taken by WWL signal-to-rise to VDD/2 until the storage nodes intersect each other. The simulations for WT were performed at all process corners. The WT (for write 1 and write 0) for 8T increases with the decrease in power supply. The WT is highest for slow nMOS and slow pMOS (SS) worst case corner. During write 1/0 operation, the power consumption of 8T is highest for fast nMOS and fast pMOS (FF) process corner dominated by the fast switching activities. As write 0 operations is faster than write 1, the write 0 power consumption during write 0 is more as compared with that of write 1.

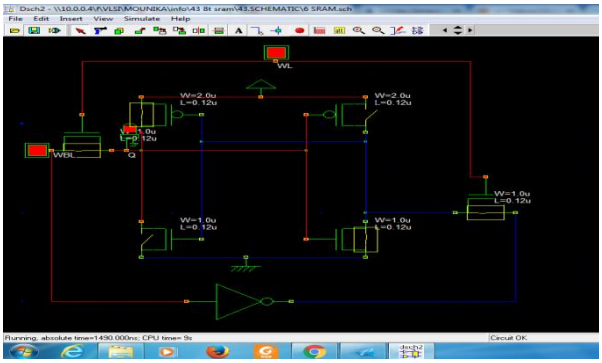
Read Operation

The read operation is performed by precharging the RBL and activating RWL. If 1 is stored at node Q then, M4 turns ON and makes a low resistive path for the flow of cell current through RBL to ground. This discharges RBL quickly to ground, which can be sensed by the full swing inverter sense amplifier. Since WWL, FCS1, and FCS2 were made low during the read operation, therefore, there is no direct disturbance on true storing node QB during reading the cell. The low going FCS2 leaves QB floating, which goes to a negative value then comes back to its original 0 value after successful read operation. If Q is high then, the size ratio of M3 and M4 will govern the read current and the voltage difference on RBL. During read 0 operations, Q is 0 and RBL holds precharged high value and the inverter sense amplifier gives 0 at output. Since M2 is OFF so virtual QB (VQB) is isolated from QB and this prevents the chance of disturbance in QB node voltage which ultimately reduces the read failure probability and improves the RSNM. During read operation, if FCS1/FCS2 turns 1 before RWL is turned 0 then QB and VQB can share charge. As WWL is 0 no strong path exists between WBL and Q, and any disturbance in QB will not affect Q. After that if RWL goes low, the positive feedback will restore the respective states (Q = 1 and QB = 0).

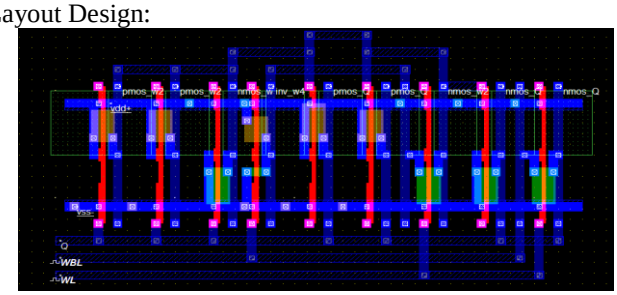
IV. SIMULATION RESULTS

Existing system:

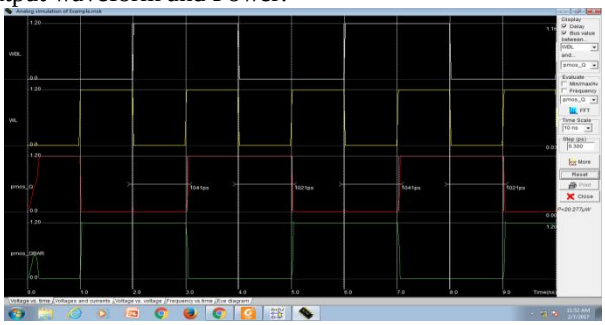
Schematic:



Layout Design:

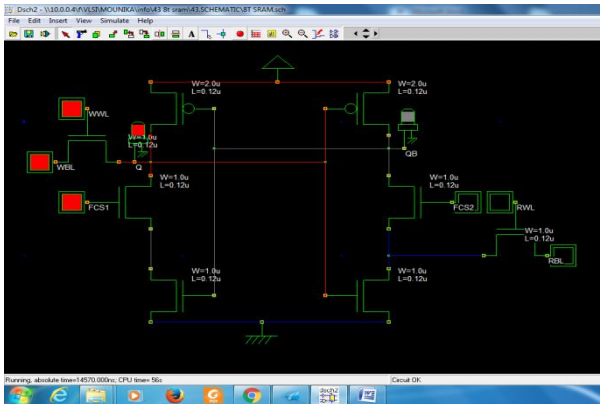


Output waveform and Power:

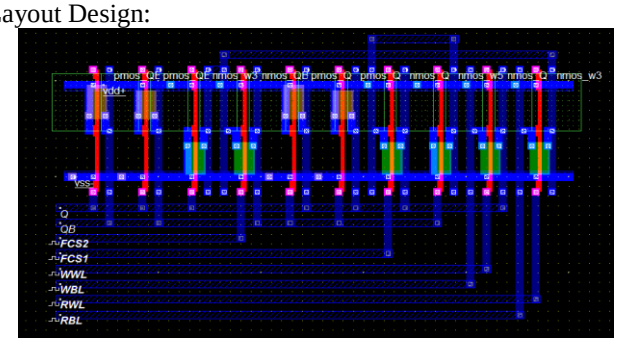


Proposed System:

Schematic:



Layout Design:



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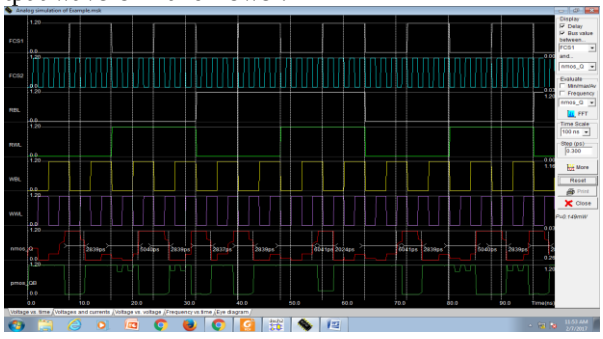

V. CONCLUSION

Voltage scaling is an effective strategy for minimizing the power consumption of SRAMs. Further, as SRAMs continue to occupy a dominating portion of the total area and power in modern ICs, the resulting total power savings are significant. Unfortunately, however, conventional SRAMs, based on the 6T bit-cell, fail to operate at Low voltages, because of reduced signal levels and because of increased variation. To address these limitations, an 8T bit-cell is incorporated, it achieves full read and write functionality. The advantage of reduced power consumption of the proposed 8T cell enables it to be employed for battery operated SoC design. Future and applications of the proposed 8T cell can potentially be in low/ULV and medium frequency operation like neural signal processor, sub threshold processor, wide-operating-range IA-32 processor, fast Fourier transform core, and low voltage cache operation.

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