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ULTRA WIDE BAND PLL USING LC VCO

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Abstract: Phase Locked Loops are used in almost every communication system. Some of its uses include recovering clock from digital data signals, performing frequency, phase modulation and demodulation, recovering the carrier from satellite transmission signals and as a frequency synthesizer. A frequency synthesizer is a circuit design that generates a new frequency from a single stable reference frequency. One approach to this necessity could be to use crystal oscillators. It is not only impractical, but is impossible to use an array of crystal oscillators for multiple frequencies. Therefore some other techniques must be used to circumvent the problem. The main benefit of using Phase Locked Loop technique in frequency synthesizer is that it can generate frequencies comparable to the accuracy of a crystal oscillator and offer other advantages mentioned previously. For this reason most of the communication design makes use of a PLL frequency synthesizer. Phase locked loop is an excellent research topic as it covers many disciplines of electrical engineering such as Communication Theory, Control Theory, Signal Analysis, Noise Characterization, Design with transistors and op-Amps, Digital Circuit design and non-linear circuit analysis.

Keywords: CMOS, LC,VCO.PLL, Oscillator, PFD,XOR PHASE

I. INTRODUCTION

A PLL is essentially a feedback loop that bolts the on-chip clock phase to that of an input clock or signal. High-performance PLLs and clock supports are broadly utilized inside a digital system for two purposes: clock generation, and timing recovery. For clock generation, since off-chip reference frequencies are restricted by the greatest frequency of swaying frequency reference, (Typically in the scope of 10 MHz) a PLL gets the reference clock and increases the frequency to the multi-gigahertz operating frequency. The high-frequency clock is then headed to all parts of the chip. Timing recovery relates to the data communication between chips. As data rates increment to fulfil the expansion in on-chip preparing rate, the phase connection between the input data and the on-chip clock is not settled. To dependably get the high-speed data, a PLL locks the clock phase that examples the data to the phase of the input data. Phase bolted loop is closed loop control system that contrasts the yield phase and the input phase. High-performance digital systems utilize clocks to arrangement operations and synchronize between functional units and between ICs. Clock frequencies and data rates have been expanding with every generation of preparing technology and processor engineering. Inside the digital systems, very much coordinated clocks are produced with phase-bolted loops (PLLs). The fast increment of the systems clock frequency has challenges in creating and circulating the clock with low instability.

II. RELATED WORK

Pietro Andreani et al [1] give two 1.8 gigahertz CMOS voltage-controlled oscillators (VCOs), tuned by Associate in Nursing inversion-mode MOS varactor Associate in Nursing an accumulation- mode MOS varactor, severally. Each VCOs show a lower power consumption and a lower section noise than a reference VCO tuned by an additional normally used diode varactor. The simplest overall performance is displayed by the accumulation-mode MOS varactor VCO. The VCOs were enforced in an exceedingly customary 0.6 /spl mu/m CMOS method

Hisao-Chin Chen et al [2] give in the TA miniaturized (0.224 mm2) 4.5~5.0 gigacycle per second 3-D LC VCO possessing area- efficient metal-6 on-chip inductors is enforced in0.18 um 1P6M CMOS technology. With inductors directly higher than the opposite devices, this VCO shows a measured section noise of -124.6 dBc/Hz at one megacycle per second offset from the 4.9 gigacycle per second carrier whereas dissipating twenty four mW.

Yuan-Kai Chu et al [3] give the wide-band CMOS VCO supported the electrical device feedback from ancient circuit to our projected work. The beginning up condition of the standard cross- coupled combine is expressed by the high frequency model. The wide band technique of this structure springs with the assistance of the high frequency model of the semiconductor device The menstruation results of the VCO exhibits the figure of benefit, core power consumption and output power at provide voltage zero.8 V square measure –193.1 dBc/Hz, 4.4 mW and –2.3 dBm, severally.

Wei-Hao Chiu et al [4] give the presents a fast-locking technique for phase-locked loops (PLLs). Within the projected technique, the polarity and magnitude of the section error at the phase-frequency detector (PFD) input is unendingly monitored throughout the protection method. The detected section error is then coarsely stipendiary by dynamically dynamical the divide magnitude relation of the frequency divider. The projected technique is incorporated within the style of a 5- GHz PLL. made-up within the TSMC 0.18-μm CMOS technology, the entire PLL dissipates eleven mA from a 1.8-V supply.

Nesreen Ismail et al [5] Falling-Edge PFD uses solely twelve transistors and preserves the most characteristics of the standard PFD. its enforced victimization Silterra 0.18 μm CMOS method. It consumes 6.6 μW once in operation at fifty megacycles per second clock frequency with 1.8V voltage provide. It free dead zone and operates up to a pair of.5 GHz. It will be utilized in high speed and low power consumption applications.

Rayan Lee Bunch et al [6] give the MOS varactors are used extensively as tunable parts within the tank circuits of RF voltage- controlled oscillators (VCOs) supported sub micrometer CMOS technologies. MOS varactor topologies embody standard D = S = B connected, inversion-mode (I-MOS), and accumulation- mode (A-MOS) structures. This paper presents an in depth analysis of this large-signal impact. Simulated results are compared to measurements for associate example a pair of.5-GHz complementary - Gm LC VCO victimization I-MOS varactors enforced in zero.35-µm CMOS technology.

Felice Liccardo et al [7] give the easy, robust, and quick synchronization technique to find the point of the positive sequence of a three-phase ac system. The algorithmic program was derived from a customary phase-locked-loop (PLL) circuit supported the pq theory.

It guarantees correct part protection and is powerful with relevance ac distortions like harmonics, sub harmonics, and voltage imbalance. The management model for the projected PLL system was supported the quality PLL structure. The projected technique was tested and compared with alternative algorithms by means that of simulations. The experimental and simulation results square measure shown and compared.

III. PROPOSED MODEL

In this part, A Phase Locked Loop or a PLL is a feedback control circuit. As the name proposes, the phase bolted loop works by attempting to bolt to the phase of an extremely exact input signal using its negative feedback way. An essential type of PLL as in Figure 1 comprises of three principal functional squares in particular.

- A Phase Detector (PD)
- A Loop Filter (LF)
- A voltage controlled oscillator (VCO)

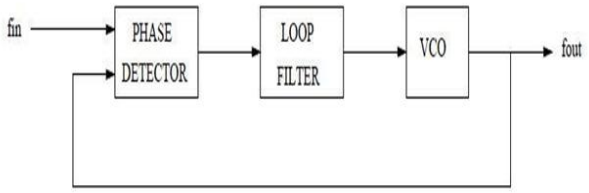

Figure 1 Block diagram of basic PLL

Phase Detector:-

The part of a Phase Detector/comparator in a phase-bolted loop circuit is to give a mistake signal which is some capacity of the phase blunder between the input signal and the VCO yield signal. Let θd speaks to the phase distinction between the input phase and the VCO phase. Because of this phase contrast the PD creates a relative voltage Vd. The connection between voltage Vd and the phase contrast θd is appeared in Figure 2 The bend is straight and occasional, it rehashes each 2π radians. This periodicity is essential as a phase of zero is indistinct from a phase of 2π.

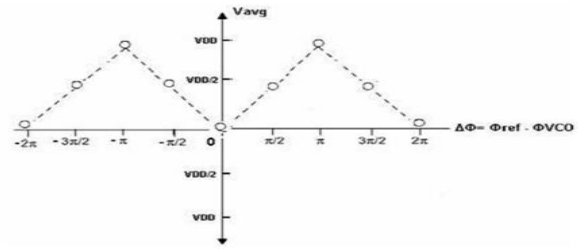

Figure 2 Phase detector characteristics

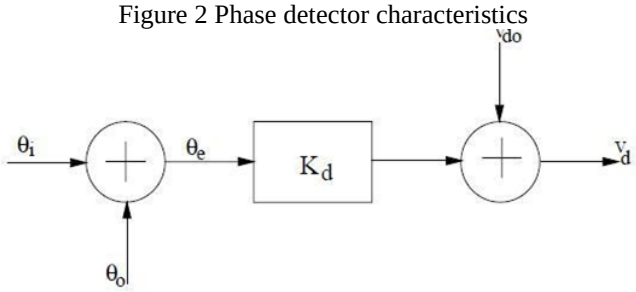

Figure 3 Signal flow Model of Phase detector

The Block diagram of PFD in Figure 4 consist of Modified high frequency D flip flop which has lesser stages as compared to conventional D flip flop so this provides the better switching time and less power dissipation. In this event that the frequency ωA of the input An is not as much as the frequency ωB input B then the PD creates positive heartbeats at the yield QA, while QB stays at zero. Same is valid for the other case, when ωA ≤ ωB positive heartbeats show up at QB and QA stays at zero.

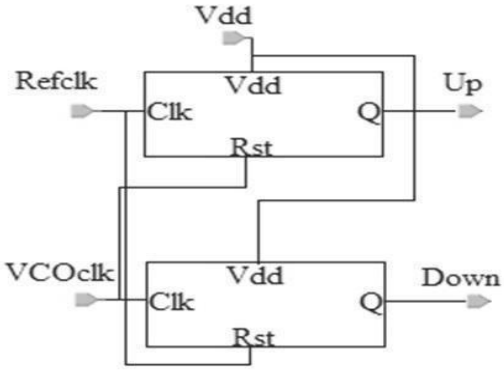

Figure 4 Block diagram of phase frequency detector

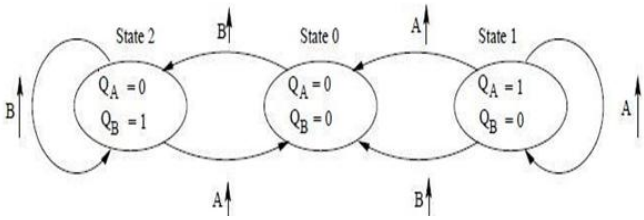

Figure 5 PFD state diagrams

VCO

A VCO is a voltage controlled oscillator, whose yield frequency ωo is directly corresponding to the control voltage VC produced by the Phase finder. This direct connection between the control voltage and the yield frequency improves the PLL plan.

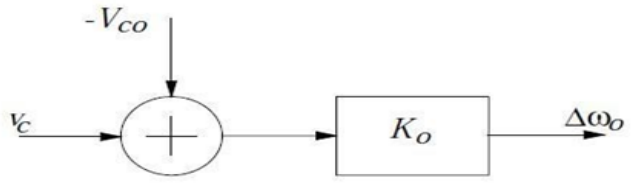

Figure 6 Signal Flow Model of VCO

Loop Filter

The loop filter is the cerebrum of PLL. In the event that the loop channel esteems are not chosen accurately, it might take the loop too long to bolt, or once secured little varieties in the input data may make the loop open. The PFD/CP/LP mix contains a post at the root and VCO likewise contains a shaft at the birthplace. To unwind this issue, a moment capacitor is usually included parallel with R1 and C1as given in Figure 7.

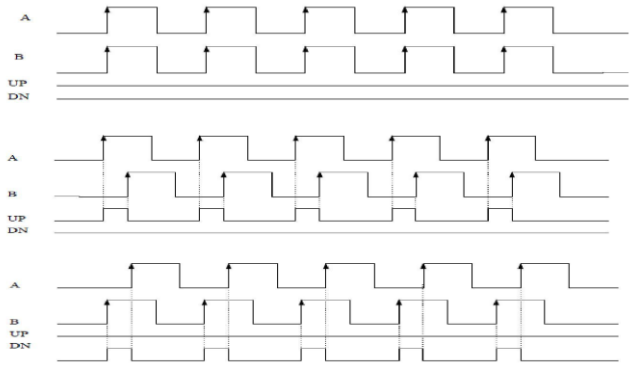

Figure 7 Outputs of PFD with different A and B input

LC Circuit

A LC circuit, likewise called a thunderous circuit, tank circuit, or tuned circuit, comprises of an inductor, spoken to by the letter L, and a capacitor, spoken to by the letter C. LC circuits are utilized either to generate signals at a specific frequency, or choosing a signal at a specific frequency from a more intricate signal. They are enter segments in numerous electronic gadgets, especially radio gear, utilized as a part of circuits, for example, oscillators, channels, tuners and frequency blenders.

Figure 8 demonstrates the ordinary cross-coupled oscillator topology giving negative resistance. It can be either best or tail-one-sided utilizing a current source transistor

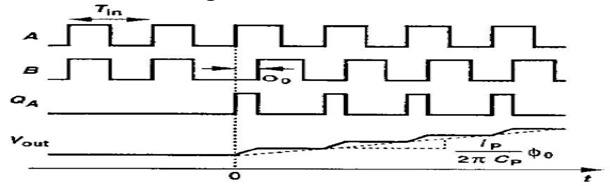

Figure 8 Step response of PFD/CP/LPF

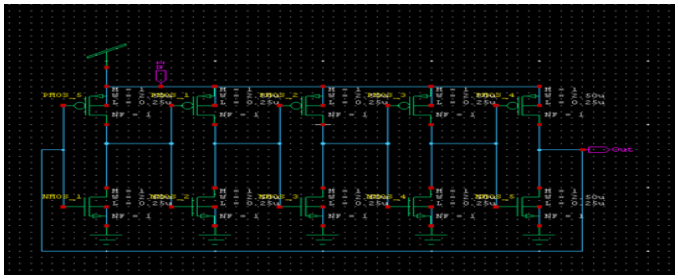

Figure 9 Proposed LC VCO

Table 1 Frequency values for different control voltages

Control Voltage (V)	Frequency (GHz)
0.0	3.8300
0.1	3.8554
0.2	3.8421
0.3	3.8611
0.4	3.8636
0.5	3.8721
0.6	3.9154
0.7	3.9738
0.8	4.0163
0.9	4.0351
1.0	4.0893
1.1	4.0952
1.2	4.2108
1.3	4.2450
1.4	4.2739
1.5	4.2924
1.6	4.3119
1.7	4.3225
1.8	4.3732

Table 2 Parameter values of voltage control oscillators

Parameters	Values	
	Schematic	Postlayout
Oscillation frequency	4.17GHz	3.5GHz
Tuning range	12.2%	8.1 %
Phase noise	-90dbc/Hz	-70dbc/Hz
Technology	180-nm	180-nm
VCO gain	1.74 GHz/v	.166GHz/v
Power dissipation	13 mW	15mW

IV. EVALUATION AND EXPERIMENTAL

Phase noise in phase detector

In simulation result the phase noise remains constant for large frequency span but it shoots up after 2GHz frequency since we know that PFD have jitter and phase noise at high frequency so we will remove this jitter by applying loop filter so that all the high frequency jitter have been reduced.

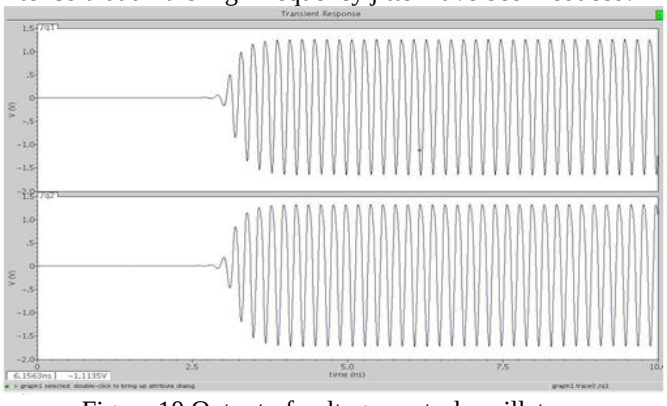

Figure 10 Output of voltage control oscillator

Charging and discharging of loop filter

In case of phase frequency detector, if the ref clk leads the vco clk then the "up" signal becomes high as seen in Figure 11 so this up signal is given to inverter and passed through PMOS to supply V_{DD} to loop filter at alternative instances so the loop filter charges.

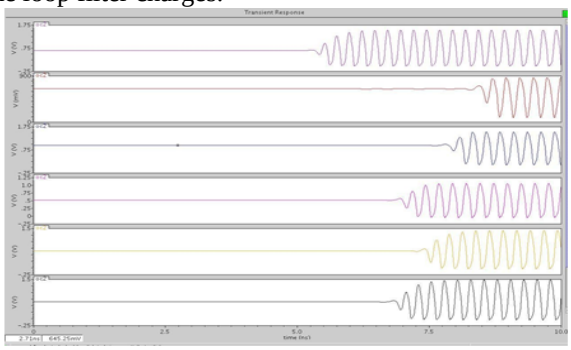

Figure 11 Output of oscillator with different control voltage and frequency

Oscillator results

The oscillations of the voltage control oscillator here the two outputs OC1 and OC2 are complementary to each other and having frequency above 3.1GHz the oscillations are sustained. Figure 12 shows the variation of oscillation frequency with the change in control voltage, ideally the graph should be linear but generally it comes nonlinear here the oscillator free running frequency is 3.87GHz and maximum frequency of oscillation is 4.37GHz.

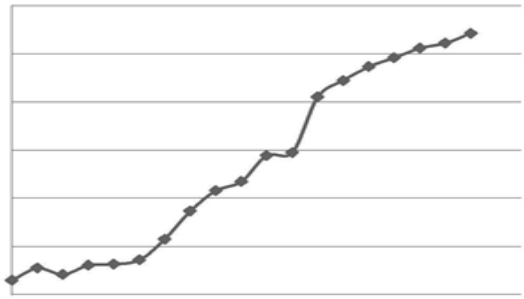

Figure 12 Change in oscillation frequency w.r.t change in control voltage

Results of PLL

The output of XOR PLL which shows that the control voltage variation across loop filter is not constant but it goes like ramp for a period and becomes step for next and this cycle is going on till the locking is not achieved in the circuit, At locking the control voltage becomes steady and the frequency of vco comes in phase with the phase of the ref frequency.

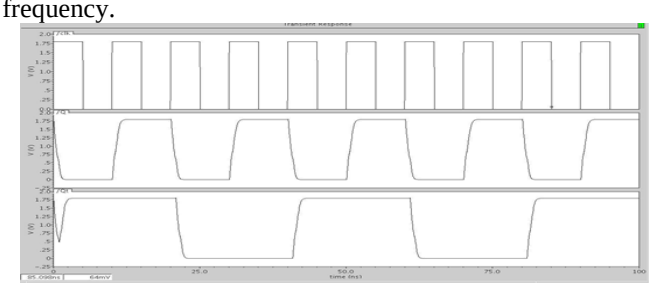

Figure 13 Outputs of divide by two and divide by four counters

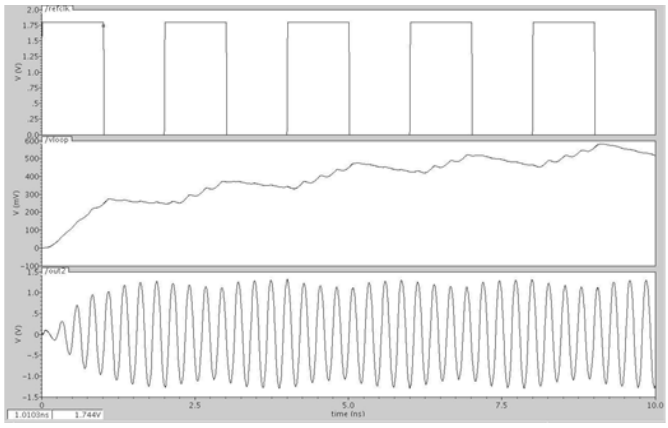

Figure 14 Output of XOR phase locked loop

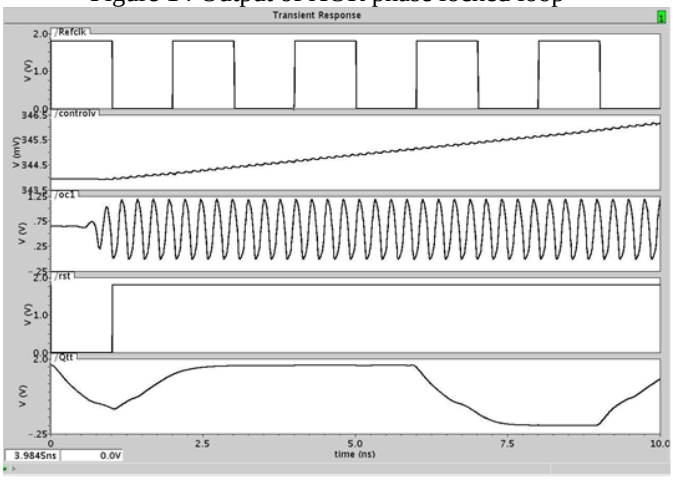

Figure 15 Output of PFD PLL with divide by 2 counter

V. CONCLUSION AND FUTURE WORK

This Phase Locked Loop is composed by utilizing XOR locator and phase frequency finder. Phase bolted loop with PFD is intended for increasing component of 8 and checked. The designs of the considerable number of squares of XOR PLL are drawn, extricated with consummation of the post format recreation and the examination amongst pre and post design has been finished. Another high speed low glitch CMOS PFD is proposed which is made of altered D flip tumble with lesser stages. The LC oscillator is chosen as the voltage control oscillator in the outline of PLL because of better commotion reaction. The phase commotion accomplished in LC VCO is –90 dbc/Hz at 100MHz counterbalance however it ought to be diminished to-100dbc/Hz in order to additionally diminish the clamor segment in VCO.

Future Scope

The subject of phase bolted loop is wide and differing. There are numerous different perspectives that can be joined in the outline to accomplish better performance and all the more powerful. Consider for moment fusing Fault Tolerant Design Techniques to a PLL outline. Since late advances in VLSI technology has made it conceivable to put complex digital circuits on a solitary chip, an ever increasing number of circuits are presently consolidated on a solitary chip to make a system as conservative as could be allowed, for example, a PLL in a handset chip. Because of this ability, it is difficult

to find a blunder in the occasion if the output of a system is not the normal one. The plan methods that make it workable for a system to be operational even under the state of disappointment are named as Fault Tolerant Design Techniques and the system as the Fault Tolerant system. . I might want to execute a Fault Tolerant Frequency Synthesizer, by including both digital plan and VLSI adaptation to non-critical failure systems. The consolidation of this will make it more solid and powerful.

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