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A NOVEL VLSI ARCHITECTURE OF LOW POWER HIGH SPEED FULL ADDER USING GDI MULTIPLEXER

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Abstract: In this paper, we propose a new technique for implementing a low power full adder using a set of GDI multiplexers. Full adder circuits are used comprehensively in Application Specific Integrated Circuits (ASICs). Thus it is desirable to have low power operation for the sub components. The explored method of implementation achieves a low power design for the full adder. Simulated results using state-of-art Tanner tool indicates the superior performance of the proposed technique over conventional CMOS full adder. Detailed comparison of simulated results for the conventional and present method of implementation is presented.

Keywords: Low power full adder, 2-Transistor GDI MUX, ASIC (Application Specific Integrated Circuit), 12-TFA, CMOS (Complementary Metal Oxide Semiconductor).

I. INTRODUCTION

Low power and High speed are the design trade-offs in VLSI industry. Power consumption, area, speed, noise immunity has emerged as a primary design constraints for integrated circuits (ICs). The VLSI designers always targets on three basic design goals such as minimizing the transistor count, minimizing the power consumption and increasing the speed. Most of the Very Large Scale IC (VLSI) applications, Full adder circuit is functional building block and most critical component of complex arithmetic circuits like microprocessors, digital signal processors or any ALUs. Almost every complex computational circuit requires full adder circuitry. The entire computational block power consumption can be reduced by implementing low power techniques on full adder circuitry. In this paper, from different existed base papers several full adder circuits based on different low power techniques have been proposed targeting Static CMOS gates are very power efficient because they dissipate nearly zero power when idle. Earlier, the power consumption of CMOS devices was not the major concern while designing chips. Factors like speed and area dominated the design parameters. As the CMOS technology moved below sub-micron levels the power consumption per unit area of the chip has risen tremendously. In CMOS circuits, the power dissipation classified into dynamic power dissipation, static power dissipation. The dynamic power dissipation occurs when charging or discharging of load capacitances and establish path from vdd to gnd called as short circuit. The static power dissipation occurs by Sub threshold conduction when the transistors are off, Tunneling current through gate oxide and Leakage current through reverse-biased diodesIn which ALU is implemented based on 2:1 MUX, 4:1 MUX, Full adder based on GDI Low power technique GATE DIFFUSION INPUT is a new existing method to reduce power dissipation, propagation delay with less area proposed by Vivechana Dubey and Ravimohan Sairam. The GDI approach allows implementation of a wide range of complex logic functions using only two transistors. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors shown in below.

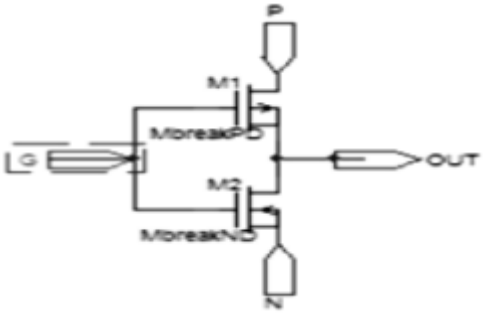

Fig 1: Basic GDI Cell

Table1: Instruction of Basic GDI Cell

S.No.	N I/P	P I/P	G I/P	Output	Function
1.	0	B	A	A'B	F_1
2.	B	1	A	A'+B	F_2
3.	1	B	A	A+B	OR
4.	B	0	A	AB	AND
5.	C	B	A	A'B+AC	MUX
6.	0	1	A	A'	NOT

In which, full adder is designed with2- 4T XOR Gates and 2to 1 MUX .The simulation is carried out MENTORGRAPHICS on 130nm technologies. An important feature of GDI cell is that the source of the PMOS in a GDI cell is not connected to VDD and the source of the NMOS is not connected to GND. Therefore GDI cell gives two extra input pins for use which makes the GDI design more flexible than CMOS design. But it adds noise in output logic levels by effect off delivered leakage power when transistor is off and degrades the performance of the system.

II. LITERATURE SURVEY

While taking account of full adder the sum and carry outputs are represented as the following two combinational Boolean functions of the three input variables A, B and C.

$$Sum = A \oplus B \oplus C \qquad \text{-------eqn.1}$$

$$Carry = AB + AC + BC \qquad \text{-------eqn.2}$$

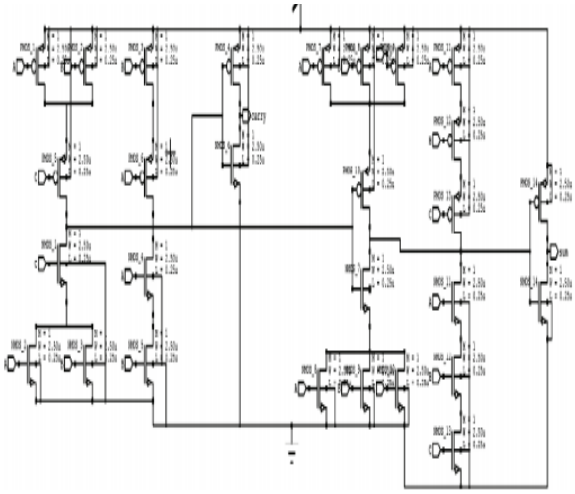

Fig. 2. Conventional 28-T CMOS 1 bit full adder

GDI technique based full adder have advantages over full adder using pass transistor logic or CMOS logic and is categorized by tremendous speed and low power. The technique has been described below.

A. Gate Diffusion Input (GDI)Technique:

The GDI technique offers realization of extensive variety of logic functions using simple two transistor based circuit arrangement. This scheme is appropriate for fast and lowpower circuit design, which reduces number of MOS transistors as compared to CMOS and other existing low power techniques, while the logic level swing and static power dissipation improves. It also allows easy top- down approach by means of small cell library [5]. The basic cell of GDI is shown in Fig. 3.

1) The GDI cell consists of one nMOS and one pMOS. The structure looks like a CMOS inverter. Though in case of GDI both the sources and corresponding substrate terminals of transistors are not connected with supply and it can be randomly biased.

2) It has three input terminals: G (nMOS and pMOS shorted gate input), P (pMOS source input), and N (nMOS source input). The output is taken from D (nMOS and pMOS shorted drain terminal)

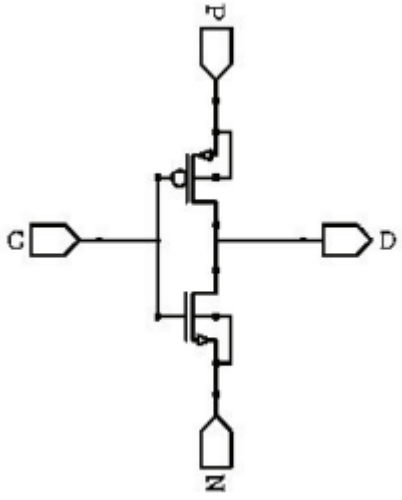

Fig 3 GDI basic cell consisting of pMOS and nMOS.

GDI logic style approach consumes less silicon area compared to other logic styles as it consists of less transistor count. In view of the fact that, the area is less, the value of node capacitances will be less and for this reason GDI gates have faster operation which presents that GDI logic style is a power efficient method of design. We can realize different Boolean functions with GDI basic cell. Table II shows how different Boolean functions can be realized by using different input arrangements of the GDI cell.

TABLE II. GDI CELL BASED VARIOUS LOGIC FUNCTIONS USING DIFFERENT INPUT CONFIGURATIONS AND CORRESPONDING TRANSISTOR COUNTS

N	P	G	OUTPUT	FUNCTION	TRANSISTOR COUNT
0	1	A	A’	Inverter	2
0	B	A	A’B	F1	2
B	1	A	A’+B	F2	2
1	B	A	A+B	OR	2
B	0	A	AB	AND	2
C	B	A	A’B+AC	MUX	2
B’	B	A	A’B+B’A	XOR	4
B	B’	A	AB+A’B’	XNOR	4

III. PROPOSED SYSTEM

GDI FULL ADDER:

The basic architecture of the 2:1 MUX using GDI method is shown in fig. 3. In this configuration we have connected PMOS and NMOS gate along with a SEL line ‘A’, as in MUX. As we know that PMOS works on ACTIVE LOW and NMOS works on ACTIVE HIGH. So, when the SELECT input is low (0) then the PMOS get activated, and show the input ‘B’ in the output and due to low input (0) the NMOS stands idle, as it is activated in high input.

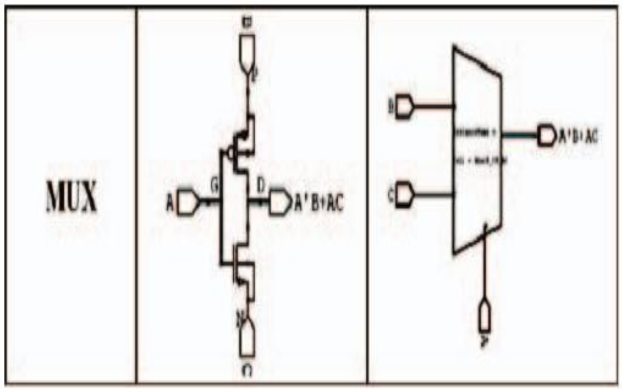

Fig 4. Basic view of 2T MUX using GDI technique

Same for the case, while the G input is high (1) then the NMOS get activated, and show the input ‘C’ at the output. Thus this circuitry behaves as a 2-input MUX using ‘A’ as SEL line, and shows the favorable output as 2:1MUX.

Now we are implementing the low power full adder circuit with the help of 2T MUX, made by GDI technique. It require total 6 numbers of 2T MUX having same characteristics to design a 12T full adder and connected as above in fig.4. The truth table for the above circuit taking each MUX as

consideration are shown table II, and from there it generates 6 various outputs of various MUX.

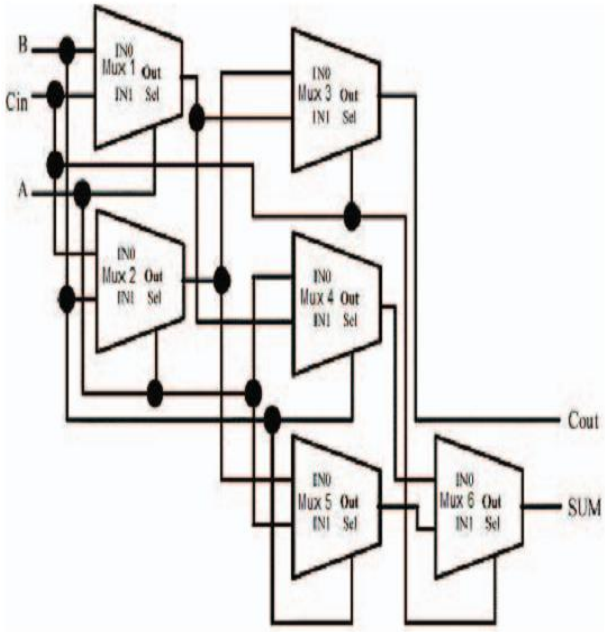

Fig 5: Block Diagram of Low Power Proposed Full Adder using 2T MUX

TABLE III.TRUTH TABLE OF LOW POWER FULL ADDER USING 2T MUX

A	B	Cin	MUX1	MUX2	MUX3	MUX4	MUX5	MUX6	SUM	Cout
0	0	0	0(B)	0(Cin)	0(Cin)	0(A)	0(Cin)	0(A)	0(A)	0(Cin)
0	0	1	0(B)	1(Cin)	0(B)	0(A)	1(Cin)	1(Cin)	1(Cin)	0(B)
0	1	0	1(B)	0(Cin)	0(Cin)	1(B)	0(A)	1(B)	1(B)	0(Cin)
0	1	1	1(B)	1(Cin)	1(B)	1(B)	0(A)	0(A)	0(A)	1(B)
1	0	0	0(Cin)	0(B)	0(B)	1(A)	0(B)	1(A)	1(A)	0(B)
1	0	1	1(Cin)	0(B)	1(Cin)	1(A)	0(B)	0(B)	0(B)	1(Cin)
1	1	0	0(Cin)	1(B)	1(B)	0(Cin)	1(A)	0(Cin)	0(Cin)	1(B)
1	1	1	1(Cin)	1(B)	1(Cin)	1(Cin)	1(A)	1(A)	1(A)	1(Cin)

An arithmetic logic unit (ALU) could be a elementary building block of the Central process Unit (CPU) of a pc, and even the only microprocessors contain one. it's liable for performing arts arithmetic and logic operations like addition, subtraction, increment, and decrement, logical AND, logical OR, logical XOR and logical XNOR. ALU consists of eight 4x1 multiplexers, four 2x1multiplexers and 4 full adders. The 4-bit ALU is intended in 250nm, n-well CMOS technology. once logic '1'andlogic '0' area unit applied as Associate in Nursing input INCREMENT and DECREMENT operations takes place severally. Associate in Nursing INCREMENT operation is analyzed as adding '1' to the number and DECREMENT is seen as a subtraction operation. Two's complement technique is employed for SUBTRACTION within which complement of B is employed.

XNOR TECHNIQUE

XNOR gate is the basic architecture section for full adder circuit. The 3Transistor XNOR module consumes the less power than the XOR module. When A and B input is zero. It gives the output value as '1'.when A=0/1 and B=0/1, it gives the output value as '0'.When A and B input is one, then it gives the output value as '1'.

FULL ADDER BASED XNOR TECHNIQUE

Full adder based XNOR technique has 8T, it consists of two 3T XNOR module generates the SUM output and multiplexer generates the carry output. Full adder is a basic component for an ALU. Depending on the three input A, B, C, the sum and carry output can be generated. Full adder based XNOR technique consumes the power of 86.39pW.

DESIGN OF ALU USING LOW POWER FULL ADDER

An arithmetic and logic unit could be a basic block for several processors. It performs several processors. It performs several operations like addition, subtraction, XOR, XNOR, buffer, NAND, OR, etc. The four bit ALU operation are often enforced exploitation eight 4x1 electronic device, four full adder, four 2x1 electronic device. Depends upon the 3 choice line s2, s1, s0, the arithmetic and operation are often performed.

The block of 4x1 electronic device consists of 4 inputs that is logic zero, logic 1, B and B'. Depends upon the s0 and s1 choice line; the required output are often generated. These outputs.

Table IV: Operations of ALU

S2	S1	S0	OPERATIONS
0	0	0	Buffer
0	0	1	EXOR
0	1	0	EXNOR
0	1	1	OR
1	0	0	ADDITION
1	0	1	SUBTRACTION
1	1	0	BITWISE NAND
1	1	1	Inverter

The next stage of 4x1 electronic device has the input of full adder add, that is EXOR, EXNOR, AND, and OR. Depends on the s0 and s1 choice lines, the output are often generated. It acts as associate input for the 2x1 electronic device. Another input of 2x1 electronic devices is that the full adder add output. Finally, the output stage of 2x1 electronic device are often generated by exploitation s2 choice line.

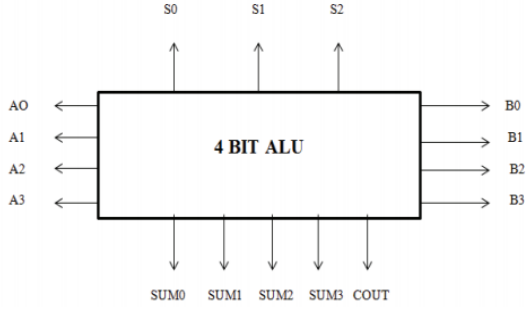

Fig 6: Logo representation of ALU

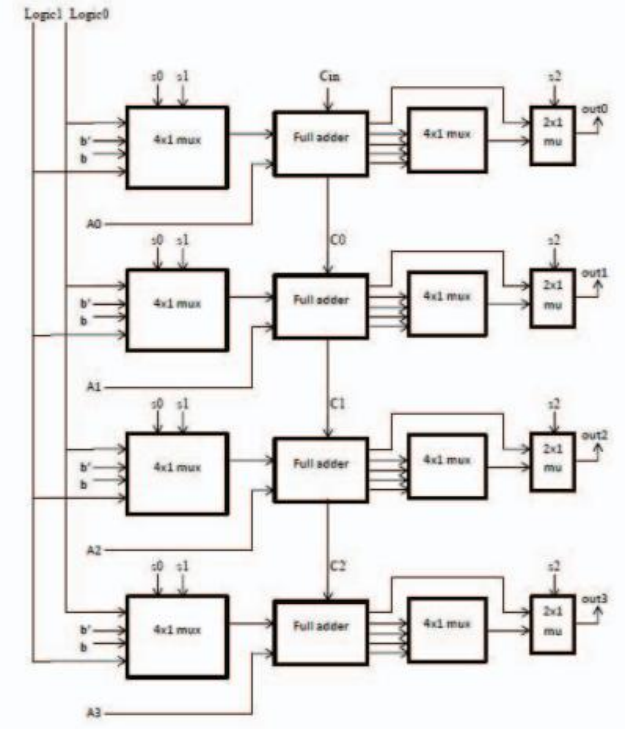

Fig 7: Process of 4bit arithmetic and logic unit.

Multiplexer logic at the input stage consists of 4x1 electronic devices and 2x1 electronic devices. Depends upon the choice line of s0, s1 and s2, the output of full adder has been computed. Electronic device logic at the output stage consists of 4x1 electronic device and 2x1 electronic device. Depends upon the choice line of s0, s1, and s2, the output of ALU has been computed. Input stage electronic device consists of VDD, VSS, B and B'. The output stage electronic device consists of EXOR, EXNOR, AND and OR input. Fig.8 shows input stage of electronic device design and fig9 shows output stage of electronic device design.

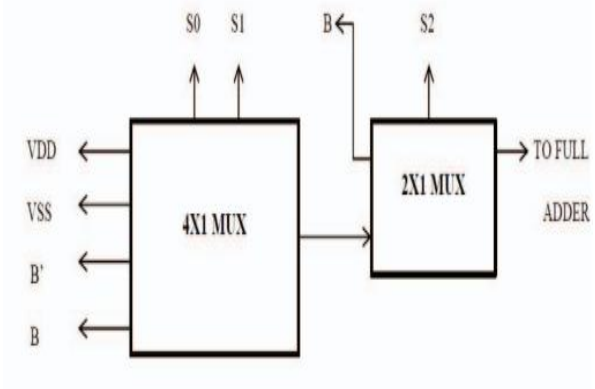

Fig 8: Architecture of multiplexer logic at the input stage

This paper presents a new technique of XNOR logic, to design the full adder is resolved by gate diffusion input technique which proven to have high power consumption and compared with XNOR logic. These new approach of XNOR logic gives excellent result then previous design in charge of power consumption, area as well as propagation delay.

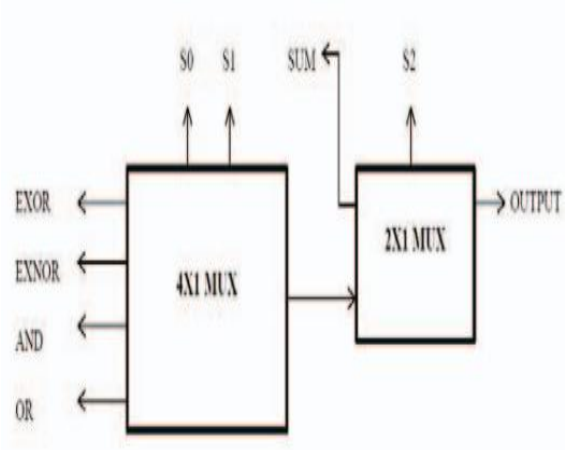

Fig 9: Architecture of multiplexer logic at the output stage

IV. CONCLUSION

Power consumption in CMOS circuit is classified in two categorize: static power dissipation and dynamic power dissipation. In today's CMOS circuits static power dissipation is negligible thus not considered as compared to dynamic power dissipation. Dynamic Power dissipation in a CMOS circuit is given by P = CLf VDD2. The power supply is directly related to dynamic power. The numbers of power supply to ground connections are reduced in GDI implementation which reduces the dynamic power consumption. This work presents a 4-bit ALU designed in MENTORGRAPHICS on 130nm technology for low power and minimum area with GDI technique. The 2x1 multiplexer, 4x1 multiplexer, 1-bit full adder with 10- transistors designed using GDI technique is chosen for lowering power consumption and minimum possible area. Power dissipation, propagation delay and the number of transistors of ALU were compared using CMOS and GDI techniques. GDI technique proved to have best result in terms of performance characteristics among all the design techniques.

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