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# VLSI DESIGN AND IMPLEMENTATION OF MULTI-BIT FLIP FLOP FOR DIGITAL CIRCUITS

Singara Vijayalakshmi[1], P.Bindu Madhavi[2]
[1]PG Scholar, [2]Assistant Professor,
Dept of ECE, Sri Sai Institute of Technology And Science, Rayachoty, Kadapa, Andhra Pradesh.

***Abstract: Power has become a burning issue in modern VLSI design. In modern integrated circuits, the power consumed by clocking gradually takes a dominant part. Given a design, we can reduce its power consumption by replacing some flip-flops with fewer multi-bit flip-flops. However, this procedure may affect the performance of the original circuit. Hence, the flip-flop replacement without timing and placement capacity constraints violation becomes a quite complex problem. To deal with the difficulty efficiently, we have proposed several techniques. First, we perform a co-ordinate transformation to identify those flipflops that can be merged and their legal regions. Besides, we show how to build a combination table to enumerate possible combinations of flip-flops provided by a library. Finally, we use a hierarchical way to merge flip-flops. Besides power reduction, the objective of minimizing the total wire length is also considered. The time complexity of our algorithm is©(n1.12) less than the empirical complexity of© (n2). According to the experimental results, our algorithm significantly reduces clock power by 20–30% and the running time is very short. In the largest test case, which contains 1 700 000 flip-flops, our algorithm only takes about 5 min to replace flip-flops and the power reduction can achieve 21%.***

***Index Terms: Clock power reduction, merging, multi-bit flip-flop, replacement, wirelength.***

## I. INTRODUCTION

Optimizations in VLSI have been done on three factors: Area, Power and Timing (Speed).Area optimization means reducing the space of logic which occupy on the die. This is done in both front-end and back-end of design. In front-end design, proper description of simplified Boolean expression and removing unused states will lead to minimize the gate/transistor utilization. Partition, Floor planning, Placement, and routing are perform in back-end of the design which is done by CAD tool .The CAD tool have a specific algorithm for each process to produce an area efficient design similar to Power optimization. Power optimization is to reduce the power dissipation of the design which suffers by operating voltage, operating frequency, and switching activity. The first two factors are merely specified in design constraints but switching activity is a parameter which varies dynamically, based on the way which designs the logic and input vectors. Timing optimization refers to meeting the user constraints in efficient manner without any violation otherwise, improving performance of the design. High performance designs are achieved by proper placement, routing and sizing the element. The word optimization is approached in different ways by merging, instead of sizing the memory element. Some of the basic ideas of timing optimization approach are (a) Circuit re- synthesis.

## II. RELATED WORK

The idea of designing the multi-bit flip-flop arises for power considerations and placement rout-ability effectiveness. Some of them are discussed here: Minimization of dynamic clock power leads the way to merge the single-bit flipflops and constructed Multi-Bit Flip-Flops. This merging process also has to satisfy the certain area constraint which decreases the total flip-flop area in synchronous design the clock power by congested constraints of unallocated bins and the length of constraints of the input and output signals of all the 1-bit flip-flop. Here redundant inverters in merging of single-bit flip-flop are eliminated. The multi-bit flip-flops are mostly viewed as low power design technique, MBFFs with larger bit numbers as possible to gain more clock power saving but larger bit number may lead to severe crosstalk's due to close interconnecting wires .To address this problem step by step procedure those are creating crosstalk model of MBFF, next coupling Capacitance Generation from these derive Flip-Flop and Intersection Graph are considered. A clustering and Placement is done by reducing the interconnect wire length. Merging of Flip-Flop is done through library that perform a coordinate transformation to identify those flip-flops that can be merged and their legal regions. This approach reduces the wire length considerably.
The Digital design uses the single-bit Flip Flop for memory applications and controller design. D flip flops are implemented in two ways which are Master-Slave latch pair and pulse-triggered latches. Most of the design involving standard cell follows Master-Slave approach because of the restricted timing constraints of pulse triggered latches. In master-slave approach, two latches are connected in serial manner with complementary clock signal in serial manner with complementary clock signal.

## III. PROPOSED SYSTEM

This proposed method is based on paper which gives the idea of merging clock pulse.
The working of single-bit D flip flop is similar to the D latch except that the output of D Flip Flop takes the state of the D input at the moment of a positive edge at the clock pin (or negative edge if the clock input is active low) and delays it by one clock cycle. That's why, it is commonly known as delay flips flop. The D Flip-Flop can be interpreted as a delay line or zero order hold. The advantage of the D flip-flop over the D-type "transparent latch" is that the signal on

  

the D input pin is captured the moment the flip-flop is clocked, and subsequent changes on the D input will be ignored until the next clock event.

From the timing diagram in fig 1 it is clear that the output Q changes only at the positive edge . At each positive edge the output Q becomes equal to the input D at that instant and this value of Q is held until the next positive edge.

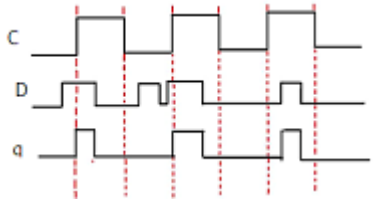


Fig 1: Timing diagram for SBFF.

Multi-bit Flip Flop which takes multiple data input and results in multiple data output. The working of multi-bit flip flop is same as single-bit flip flop, whenever the clock gets active state flip flop latches all input to output. For inactive state the flip flop holds the data. The basic structure of multi-bit flip flop is given in fig 2 and its corresponding waveform is given in fig 3.

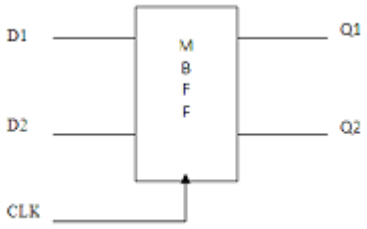


Fig 2: MBFF

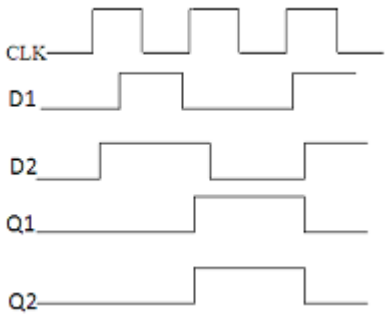


Fig 3: Timing for MBFF

This paper experimented the proposed technique by designing the Serial-In Serial-Out using SBFF and MBFF separately. Designing of SISO has two reasons:- SISO is basic sequential device and easy to analyze. Another one is pipelining, SISO of n-bit register is nothing n-stage pipeline worked for many application such as Serial Bit Communication [7]. We analyze both existing and proposed design using basic sequential circuit of SISO. For existing system, Serial in serial out circuits are constructed by SBFF and MBFF which shown in fig 4 and fig 5. The operation described as arrival of a clock pulse, data at the D input of each flip-flop is transferred to its Q output. At the star, the contents of the register can be set to zero by means of the CLEAR line. If a 1 is to the input of the first flip flop. Then upon the arrival of the fist clock pulse, this 1 is transferred to the output of flip-flop 1. After four clock pulses this 1will be at the output of flip-flop 4. In this manner, a four bit number can be Stored in the register. After four more clock pulses, this data will be shifted out of the register.

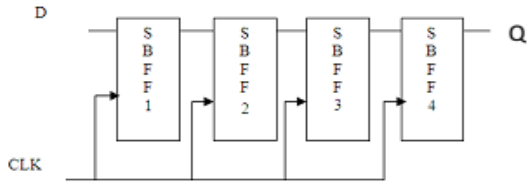


Fig 4: SISO using SBFF

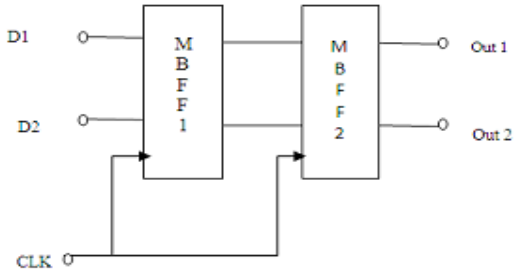


Fig 5: SISO using MBFF

Simulation results:

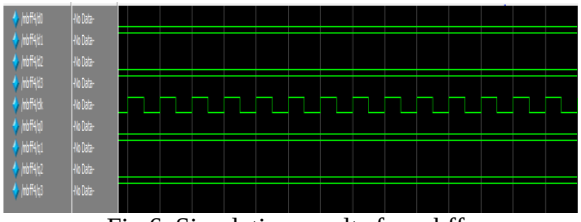

Fig 6. Simulation results for mbff.

## IV. CONCLUSION

In present VLSI design area is one of the important issues to be addressed. To achieve reduced area various types of flip flops and shift register are discussed. Single bit flip flop and Multi bit flip flop are implemented to achieve less usage of area. Various size of shift register is implemented with Multi bit flip flop. This proposed method is implemented in Xilinx Virtex 5 FPGA family. Experimental results are targeted to number of flip flop usage, delay and clock buffer. Flip flop area usage is minimized approximately to 50%. Thus this proposed method is more suitable for reduction of hardware.

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