REVIEW OF NCL BASED DESIGN

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Abstract: As SoCs get bigger and performance is more demanding, the normal synchronous implementation gives designers severe problems related to clock domain and Synchronizing them, the current spikes generated by fast switching and contact drop inside the chip are all complex. Null Convention Logic (NCLTM) technology, developed by Theseus Logic, may help to eliminate problems related clock tree and also significantly reduce power consumption, noise and Electromagnetic Interference (EMI).In this paper, we present comprehensive introduction on NCL design approach for fundamentals.

Keywords - Asynchronous design, Null Convention Logic (NCL) , Quasi –delay Insensitive(QDI)

I. INTRODUCTION

Currently, most digital circuits have been designed by a synchronous design methodology. However, fully-synchronous digital systems have the weakness of high power consumption because clock distribution over whole synchronous circuits is a large source of power consumption. Especially, the conventional synchronous design circuits cannot satisfy the timing requirement of the low voltage digital systems, but also can generate wrong outputs under the influence of scaling issues in nanometer region such as severe process variations, short channel effects, aging effects, and etc.

Therefore, in the reliable ultra-low power design, asynchronous circuits have recently been re-considered as a solution for the scaling issues, and Null Convention Logic (NCL) is one of the promising delay-insensitive asynchronous circuit design methodologies. It has many advantages of inherent robustness, power consumption, and easy design reuses.

II. ASYNCHRONOUS DESIGN APPROACH

A. Bounded Delay

The models such as micro pipelines assume that delay of all wires and gates are bounded. Each gate and wire will be assigned a range of delay values and it is assumed that for all operations, the delay will fall in this range. Therefore, bounded delay models are usually implemented through a bundled-data encoding scheme (Fig.1), which control data flow by localized worst-case timing constraints (matched delays). The req signal must be delayed long enough until all data signals are valid and stable, then the ack signal will be sent back when all data values are latched. In general, bounded-delay models utilize a synchronous style and provide good coding efficiency but require extensive worst-case timing analysis.

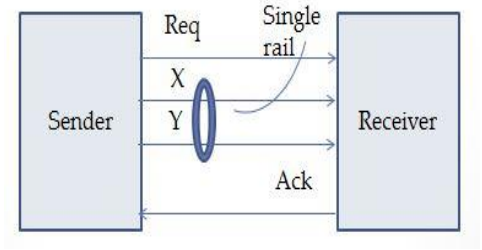

Fig 1 Bundled-data encoding

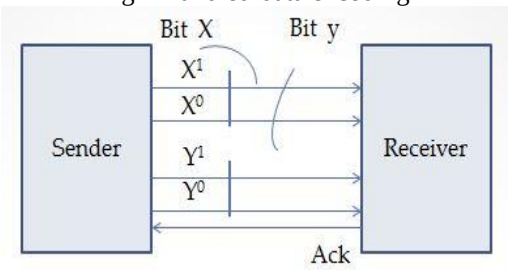

Fig 2 Dual-rail encoding

B. QDI (Quasi Delay Insensitive)

Quasi-delay-insensitive (QDI) circuits allow arbitrary gate and wire delays but impose an isochronic fork assumption to avoid unwanted hazards and glitches. This assumption is that within basic components, such as full adders, timing skews caused by wire delays are much less than gate delays and thus delays to all endpoints of each forking wires are almost identical. Typically, the isochronic fork assumption is attained at the gate-level design of basic components, where engineers can manipulate delays. It is important to note that, at a component connection level, wire delays do not need to comply with this assumption, since arrival of input data can be controlled by completion detection circuits. Therefore, QDI circuits need very little timing analysis and can achieve average performance instead of worst-case performance as Bounded-delay models. In implementation, QDI circuits typically use multiple-rail encoding scheme to transfer data. Fig.2 is an illustration of dual-rail encoding scheme, which uses two wires for each binary signal. The data itself indicates whether it is valid or not, hence the req wire is removed.

C. NCL (NULL Convention Logic)

NULL CONVENTIONAL LOGIC is a new technique developed for designing asynchronous circuits. NULL mean there is NODATA or spacer between corresponding DATA. It indicates no input or output is present. NCL is theoretically complete and economically viable approach to delay insensitive circuits. NCL is not purely based on DI circuit method but on a class of DI called as quasi delay insensitive (QDI). QDI is designed using Isochronic Forks. The delay in the fan-out is assumed to be same. NCL uses 2 criteria to

achieve delay insensitive behavior 1] Symbolic completeness& 2] Completeness of inputs NCL logic design is implemented using threshold gates with hysteresis. These gates have many inputs and one output. Output from this gate is DATA when numbers of inputs reach or exceed the threshold. The hysteresis behavior is achieved by keeping the output is same state as previous till all the input goes to NO DATA.

III. NCL BACKGROUND

A. DUAL RAIL/LOGIC RAIL

NCL is a delay-insensitive (DI) asynchronous (i.e., clock less) paradigm, which means that NCL circuits will operate correctly regardless of when circuit inputs become available; therefore, NCL circuits are said to be correct-by-construction (i.e., no timing analysis is necessary for correct operation). NCL circuits utilize dual-rail or quad rail logic to achieve delay-insensitivity. A dual-rail signal, D, consists of two wires or rails, D0 and D1, which may assume any value from the set DATA0, DATA1, NULL, as depicted in Table 1. The DATA0 state corresponds to a Boolean logic 0, theDATA1 state corresponds to a Boolean logic 1, and the NULL state corresponds to the empty set (meaning that the value of D is not yet available).

	DATA0	DATA1	NULL	Illegal
D0	1	0	0	1
D1	0	1	0	1

Table 1 Dual-Rail signals

B. NCL as threshold gate

NCL is implemented using discrete threshold gates. NCL design consists of predefined 27 gates. This gate determines DATA of the output when the threshold numbers of wires are present with data at the input. A general THmn gate described in Fig. 3(a) will have n inputs and threshold level is m with the meaning that the output will only become asserted when at least m inputs are asserted, and de-asserted when all inputs are de-asserted; otherwise, it will keep its previous state(Fig. 4).

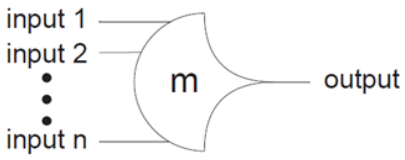

Fig 3.a THmn Threshold Gate

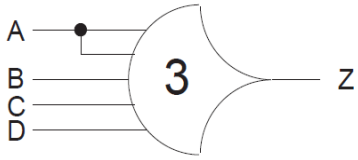

Fig 3.b TH34w2 Threshold Gate

Another type of threshold gate is referred to as a weighted threshold gate, denoted as THmnWw1w2.wR (Fig 4). Weighted threshold gates have an integer value, m ≥wR> 1, applied to inputR. Here 1 ≤ R < n; where n is the number of inputs; m is the gates threshold; and w1, w2, .wR, are the integer weights of input1, input2,... inputR, respectively. For example, consider a TH34W2 gate, whose n = 4 inputs are labeled A, B, C, and D. The weight of w is 2.

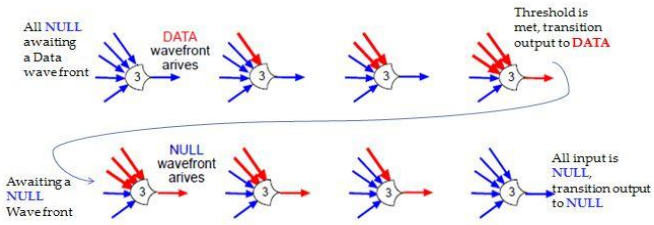

Fig 4 Hysteresis behavior of NULL Convention Logic gate

B. NCL Register

The framework of NCL circuits (Fig. 5) is very similar to conventional synchronous circuits in which registers are used to control dataflow between combinational logic blocks. With this similarity, circuit designers can follow the same fundamental steps to design an NCL system.Therefore, NCL usually is the best choice with lowest switching cost when changing from synchronous flows to an asynchronous framework.

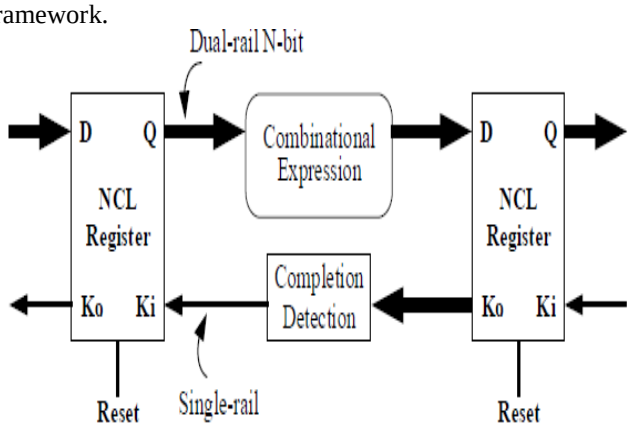

Fig 5 NCL system framework

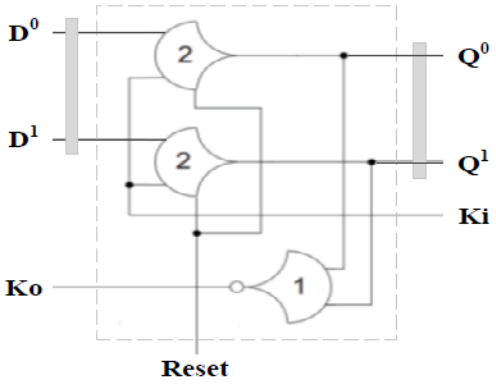

Fig 6 Single-bit dual-rail register

An NCL register operates as a “dual-state latch” with Ki as an enable signal. It becomes transparent when Ki and input D are both DATA or both NULL and becomes opaque otherwise. To explain, when Ki is NULL (or DATA), D will flow through to Q if D is also NULL (or DATA); in contrast, output Q will remain as previous if D is not in the same DATA/ NULL state with Ki. The implementation of an NCL 1-bit register is depicted in Fig. 6.

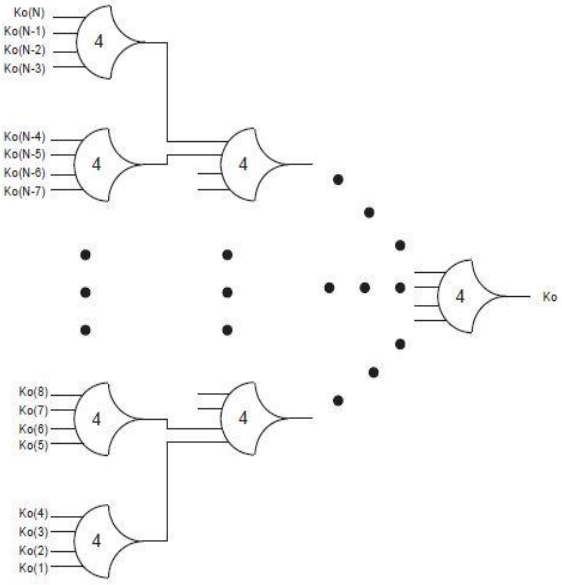

Fig 7 N- Bit completion detection

NCL Gate Boolean Function	NCL Gate Boolean Function
TH12	A + B
TH22	AB
TH13	A + B + C
TH23	AB + AC + BC
TH33	ABC
TH23w2	A + BC
TH33w2	AB + AC
TH14	A + B + C + D
TH24	AB + AC + AD + BC + BD + CD
TH34	ABC + ABD + ACD + BCD
TH44	ABCD
TH24w2	A + BC + BD + CD
TH34w2	AB + AC + AD + BCD
TH44w2	ABC + ABD + ACD
TH34w3	A + BCD
TH44w3	AB + AC + AD
TH24w22	A + B + CD
TH34w22	AB + AC + AD + BC + BD
TH44w22	AB + ACD + BCD
TH54w22	ABC + ABD

Table 2The Fundamental NCL gates

Ko, on the other hand, is used to detect completeness of the output but indicates in inverse domain. For 1-bit register, when Q is a valid DATA, Ko will be NULL and vice versa. For multi-bit registers, completion detection (Fig. 7) is needed. When all bits of Q are valid DATA, it is said to be 'complete DATA', and at that time, Ko will be NULL. In contrast, Ko will be DATA when Q is 'complete NULL'. A completion detection is simply a 'hysteresis' AND function, which is a THnn gate in NCL. Although the maximum number of inputs in a fundamental NCL gate is only 4, the completion detection circuit of an output with more than 4 bits can be implemented as a combination of TH44 gates (Fig. 7). In an NCL sequential circuit, Ko of a register is connected to Ki of the previous one and behaves as an acknowledge and request signal. When the output Q of a register is already 'complete DATA', its Ko transitions to NULL and thus, drives Ki of the previous register to NULL to wait for a NULL wavefront. Similarly, when the output Q of a register is already reset to 'complete NULL', its Ko will drive Ki of the previous register to DATA to wait for a DATA wavefront. Therefore,instead of aligning with a clock edge as in conventional synchronous systems, in NCL, two DATA wavefronts will always be separated by a NULL wavefront to avoid data overwriting.

IV. NCL ADVANTAGES IN SPECIFIC APPLICATIONS

Smartcards

These contain personal and card specific custom data in memory which are needed for access purposes. With a smartcard designed in synchronous technology, it is possible to guess at the stored data by "listening" to current consumption and EMI. As transmission protocol and interaction activities are known, it is possible to assign a meaning to the different extracted patterns. This is a very complex task but possible. Using NCL changes the picture: the different parts of the chip work independently and speed changes with voltage and temperature. Listening results look like random noise and emit less EMI, leading to increased protection against deciphering of the chip data.

Smartcard example

Infineon owns an NCL license and has implemented the DES algorithm with 64 bit data block length using a 56 bit key. The code consists of 5000 lines VHDL that were synthesized using the NCL shell. The chip has been manufactured in a 0.13m CMOS process and is currently under evaluation.

Low current consumption systems

NCL technology improves performance in all areas. Direct improvement is less current consumption in the digital circuits compared to existing designs. Less current peaks produce indirect benefits of better performance in all four analogue functions on-chip (microphone amplifier, A/D, D/A and output amplifier).

Increased performance for ICs with fast analogue and digital functions

NCL generates on-chip random noise rather than synchronous current peaks that degrade the specifications of analogue on chip parts. The implementation of digital functionality in NCL will always reduce noise. The example of a microprocessor shows values 11dB lower noise compared to a synchronous implementation.

Better sensitivity for wireless ICs

Less noise generated by the on-chip logic will improve the specifications of amplifiers, mixers and VCOs. One example would be in Bluetooth technology for wireless transmission to microphone and earpiece. Less current consumption reduces battery weight on the ear and less noise eases design of the analog blocks. Interpolating D/A converters these products are used in high volume in mobile phone base

stations. The main blocks are digital FIR filters containing multipliers. Even though the data is transmittedsynchronously, NCL design leads to reducednoise levels in the DAC block that is fed with the digital results.

V. CONCLUSION

In this late-Moore era, the conventional synchronous design is suffering from some problems such as clock skew and power consumption in the deep submicron region. This caused a continuous growth of interest in asynchronous paradigm recently, especially with Null Convention Logic (NCL) subset. This paper has provided a comprehensive introduction to theNCL design approach, from fundamentals to recent advances. On other hand NCL design increase chip area so there is one trade off.

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