PERFORMANCE ANALYSIS OF LOW POWER ALU USING NOVEL FULL ADDER AND PASS TRANSISTOR LOGIC BASED MULTIPLEXER

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Abstract: An optimized compensation strategy for two-stage CMOS OTA has been proposed for a high frequency OPAMP design. Here, the slew rate and bandwidth has been increased by employing thin and long transistors into the design at output stage and wide transistors in input stage. These two techniques are able to increase the gain up to a great extent by increasing the output resistance and input transconductance respectively. There is a slight increase in static power dissipation of proposed architecture, but, the overall advantage of increased slew rate and gain bandwidth product which is very important parameter of communication so it compensates for this limitation.

I. INTRODUCTION

The operational transconductance amplifier (OTA) is an amplifier whose differential input voltage produces an output current. Thus, it is a voltage controlled current source (VCCS). There is usually an additional input for a current to control the amplifier’s transconductance. The principle differences from standard op-amp are-

- Its output of a current contrasts to that of standard operational amplifier whose output is a voltage.
- It is usually used "open-loop"; without negative feedback in linear applications. This is possible because the magnitude of the resistance attached to its output controls its output voltage. Therefore a resistance can be chosen that keeps the output from going into saturation, even with high differential input voltages.

The schematic symbol of an Operational Transconductance Amplifier (OTA) is shown in Figure 1.1

The OTA converts an input voltage to an output current relative to a transconductance gain parameter Gm=io/vi. Ideally the input and output resistances are infinite (Ri=Ro=∞) such that ii=0 and the output current is absorbed solely by the load. The conventional OTA is classified as a Class A amplifier and is capable of generating maximum output currents equal to the bias current applied. The equivalent circuit model indicates the transconductance amplifier generates an output current (io) proportional to an input voltage (vi) based on the transconductance gain Gm. The open circuit voltage gain of the conventional OTA model IN Figure 1.1 (B) is given by A=GmRo.

II. LOCAL COMMON MODE FEEDBACK

Industry is researching techniques to reduce power requirements, while increasing speed, to meet the demands of low (battery) powered wireless systems. These systems require amplifiers with low bias currents, capable of producing large dynamic currents. Application of Local Common Mode Feedback (LCMFB) techniques to the conventional OTA architecture produces an efficient class AB amplifier with enhanced gain-bandwidth and slew rate.

Characterization Parameters

Several common characterization methods are used to classify the functionality of OTA structures. These performance measurement techniques will be used to analyze designed structures via theoretical calculation, simulation, and experimentation throughout the documentation presented in the following chapters. A list of the measured characteristics is provided below:

1. Open Loop Gain (AOL)
2. Gain Bandwidth (GB)
3. Maximum Output Current (IOUTMAX)
4. Slew Rate (SR)
5. Static Power Dissipation (PSTATIC)

III. DESIGN AND IMPLEMENTATION OF PROPOSED OTA

3.1 Single Ended Proposed OTA

The conventional OTA (Figure 3.1(a)) uses a differential pair in conjunction with three current mirrors to convert an input voltage into an output current. A Differential Amplifier has been implemented using Microwind 3.0 with its simulation result shown in Figure 6.1.
An approach to show that current mirror circuit is more beneficial than conventional Diode load has been implemented using Microwind 3.0. The simulation of this circuit has been shown in next chapter in Figure 6.2.

The schematic layout of Conventional Operational Transconductance Amplifier (Figure 3.1(a)) in S-Edit Tanner EDA Tool and LTSPICE IV is shown in Figure 5.3 below.

For quiescent (or common mode) operation, the drain currents of transistors M1-M10 have equal values \( I_{D1-10} = I_{S} \) while the current \( i_r \) in transistors MR1, MR2 is zero. The gate-source voltage of M3, 4 is the same as their drain-source voltage. For common mode signals, these transistors perform as low impedance (diode connected loads) with value:

\[
R_{CM} = \frac{1}{g_{m3,4}}
\]

Upon application of a differential signal, the signal current component \( i_d = i_r \) flows through transistors MR1, 2, and \( i_{D1,2} \) are given by:

\[
i_{D1,2} = I_D + i_r = \frac{I_{Bias}}{2} + i_r
\]

and, \( v_d \) is the applied differential voltage. The drain currents in M3, 4 remains unchanged \( i_{D3,4} = I_{Bias/2} \). The current \( i_r \) generates differential complementary voltage changes at nodes A and B while node C remains at a constant voltage. Signal voltages at nodes A and B are given by:

\[
V_A = -V_B = \frac{v_d}{2} \left( 1 - \frac{v_d/2}{V_{GS1,2}-V_{TH1,2}} \right) \left( \frac{v_d/2}{V_{GS1,2}-V_{TH1,2}} \right)
\]

Where \( V_{R} \) is the resistance generated by transistors MR1, MR2 and, based on the triode channel resistance equation, is given by:

\[
R_{MR1,2} = \frac{1}{\beta_{MR1,2}(V_C-V_{THP}-V_R)}
\]

Where \( V_R \) is the applied control voltage (Figure 5.1 (b)), \( \beta_{MR1,2} = kP \left( W_{MR1,2}/L_{MR1,2} \right) \), and \( V_C \) is the constant voltage at node C. This complementary swing at A, B generates large, non-complimentary, signal current in the shell (M5-10) of the OTA by creating large gate-source voltage differentials for common source transistors M5, M6, respectively. The schematic layout of Proposed OTA architecture in S-Edit Tanner EDA tool and LTSPICE IV has been shown below: 5.2 Design Parameters of Proposed OTA

The gain bandwidth of the conventional OTA is defined as:

\[
GB = \frac{(Kgm_{1,2})}{2C_{L}}
\]

Rearranging equation (5.24), with unity mirror gain (K=1), the following equation can be used to calculate the
transconductance gain of the input differential pair.

\[ 2\pi C_L \cdot GB = gm_{1, 2} \]

5.7

The transconductance of a MOS transistor can be calculated with the following expression:

\[ gm = \frac{2KPW_L}{L} \]

5.8

Using this expression, the width of the NMOS differential input pair (M1, 2) can be determined based on a fixed bias current and predetermined length by rearranging Equation (5.26) for the following relation:

\[ W_{1, 2} = \left(\frac{gm_{1, 2}}{2} L_{1, 2}\right) / (2KP) \]

5.9

Utilizing a drain current of \( I_D = I_{BAS} / 2 = 250\mu A \) (for \( V_{DS, SAT} = 0.25V \)), a length \( L_1 = 3\lambda \) \((L_1 > L_{MIN} = 2\lambda \) for improved matching) and recognizing \( KP = 3KP_F \), Equations (5.25) and (5.27) can be used to size all transistors for the conventional OTA. Designed transistor sizes and corresponding \( V_{DS, SAT} \) voltages, based on theoretical calculations are listed below in Table 5.1.

<table>
<thead>
<tr>
<th>TRANSISTORS</th>
<th>DIMENSIONS (W/L)</th>
<th>( V_{DS, SAT} ) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1=M2</td>
<td>4.12/0.18 µm</td>
<td>0.25</td>
</tr>
<tr>
<td>M3</td>
<td>1.91/0.18 µm</td>
<td>0.28</td>
</tr>
<tr>
<td>M4</td>
<td>7.21/0.18 µm</td>
<td>0.28</td>
</tr>
<tr>
<td>M5</td>
<td>7.70/0.18 µm</td>
<td>0.28</td>
</tr>
<tr>
<td>M6=M7=M8</td>
<td>5.18/0.18 µm</td>
<td>0.23</td>
</tr>
<tr>
<td>M9=M10, (( L_{MIN} ))</td>
<td>1.098/0.18 µm</td>
<td>0.24</td>
</tr>
</tbody>
</table>

Cascoding output transistors (M9, M10) do not require matching design and were designed with minimum length for speed. Their widths were reduced by a factor 2 to reduce area.

The SE-LCMFB OTA is designed for comparison with the conventional structure. For an equivalent comparison, the SE-LCMFB structure is designed with core transistor sizes identical to those of the conventional OTA listed in Table 5.1. The core of the SE-LCMFB structure is therefore identical to the conventional structure and the only design required is the sizing of triode resistance transistors MR1, MR2.

The resistance formed by MR1, 2 (MR1, 2) can be used to trade slew rate and gain bandwidth enhancement with phase margin for the class AB SE-LCMFB OTA. The high frequency pole at nodes A/B, maximum output current, and open loop gain are all functions of \( R_{MR1, 2} \). \( R_{MR1, 2} \) is programmable, is determined by the control voltage \( V_R \), and is given by:

\[ R_{MR1, 2} = \frac{1}{\beta_{MR1, 2} \cdot (V_C - V_R - V_{THP})} \]

5.10

Where, \( V_R \) is the control voltage applied at the gate of MR1, 2, \( V_C \) is the constant voltage at node C, and \( \beta_{MR1, 2} = KP(W_{MR1, 2}/L_{MR1, 2}) \). For design of MR1, 2, a range of \( A_{MR1, 2} \) can be determined based on a desired range of phase margin \( \Delta P M \). Simplifying for the position of the high frequency pole (phase margin) as a function of the resistance \( R_{MR} \) (assuming \( r_{ds1} \approx r_{ds2} \approx r_{ds3} \approx r_{ds4} \) the following expression is obtained:

\[ f_{PA, B} = \frac{1}{2\pi R_{MR1, 2} C_{GS1, 2}} \]

5.11

This relationship indicates a decrease in \( f_{PA, B} \) and consequently, a decrease in phase margin, as \( R_{MR1, 2} \) increases. A decrease in \( R_{MR1, 2} \) would then lead to an increase in \( f_{PA, B} \) and an increase in the phase margin. The design method for sizing MR1, 2 involves replacing transistors MR1, 2 with resistors R1, 2 as shown in Figure 5.5.

Table 5.2 SE-LCMFB MR1, 2 Design Transistor Sizes

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MINIMUM VALUE</th>
<th>MAXIMUM VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase Margin</td>
<td>40°</td>
<td>90°</td>
</tr>
<tr>
<td>( R_{MR1, 2} )</td>
<td>200</td>
<td>1000</td>
</tr>
<tr>
<td>( V_R )</td>
<td>-1.75</td>
<td>-0.75</td>
</tr>
<tr>
<td>Transistors</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( W_{MR1, 2}(\mu m)/L_{MR1, 2}(\mu m) )</td>
<td>1.4/0.18 µm</td>
<td>2.67/0.18 µm</td>
</tr>
<tr>
<td>MB1</td>
<td>1.098/0.18 µm</td>
<td></td>
</tr>
<tr>
<td>MB2</td>
<td>2.67/0.18 µm</td>
<td></td>
</tr>
</tbody>
</table>

Table 5.3 Analysis Table

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>WORK(results)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slew Rate</td>
<td>910</td>
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<tr>
<td>Bandwidth</td>
<td>2.4</td>
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<tr>
<td>Maximum O/P Current</td>
<td>0.5</td>
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Simulation Results

<table>
<thead>
<tr>
<th>(mA)</th>
<th>4.95</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Power</td>
<td></td>
</tr>
<tr>
<td>Dissipation (mW)</td>
<td>88.3</td>
</tr>
<tr>
<td>Phase Margin (Degree)</td>
<td>38.3</td>
</tr>
</tbody>
</table>

FUTURE WORK
The single ended Local Common Mode Feedback Network CMOS Operational Transconductance Amplifier serves as prototype, and, hence, can be reconfigured to many OTA architectures to be used in smart cards, credit cards, etc. for random number generations. This single ended LCMFB CMOS OTA can be further enhanced to a fully differential LCMFB Operational Transconductance Amplifier for improved performance in gain and phase margin as well.

REFERENCES
[9] Tsung-Hsien Lin, Member, IEEE, Chin-Kung Wu, and Ming-Chung Tsai, “A 0.8-V 0.25-mW Current-Mirror OTA With 160-MHz GBW in 0.18μm CMOS”, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 54, NO. 2, FEBRUARY 2007
Publications


