International Journal For Technological Research In Engineering
Volume 5, Issue 8, April-2018 *ISSN (Online): 2347 - 4718*

OPTIMIZATION 8-BIT ALU USING HYBRID LUT/MUX FPGA DESIGN USING VERILOG HDL

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Abstract: In this project, we are going to Optimization 8-Bit ALU using Hybrid LUT/MUX FPGA Design using Verilog HDL, and recent Verification. This Project proposes synthesize RTL design for Look UP Table (LUT's), Multiplexer (MUX) separately, and Hybrid LUT/MUX architecture of combined RTL and LUT. In Verification methodology, separate result for LUT and MUX and then combined result of both LUT and MUX compared. This Proposed design using Xilinx Tool will give Optimized result of LUT, MUX and Hybrid LUT/MUX design, and this design verification and simulation in Questasim Tool. The purpose of this design is to optimize power, delay and area for better performance. In my research work my design verification for using the difference on way and find the coverage area and 100 % coverage report generated in my Optimization 8-Bit ALU using Hybrid LUT/MUX FPGA Design.

Keywords: LUT, MUX and Hybrid Design, Compare Result's

I. INTRODUCTION

HYBRID configurable logic blockarchitectures for field-programmable gate arrays that contain a mixture of lookup tables and hardened multiplexers are evaluated toward the goalof higher logic density and area reduction. [1], presents a hybrid design of configurable logic block (CLB) composed of look-up tables (LUTs) and universal logic gates (ULGs). An ULG is designed to realize holistic efficiency compared with the corresponding LUT. Previous designs with ULGs are either based on pure ULG or LUTULG complementary architecture, which incur longer delay or double the area compared to LUT based design. [2], Generous flexibility of Look-Up Tables (LUTs) in implementing arbitrary functions comes with significant performance and area overheads compared with their Application Specific Integrated Circuit (ASIC) equivalent. [3] A LUT/MUX and Hybrid method for using the check and find the difference between these three-type methods to what change are created in CLB.And CLBthe relationship between the MUX, LUT and the Hybrid to configure, compared to the definition of the path, field and power, which is fully derived. These methods are then using these three types of design to use this relation to reduce the area of CLB and the choice can be configured to use three methods to test the user. In this paper how to design of three methods to ALU in Hybrid LUT/MUX and how-to optimization od 8-bit ALU. LUT therefore works like a type of memory. Before handin the same memory the data of the logical operation is done in the storage by the configurator, and the robbery acts as a mux, there is select and input. LUT can be selected by making minimal 3-in-dip input. MUX is a type of controller. It works like a switch, selects the input and gives the signal in the output, and the selection pin is calculated by the input in the mux, as there are 2 inputs, there is a select pin for it. Which sends the output point signal by multiplying the input into a signal, in which the output signal transmits one after the other. And tool development in this area are still advancing, spurred on by the following advantages that asynchronous design offers. Hybrid design is a Communication of LUT and MUX, which is used to reduce the size and path of connecting MUX with LUT, can also lead to change in CLB, and I tested CLB in my research work. I'll also see what makes a difference between the result and the result. See the Figure below for what looks like in hybrid design. CLB is a configurable logic block, and changes in the CLB can be changed according to user's configuration code. Which includes static memory and logical gate and MUX and is connected to the outer side of the border with an In-Out pin, with which the switch boxes are also attached, which is between the CLB and the job of managing the power supply doing. Hybrid CLB architectures that contain a mixture of MUX LEs and the traditional LUTs yielding up to 6% area,power and reduce path delay savings.

II. RELATED WORK

The objective is to minimize the area of circuits that have to be implemented into an FPGA,and i want to design CLB in a new way for which i have used the XILINX tool, I will do my RTL code synthesize with the help of the Xilinx tool and change it to Manuel, in the LUT, MUX and Hybrid Design Structures Prepare them. And have used the mentor graphic tool for simulation.

III. PROPOSED ARCHITECTURE

For the work of my research I evaluated a number of FPGA architectural papers and a new change can be made.

For example, I have designed the section III(a) 4: 1 in the LUT of the Mux, and on its basis, I have designed the same 4: 1 MUX from MUX, which showed its Figures in section III (b), And then I combined Hybrid Design with LUT and MUX's Communication, which is shown in section III (c).

a. LUT: 4-to-1 Multiplexer Design

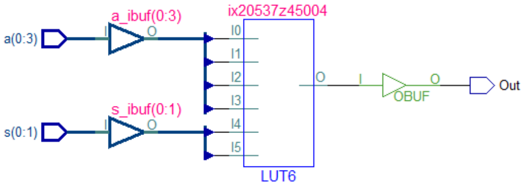

Figure 1 Using LUT to design 4:1 MUX

To design this LUT from 4: 1 mux, Xilinx on XST tool has a few menu changes in which I have selected LUT to generate this RTL view, which was difficult to make the first change as it was very difficult but a few papers and After the searching work, I found a solution.

b. LUT: 4-to-1 Multiplexer Design

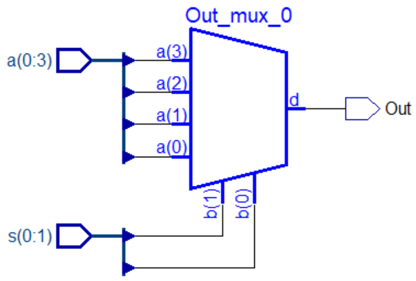

Figure 2 Using MUX to design 4:1 MUX

What I did not do for this design from MUX, as shown above, I made this design an RTL view after the XST tool changes. In the same way as in the LUT and the input and select line has been taken. And I made it into MUX constantly provide a powerful clock that reaches all parts of

c. Hybrid: 4-to-1 Multiplexer Design

For the hybrid design i made LUT and MUX communicating and converted it into the RTL view of Hybrid and for that I did the next process and in which I selected the option of MUX and LUT to change its view, as shown below, which you can see.

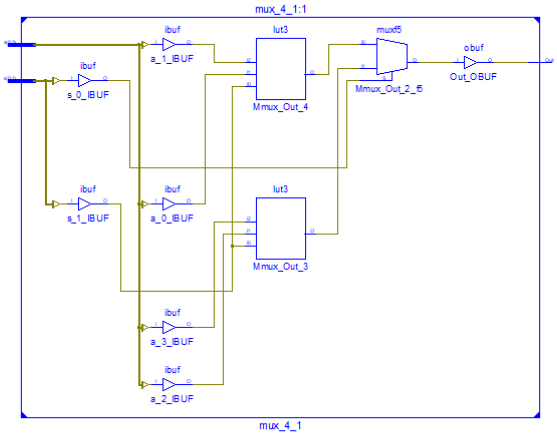

Figure 3 Using LUT and MUX Hybrid to Design 4:1 MUX

FOR ARCHITECTURE OF ALU IN HYBRID LUT/MUX

As shown above, I have designed the ALU for my research work. In which LUT MUX and Hybrid have used these three different matrices, and one of the three methods has got a good result in which the table has been produced, and in which method, trying to delay less area, power and path.

IV. PROPOSED METHOD

In my work, I thought of making a few changes in the inside part of the FPGA, in which I used LUT MUX and Hybrid with the static memory in CLB and different used logic gate and MUX, which is my future work, which I used to do with FPGA What you want to put in such a way that you will see in the following Figure.

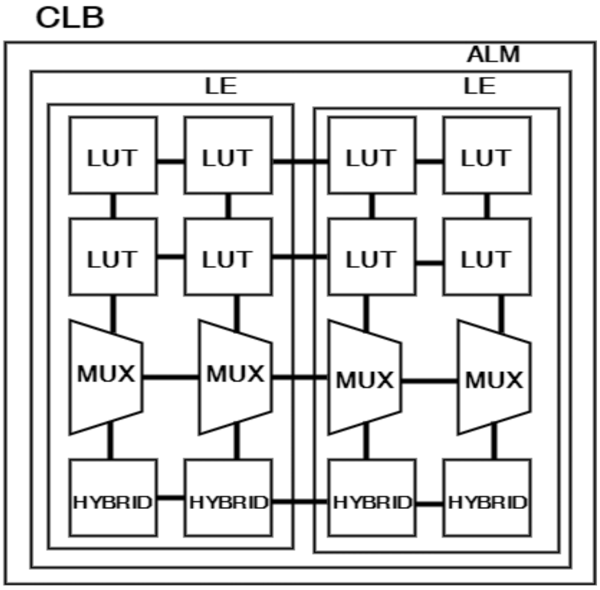

Figure 4 In FPGA CLB Architecture

In which all the used LUT MUX and Hybrid are paired with each other and it is paired with an In Out pin in the CLB, the programmer who uses this FPGA will get an option and the way the output is needed, CLB can debug in.

Challenges in Design

I had to make many changes in Xilinx tool in the design of LUT, because in my design I had the need of a Lift created by LUT for which I have Manuel LUT place and route setting function which was the core work of my research, Complicated problem came.

The 8-bit designed ALU in it I did have three RTL view events of ALU and to test how many LUTs are used in its place and route in RTL View. I have discovered the difference between the one who made Manual setting. Now I have also designed MUX and Hybrid like that which I have written shortly and have also shown its diagram.

Like the change in LUT, the change in MUX design has also changed, which is all in the figure shown next.

In this way hybrid LUT and MUX are designed and there are many changes in the program and Xilinx tool automatic place and routing space. I also reduced the path and shape of the path with the help of the Manuel setting.

I have completed 94% of my goals as per my research work, and now I have thought of its backend side design, but for me it is enoughLike the change in LUT, the change in MUX design has also changed, which is all in the figure shown next.

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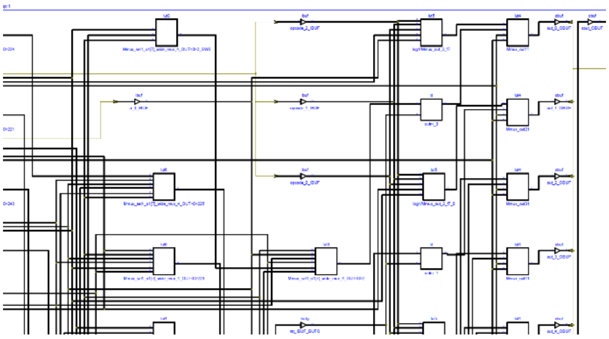

Figure 5 8-bit ALU LUT RTL View

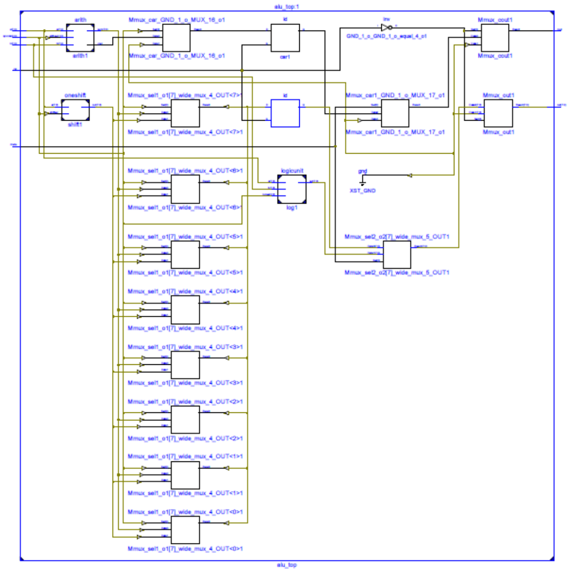

Figure 6 8-bit ALU MUX RTL View

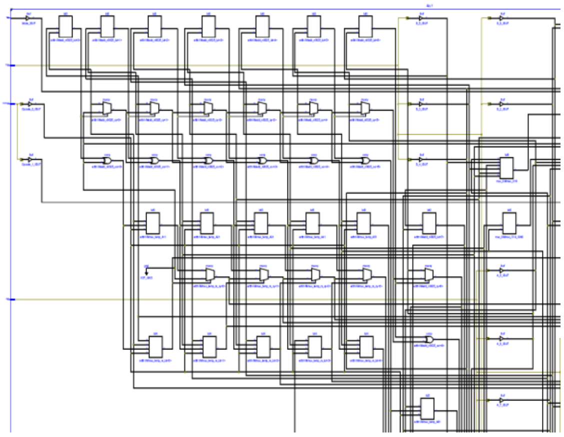

Figure 7 8-bit ALU Hybrid RTL View

Verification

Verification of synchronous designs requires the checking of the static timing constraintimposed by the clock and of the logical functionality of each module. For anasynchronous design, verification is difficult due to the non-deterministic behavior of arbiter elements, and deadlock is not easy to detect without exhaustive state spaceexploration. Formal techniques for asynchronous circuit design may assist inthis area.

V. SIMULATION RESULTS AND ALU OUTPUT RESULT's

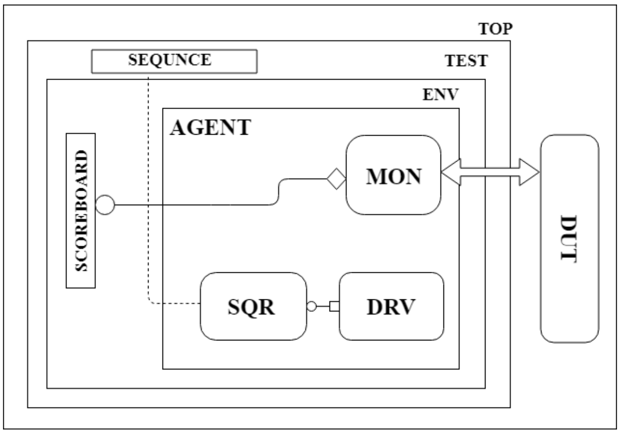

Figure 8 UVM Verification Block Diagram

This is my model for verification, which I am using for my 8-bit ALU Design LUT MUX and Hybrid LUT/MUX. I am using UVM verification. Which is called Advanced Verification Methodology.

In Unicorns, a single angle is used, and it is digitized in the driver monitor and sequencer, and it is connected with the scoreboard pointer in the Connection Environment using an Analysis Port.

Result of my certification as shown below 6 also includes a simulation race.

SIMULATION RESULT's

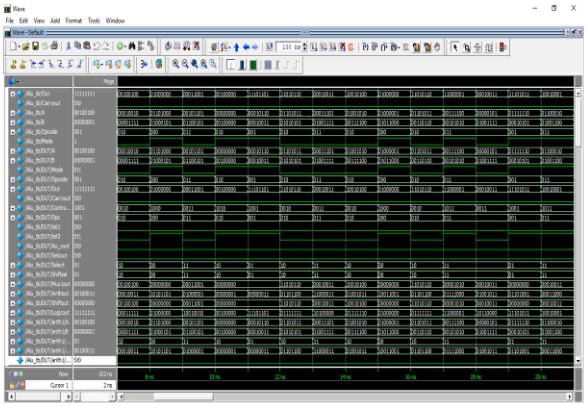

Figure 9 RTL Design Simulation View

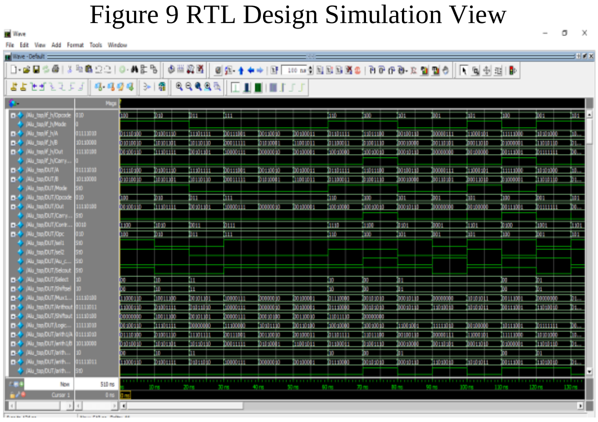

Figure 10 UVM Verification Simulation View

Table of Delay

Item No.	LUT	MUX	Hybrid
Delay Path	7.093ns	7.846ns	4.986ns

Table1 DELAY RESULT's

VI. CONCLUSION

We have proposed a new type LUT MUX and Hybrid CLB architecture containing MUX and LUT hard elements shown in figure no. 4.Optimization LUT MUX and Hybrid LUT/MUX And my work in more than optimized totally delay path LUT inis7.093ns, MUX in is 7.846ns and HYBRID in is 4.986ns.And UVM verification in totally coverage report cover in 100%, Using UVM advance verification methodology. But, I am not design in backend side because not available of backend design tool but completed design codding in using Xilinx Synthesize Tool and Questa sim for verification and simulation result's, and I am find and optimization Delay, area and Power using synthesize RTL design, it's my Goal and I archive this goal in my research work which is best in LUT MUX and Hybrid designing into.

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