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# HARMONICS AND STRESS REDUCTION BY A 5 LEVEL DC BOOST CONVERTER USED FOR THE EXCITATION SYSTEM

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***ABSTRACT:*** ***This paper presents new boost type power factor corrector rectifiers that operates in continuous-conduction mode (CCM) and generates a multilevel voltage waveform at the input. Due to CCM operation, commonly used ac-side capacitive filter and dc-side inductive filter are removed from the proposed modified packed U-cell rectifier structure. The proposed transformer less, diminished channel, and multilevel rectifier topology has been explored tentatively to approve the great dynamic execution in producing and directing double 125-V dc yields terminals as media transmission board's feeders or mechanical battery chargers under different circumstance incorporating change in the heaps and change in the fundamental matrix voltage adequacy. High power factor or PFC support converter is utilized as a part of model which works in help mode. IGBT is utilized for exchanging task and Model takes a shot at 50 Hz recurrence it utilizes Less no. of framework switches which lessens the framework stretch and Less number of switches decreases misfortune in influence and furthermore makes circuit straightforward and less expensive.***

***Keywords: boost convertor, less switches IGBT, continuous-conduction mode (CCM)***

## I. INTRODUCTION

Ac–dc conversion of electric power is widely used in several applications such as adjustable-speed drives (ASDs), switch-mode power supplies (SMPSs), uninterrupted power supplies (UPSs), and battery energy storage. Conventionally, ac–dc converters, also known as rectifiers, are developed using diodes and thyristors to provide uncontrolled and controlled dc power with unidirectional and bidirectional power flow. Major drawbacks include poor power quality in terms of injected current harmonics; resulting voltage distortion, poor power factor at input ac mains, and slow varying rippled dc output at load end; low efficiency and large size of ac and dc filters.Reduction of harmonic content with the consequent increase of power factor (PF) can be obtained by using either passive or active power factor correction (PFC) techniques. Passive methods include the use of tuned LC filters, what represents a robust solution. However, increased size, weight, and volume result. Besides, the passive filter may not respond adequately if the load power factor comes to vary. On the other hand, active methods come as a more efficient solution by using controlled solid-state switches in association with passive elements such as resistors, inductors, and capacitors. In fact, the closed-loop operation of the static power converter dedicated to PFC assures satisfactory performance with high input PF and regulated dc output voltage over a wide operating range. Increased complexity and reduced robustness are distinct characteristics of this practice though. In order to meet the requirements in the proposed standards such as IEC 61000-3-2 and IEEE Std 519 on the quality of the input current that can be drawn by low-power equipment, a PFC circuit is typically added as a front end stage. The boost PFC circuit operating in continuous conduction mode (CCM) is by far the popular choice for medium and high power (400 W to a few kilowatts) application. This is because the continuous nature of the boost converter's input current results in low conducted electromagnetic interference (EMI) compared to other active PFC topologies such as buck–boost and buck converters. With the application of multilevel topology in DC-DC converter, main disadvantage is found due to increasing of level need large number of switches. These switches produce loss in power with the application. Also with the using large number of switches makes circuit more complex and expensive. Additionally the complex circuits need complex control circuit. Not only the number of gate drive circuits is high, but since it is necessary to ensure that the DC levels in all the capacitors are balanced, their coordination is a complex task that must be performed by a powerful high performance (and therefore expensive) processor. Overall these characteristics (complex power circuitry, high number of gate drivers and high computational load) combine to drive both system complexity and cost to very high levels, making the multilevel inverter a solution that could be applied only in very high power applications such as marine motor drives, massive chemical industry drives and high power transmission systems where the overall capital invested was so high that the power converter cost was not the main consideration.

## II. ANALYSIS OF THE MODEL

Conventional AC-DC Boost Converter

The single-stage diode rectifier related with the lift converter, as appeared in Figure 2.1, is generally utilized in dynamic PFC. On a fundamental level, the mix of the diode connect rectifier and a dc-dc converter with sifting and vitality stockpiling components can be stretched out to different topologies, for example, buck, buck-lift, and Cúk.

The lift topology is extremely straightforward and permits low-misshaped input streams, with nearly solidarity control factor utilizing distinctive devoted control procedures. Common procedures are hysteresis control, normal current mode control and pinnacle current control [4]. All the more as of late, on-cycle control [5] and poise [6] have additionally been utilized.

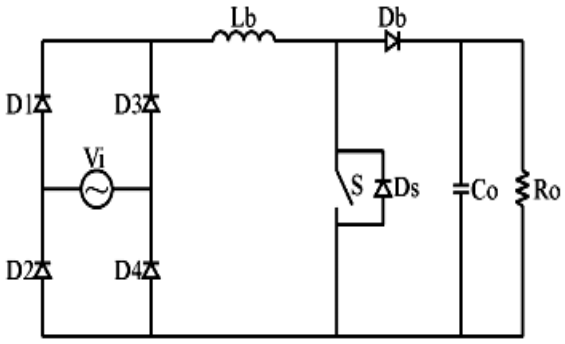



Figure 1:Conventional AC-DC Boost Converter

## III. SYSTEM MODELING

Reduces switching is more necessary for decreasing the stress in the system. Here we design the new approach for the PFC boost convert which uses one stage methodology for conversion of the voltage. Figure 4.1 shows the proposed model of the system.

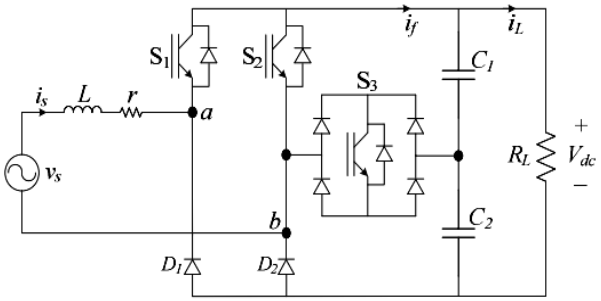



Figure 2: Proposed Model of PFC boost Converter

The proposed five-level boost PFC rectifier in which three active switches and six diodes have been used as a slight modification to a similar topology that includes four switches requiring more gate drives and consequently more space on the manufactured board.

It is clear from the figure 4.1 a bidirectional switch has been connected between leg b and midpoint of DC capacitors to provide different paths for current in order to produce five voltage levels at the output including $\pm V_{dc}$, $\pm V_{dc}/2$ and 0 where $V_{dc}$ is the output DC voltage generated by the rectifier. The bidirectional switch is made by four diodes and one active switch instead of using two active switches to shrink the 0scheme adopted for producing five level PFC boost configuration.

Table 1: Switching Pattern of the five level PFC boost configuration

| Switching State | $I_s$ | $S_1$ | $S_2$ | $S_3$ | $V_{dc}$ |
|---|---|---|---|---|---|
| 1 | >0 | 1 | 0 | 0 | $V_{dc}$ |
| 2 | >0 | 1 | 0 | 1 | $-V_{dc}/2$ |
| 3 | $\geq 0$ & $\leq 0$ | 1 | 1 | 0 | 0 |
| 4 | < 0 | 0 | 0 | 1 | $-V_{dc}/2$ |
| 5 | < 0 | 0 | 1 | 0 | $-V_{dc}$ |

From the switching table it can be said that based on current direction, different voltage levels would be produced by firing necessary switches. If the current is positive, turning ON the switch S1 leads to conducting the diode $D_2$ so $+V_{dc}$ will be appeared at $V_{ab}$ and both capacitors ($C_1$& $C_2$) are charged up.

In next switching state, by firing switches $S_1$ and $S_3$ simultaneously, a low impedance current path would be provided through $C_1$ and bidirectional switch $S_3$ so the upper capacitor would be charged and $V_{ab}$ will have the voltage level of $+V_{dc}/2$. The zero level would be generated by a short circuit between points a and b using switches S1 and $S_2$. For negative current direction, $D_1$ is mostly responsible to prepare required current path. Hence, by turning ON the $S_3$, the current will pass through only the lower capacitor $C_2$ and charges it up while $D_1$ is conducting and the negative voltage level $-V_{dc}/2$ would be generated at the rectifier input. Finally, during negative current direction, if switch $S_2$ is fired, then diode $D_1$ conducts and $V_{ab}$ would be equal to $-V_{dc}$. Having no redundancy switching states is the most important problem of this topology which makes the dc capacitors voltages balancing difficult.

Due to five level output it produce low harmonics in then grid hence it required small size of filter compared to the conventional two-stage rectifier. So reduce size of passive element produce it light weighted and hence manufacturing cost of the converter is low.

## IV. ANALYSIS OF THE RESULTS

For showing the dynamic behavior of the proposed work is implemented in the MATLAB software. Here for simulation use simpower system toolbox. The simulation mode is use variable step discrete with simulation time of 50µs.

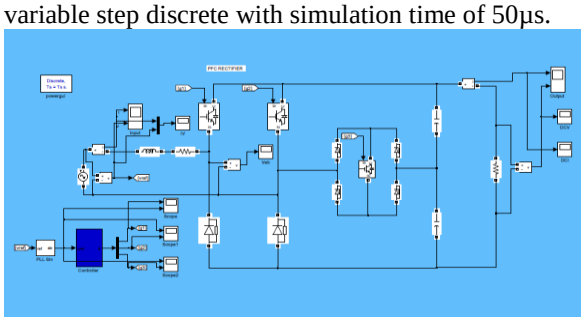


Figure 3: Proposed Boost Converter for Power Factor Improvement

Table 2 : Parameter used in proposed work

| System Parameter | |
|---|---|
| AC Supply Voltage Peak Value | 120 V |
| AC frequency | 50Hz |
| Inductor size | 2.5mH |
| DC Voltage | 220 V |
| DC Capacitor ($C_1$& $C_2$) | 47000µF |
| DC Load ($R_L$) | 100Ω |
| Switching Frequency | 5kHz |

Figure shows the Simulink model of proposed work. Table 2 shows the parameter used in the simulation.This section

deals the result obtained from the simulation of proposed work. The following results are obtained with the simulation of the 5 level PFC boost converter which is proposed in previous chapter.

Test results from the boost convertor model

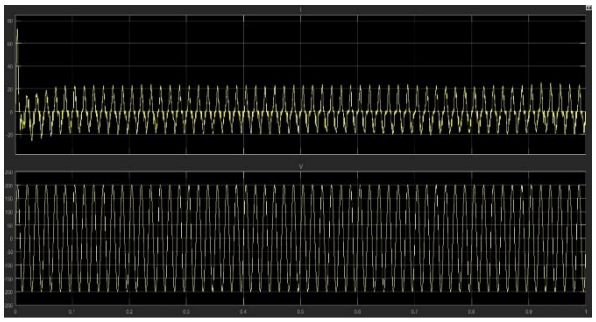
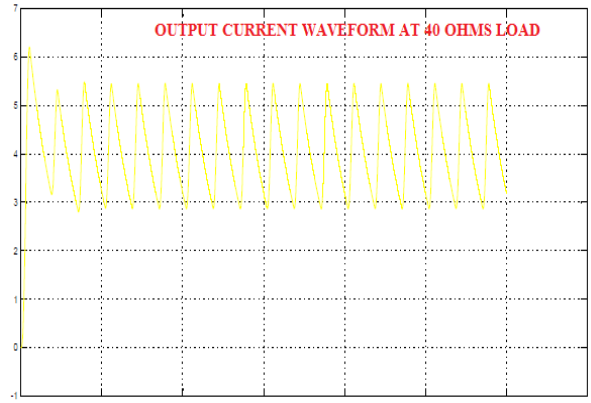


Fig. 6.5 Input supply from grid for load 40 ohms



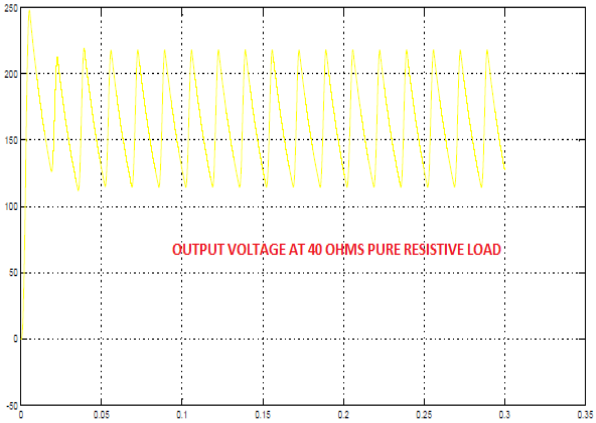




Fig. 6.6 Output from boost convertor for load at 40ohms

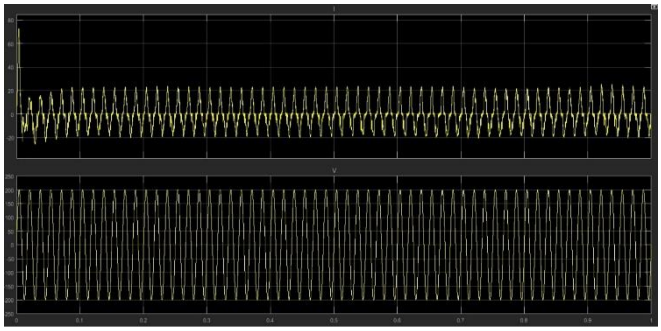
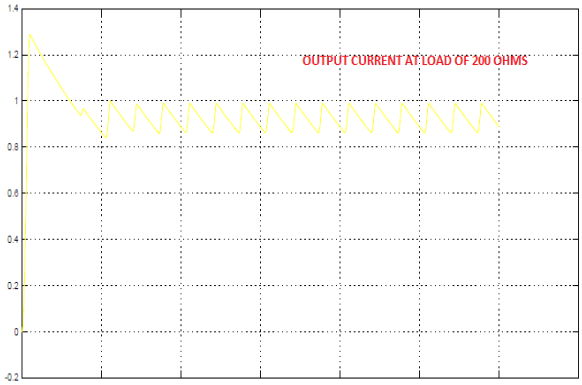


Fig. 6.7 Input supply from grid for load at 200 ohms



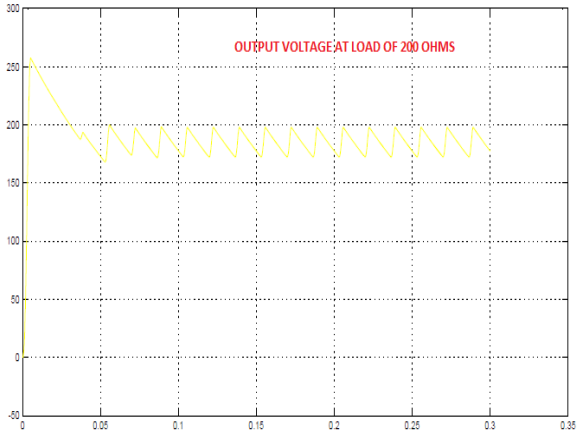




Fig. 6.8 Output from boost convertor for load at 200 ohms

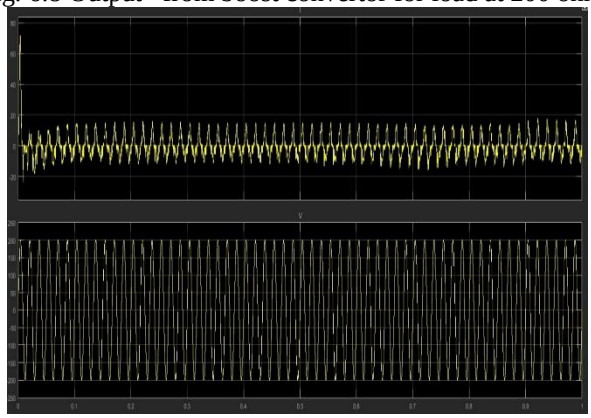
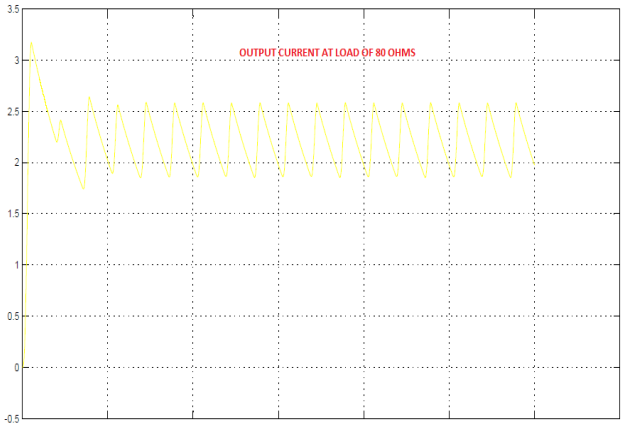


Fig. 6.9 Input supply from grid for load 80 ohms



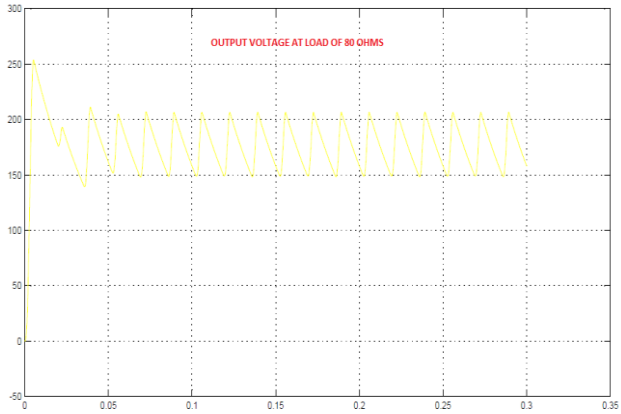



Fig. 6.10 Output from boost convertor for load at 80 ohms

Test results from base paper

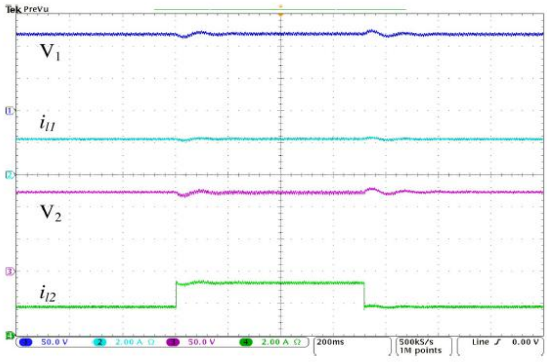



Fig. 11. Test results during 50% decrease in load$_2$ from 80 to 40 Ω.

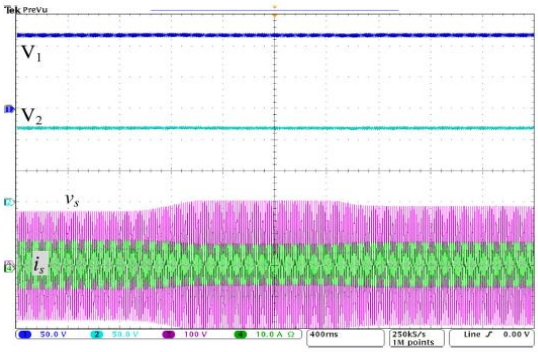



Fig. 12. Supply voltage variation while the output dc voltages are regulated at 125 V as buck mode of operation.

## V. CONCLUSION

Air conditioning DC change is currently generally utilized as a part of numerous applications like SMPS, ASD's battery charging unit and so on. Multilevel converter is currently use for creating low music. This proposition in view of the new topology for AC-DC transformation with lessens number of switch.

For finishing of theory right off the bat review the writing of given in part 2. In part 3 examine the different approach for control system of the converter. Based on this here proposed new topology for control factor revision. Here in theory a diminish number of switch is utilized for age of 5 level lift converter. For transformation of AC-DC here required three switches.

To approval of the framework, the framework is reenacted in MATLAB programming. MATLAB programming is capable programming for recreation of the work. Results demonstrate the proposed framework create solidarity control factor appeared in result area. Additionally create DC yield for amendment.

Future work:

Every work has some drawback. This drawback is used for advancement in future work. Some of important future work as:

The proposed system is based on single phase supply system. In future this system is applicable in 3-pgase system to.

In this proposed work harmonics related topic is not consider so in future harmonic related work is consider.

In future increasing level is considered for more advancement or reduction in harmonics.

## REFERENCES

[1] W. Y. Choi, J. Kwon, E. H. Kim, J. J. Lee, and B. H. Kwon, "Bridgeless boost rectifier with low conduction losses and reduced diode reverse-recovery problems," IEEE Trans. Ind. Electron., vol. 54, no. 2, pp. 769–780, April 2007.

[2] J. M. Kwon, W. Y. Choi, and B. H. Kwon, "Cost-effective boost converter with reverse-recovery reduction and power factor correction," IEEE Trans. Ind. Electron., vol. 55, no. 1, pp. 471–473, Jan. 2008.

[3] F. L. Tofoli, E. A. A. Coelho, L. C. de Freitas, V. J. Farias, and J. B. Vieira Jr., "Proposal of a soft-switching single-phase three-level rectifier," IEEE Trans. Ind. Electron., vol. 55, no. 1, pp. 107–113, Jan. 2008.

[4] L. Rossetto, G. Spiazzi, and P. Tenti," Control techniques for power factor correction converters", in Proc. Power Electronics, Motion Control (PEMC), September 1994, pp. 1310–1318.

[5] K. M. Smedley and S. Cúk, "One-cycle control of switching converters", IEEE Trans. Power. Electron., vol. 10, no. 6, pp. 625–633, Nov. 1995.

[6] D. Borgonovo, J. P. Remor, I. Barbi, and A. J. Perin, "A self-controlled power factor correction single-phase boost pre-regulator", in Proc. IEEE 36th Power Electronics Specialists Conference (PESC '05), 2005, pp. 2351–2357.

[7] R. Martinez and P. N. Enjeti, "A high-performance single-phase rectifier with input power factor correction," IEEE Trans. Power Electron., vol. 11, no. 2, pp. 311–317, Mar. 1996.

[8] J. W. Lim and B. H. Kwon, "A power factor controller for single-phase PWM rectifiers," IEEE Trans. Ind. Electron., vol. 46, no. 5, pp. 1035–1037, Oct. 1999.

[9] W.-Y. Choi, J.-M. Kwon, E.-H. Kim, J.-J. Lee, and B.-H. Kwon, "Bridgeless boost rectifier with low conduction losses and reduced diode reverse-

recovery problems," IEEE Trans. Power Electron., vol. 54, no. 2, pp.1406–1415, April 2007.

[10] B. Su and Z. Lu, "An interleaved totem-pole boost bridgeless rectifier with reduced reverse-recovery problems for power factor correction," IEEE Trans. Power Electron., vol. 25, no. 6, pp.769-780, June 2010.

[11] Y. Jang and M. M. Jovanovic, "Interleaved boost converter with intrinsic voltage-doubler characteristic for universal-line PFC front end," IEEE Trans. Power Electron., vol. 22, no. 4, pp. 1394–1401, July 2007.

[12] D. J. Perreault and J. G. Kassakian, "Distributed interleaving of paralleled power converters," IEEE Trans. Circuits and Systems I: Fundamental Theory Application, vol. 44, no. 8, pp. 728–734, Aug. 1997.

[13] B. A. Miwa, D. M. Otten, and M. E. Schlecht, "High efficiency power factor correction using interleaving techniques," in Proc. IEEE Applied Power Electronics Conference and Exposition, 1992, pp. 557–568.