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DESIGN AND IMPLEMENTATION OF SINGLE LEG DUAL OUTPUT INVERTER

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Abstract: In this paper, two single phase ac loads are supplied with one inverter and reduced switch count topologies are introduced in this paper. It has three switch single leg structures. This single leg inverter is functionally comparable to half bridge inverter working independently though with a less number of semiconductor switch and hence control and gate drive circuit components. This three switch topologies has two modes of operation which are equal frequency (EF) and different frequency (DF). Each modes of operation has its own distinctive characteristics are considered for them and their PWM schemes are elaborated. Comprehensive analysis of power loss profile and output waveform properties are conducted via simulation and their result is compared with half bridge inverter.

I. INTRODUCTION

The usual approach to fulfil the growing demand for independently supplying a number of ac loads in several applications is by using separate inverters for each of them. This may lead to undesirable increase in system cost, size and weight. There is a growing trend in power electronics for reduced switch count power converters with the aim of sustaining high power quality and enhancing the system reliability. Dual-terminal converters provide the researches with an extra degree of freedom in realizing switch reduction of power converters resulting in system cost, size and weight optimization. Dual-terminal reduced switch count topologies may be utilized as ac/ac converters for conditioning the input ac power, (regulating input voltage/current) dual-output inverters to independently supply two ac loads [9-12]. Four-leg inverter is the pioneering effort initiated with the purpose of reducing the number of switches by replacing a switch-leg with a split-capacitor-leg and sharing it between two power converters. The configuration was proposed as a VSI-PWM rectifier/inverter system in and as a dual-ac-drive system. Subsequently, the idea of replacing a switch leg with a split-capacitor-leg and sharing a leg between the two stages of power conversion is implemented in several configurations. References [2] and [8] have suggested a number of reduced switch counts single-phase to three-phase ac/ac converters by implementation of the same idea. Moreover, some reduced switch count topologies in which there is no split-capacitor-leg and switch reduction is realized by simply sharing a switch-leg are proposed in [3] and [4] as single-phase three-leg type converter and in [5] and [6] as respectively five-leg and six-leg converter topologies. Sharing a switch-leg in a group of ac drive systems is also proposed in [11] and a general PWM method applicable for any number of machines in the group is presented in [12].

II. THREE - SWITCH INVERTER TOPOLOGY

Fig. 1 shows the proposed three-switch inverter which is actually developed by replacing a leg of the six -switch inverter with a series combination of capacitors at the cost of losing zero output voltage state so as to further economize the inverter cost by reducing the number of power switches. The single-leg topology which uses only three semiconductor switches for independently supplying two single phase loads is structurally comparable to two half-bridge inverters with a common row of switch and capacitor (middle row of the proposed structure). The output voltages of the three-switch inverter can be expressed as $V_{ox} = (1/2)M_xV_gSin(\omega_xt+\varphi_x)$ where x denotes upper or lower output similar to single-phase half bridge inverter except that the modulation indices M, frequencies ω and phase difference φ of the output references face some constraints depending on the inverter DF and EF operation modes.

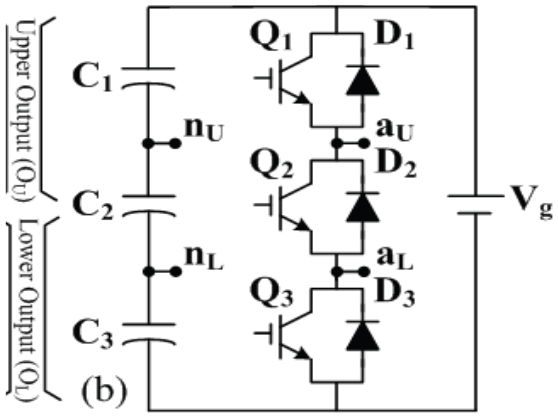

Fig. 1: Three switch inverter

Three-switching states of Fig. 1 are possible for the three-switch inverter. There is no zero state for neither of the outputs in this inverter. Moreover, the low level of an output voltage may not be negative of its high level and voltage levels of the upper and lower outputs may not be equal depending on the capacitor voltage levels. When the lower switch is OFF state a both outputs are positive, when the upper switch is OFF state c both outputs are negative and when the middle switch is OFF the upper output is positive

and the lower output is negative. Similar to the six-switch inverter, three-switch inverter can use these states to function in two operation modes of DF and EF considering frequency/amplitude independency of the output voltages.

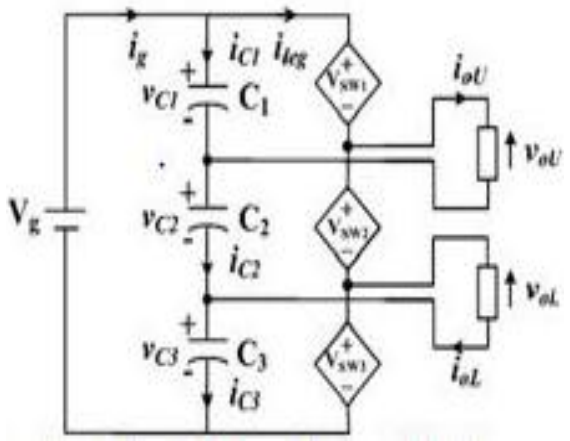

Fig. 2: Equivalent circuit for exploring voltages of dc-link capacitors

A. Different frequency mode of operation

DF operation enables the inverter to produce two output voltages independent of each other from both frequency and amplitude aspects. Turning the lower switch ON for producing the upper output voltage and vice versa, the two inverter outputs can function independently. This is achieved by portioning the modulation space out among the two voltage references via adding appropriate offsets to them. For this purpose upper and lower output voltage reference waveforms should respectively be shifted up and down in the modulation space occupied by the carrier signal (Fig. 3). This prevents interference of modulating signals and hence provides frequency independency in the outputs.

B. Equal frequency mode of operation

Since the inverter outputs have equal frequencies in this mode, the maximum modulation index can be increased up to one depending on the phase difference between the references. Similar to the six- switch inverter, (2) should be satisfied and offsets of (3) can be added to the output voltage references (Fig. 4(b)) to prevent their interference. Fig. 5 is used for upper, middle and lower switch gate signal generation.

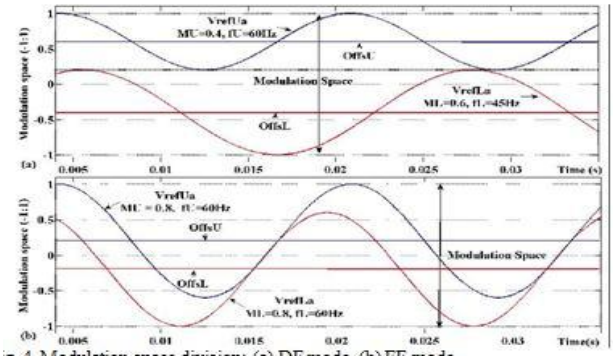

Fig. 3: Modulation space division

Switching states

Switching State1
Switching State2
Switching State3

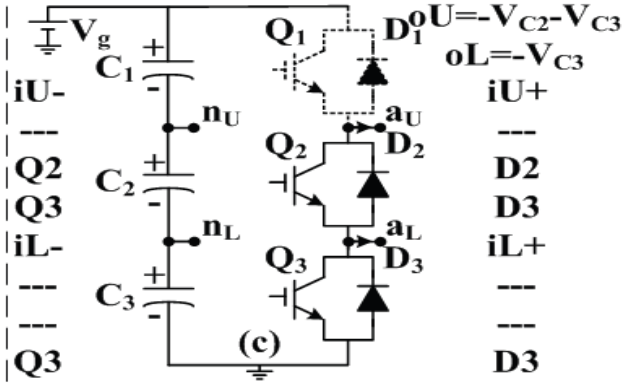

Fig. 4: State 1

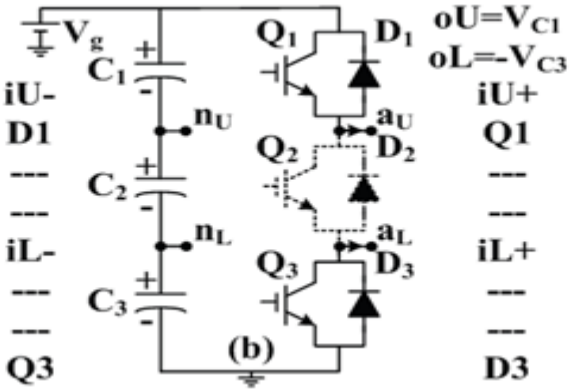

Fig. 5: State 2

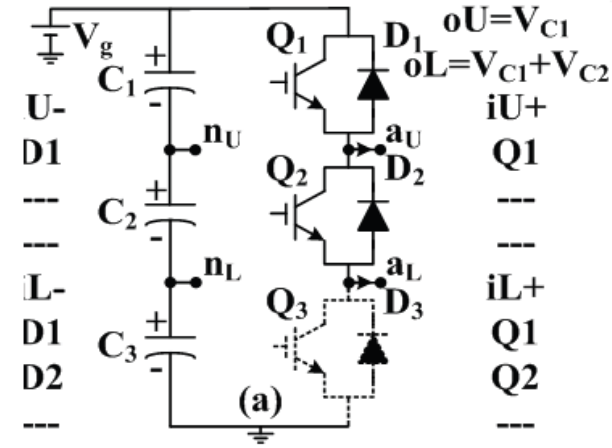

Fig. 6: State 3

C. Investigation of dc-link voltage balancing

In this section voltage sharing on dc-link capacitors is studied and it is shown that the offsets added to the references determine the capacitors voltage levels. Dc-link voltages are investigated by replacing the switches with dependent voltage sources controlled by gate command signals. The equivalent circuit is depicted in Fig. 2. It is

assumed that the natural time constants of the converter network are much longer than the switching period.
Noticing that at any moment only one switch is off, the average voltages over a switching cycle can be obtained using the switch off time interval which according to Fig. 6 is T_1, T_3 and $T_2=T_s-(T_1+T_3)$ for the upper, lower and middle switches respectively.

D. Capacitor sizing

As stated dc voltage sharing on capacitors is not related to their size. However the ac voltage component across the capacitors i.e. voltage ripple, which depends on the size of capacitors should be negligible. Using superposition principle for upper and lower output frequencies and ac steady state circuit analysis techniques, the general term for ac voltage component on dc-link capacitors can be obtained. To provide an insight into the nature of the ac ripple and to achieve a tangible result comparable to half-bridge inverter, a typical case is studied here in which a final condition as follows will be imposed on capacitor sizes. This condition resembles having similar capacitors at the dc-link of half-bridge inverter - the total reactive power delivered by the capacitors is zero.

E. THD analysis

Output voltage total harmonic distortion (THD) is compared between the six switch and full bridge inverters and between the three-switch and half bridge inverters in Fig. 9(a) and (b)

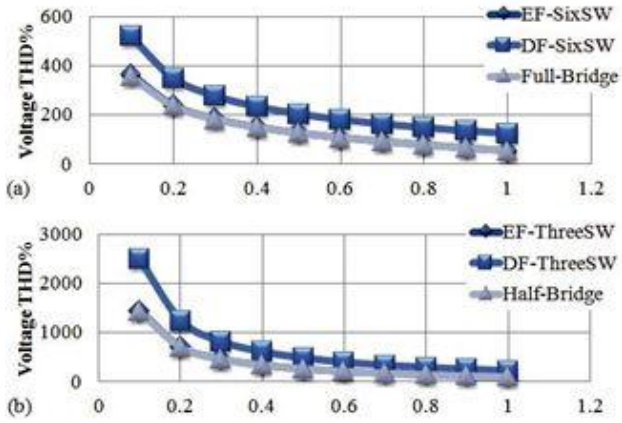

Fig 7

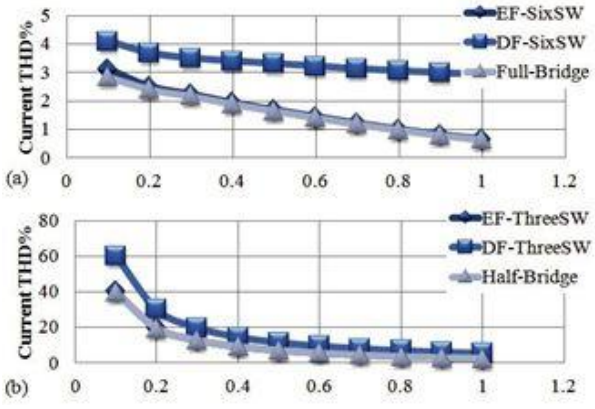

Fig.8

F. Semiconductor loss analysis

The power loss profile of the three-phase nine-switch ac/ac converter is thoroughly investigated. The results are compared to the conventional 3Ø back-to-back (B2B) VSC. Since the inverter operation has distinctive characteristics, loss analysis is conducted for the proposed dual-output topologies and their counterpart inverters employing the same method used for the same switches so as to first explore the semiconductor loss profile of the proposed inverters in comparison with conventional topologies and second to highlight the differences between the inverter and ac/ac converter operations. Since the required dc bus voltage level of the proposed topologies changes according to Table II, semiconductor switches of different voltage ratings should be used.

CURVE FITTED SWITCH PARAMETERS USED IN LOSS ANALYSIS

Parameters	600V/50A IGBT RSM50GB60DLC		1200V/50A IGBT RSM50GB120DLC
V_{dc}	200	400	800
V_{T0}	0.774	0.774	0.82
r_{CE}	0.031	0.031	0.036
V_{D0}	0.635	0.635	0.68
r_D	0.013	0.013	0.024
A_{onT}	0	0	0.467
B_{onT}	0.01785	0.0357	0.153
A_{offT}	0.04762	0.0952	1.867
B_{offT}	0.01192	0.02348	0.133
A_{onD}	0.2693	0.54	1.267
B_{offD}	0.00795	0.01587	0.1

Considering the fact that the price of low voltage switches varies in a narrow range and that the decreased number of switches overshadows the required higher switch voltage ratings, same switches are used for six-switch inverter DF and EF mode loss analysis to gain a reasonable level of understanding of the inverter loss behavior when the same switches are used. On the other hand, first due to the considerably increased dc bus voltage level of the three-switch inverter and second to investigate the effect of using different switches on the inverter loss profile, different switches are used in loss analysis of DF and EF modes of the three-switch inverter. The curve fitted parameters of the employed switches such as V_{T0}, r_{CE}, A_{onT}, B_{onT}, etc are shown in Table III. Reference [23] has proposed a straightforward method for PWM-VSI inverter loss calculation by developing inverter loss model based on experimental determination of the power losses. The simplified equations of loss calculation which are obtained by linearizing the turn-off and turn-on energy curves around the operating point are defined in (13) where P_{con} denotes conduction loss of the switch (T) or the diode (D) and $P_{on/off}$ denotes their turn-on and turn-off loss power over the output fundamental cycle (T_0)

In EF mode of both six-switch and three-switch inverter topologies the switching loss of the middle row semiconductors is zero because the modulation index of the upper and lower in-phase outputs have been increased simultaneously without adding any offsets and hence the middle switches are always ON. Furthermore, despite the nine-switch ac/ac converter in which power losses of the

middle switches are higher than the upper and lower switches, the upper and lower switches of the dual-output inverters have a bigger share of the total power loss. The reason of this dissimilarity can be understood noting that the current of the upper and lower switches is the sum of the upper and lower load currents whereas the middle switches only conduct one load current at any moment. In EF mode, when the output voltages are in-phase, the output currents nullify each other to some extent in upper and lower switches while operating as an ac/ac converter because of the power flow direction whereas in inverter operation they amount to a greater value. In inverter operation, although the average current of the switches is the same over the fundamental output frequency, owing to the RI^2 component of the conduction loss, higher instant current of the upper and lower switches intensifies their conduction loss. This is also the reason of greater semiconductor loss in EF mode of the proposed dual-output topologies compared to their counterpart single-output inverters.

III. CONCLUSION

Dual-leg and single-leg reduced switch count dual-output inverter topologies based on three-switch inverter legs were proposed in this paper with the aim of reducing cost, size and weight of low power inverters. The performance of the proposed topologies was compared to the conventional topologies regarding the output waveform characteristics and semiconductor power losses.

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