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GLITCHLESS DIGITALLY CONTRLLED DELAY LINES FOR POWER OPTIMIZATION

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Abstract: ***The project GLITCHLESS DIGITALLY CONTROLLED DELAY LINES FOR POWER OPTIMIZATION reduces the power consumption by avoiding the glitches that enter into the circuit. The proposed system uses the gated clock for reducing the power consumption. The delay element based digitally controlled delay-lines (DCDL) present a glitching problem limiting their employ in many applications. The existing system of DCDL allows reducing the glitching problem occurring in the circuit.***

I. INTRODUCTION

A glitch is a short-lived fault in a system. Glitch is a transient fault that corrects itself, and it is difficult to sense the error. The term glitch is also used in the computing and electronics industries, and in circuit bending, including in video games. The glitching problem is applied to all types of systems which includes human organs and nature. In other words glitch is an undesired transition that occurs before the signal settles to its intended value. An electrical pulses of short duration is the glitch, which results in fault or design of circuits with error, particularly in a digital circuit. Flip-flops are triggered by a pulse. The pulse must not be shorter than a specified minimum duration. If the pulse is below the minimum duration, the component may malfunction. The pulse shorter than the specified minimum duration is the glitch. The race condition occurring in the design of digital circuits pays the way for glitching problem. The time taken for a signal to propagate from one point to another is called the delay. In Digital circuits the propagation delay or gate delay, is the time taken which starts when the input to a logic gate becomes stable and valid, to the time that the output of that logic gate is stable and valid. The gate consists of several transistors .the switching time of the gate depends on the switching time of the transistor. It takes some time to change the output for the change in the input. Processing data at a faster rate reduces the gate delay and improves the overall performance. The propagation delays of logic elements may differ and is the major contributor to glitches in asynchronous circuits which results in race condition. The principle of logical effort utilizes propagation delays to compare designs implementing the same logical statement. Propagation delay increases with operating temperature, power supply voltage as well as an increased output load capacitance. The supply voltage is the largest contributor for the increase of propagation delay. The propagation delay increases substantially, when the output of a logic gate is connected to a long trace or used to drive many other gates (high fan-out). Gates can have propagation delay ranging from more than 10 nano second to the Pico second range. This delay depends on the technology being used for implementing the circuit. For an electric signal, it is the time taken for the signal to travel through a wire. The other different types of delays include source delay, network delay, insertion delay, transition delay, path delay, intrinsic delay, phase delay which causes glitching problem. A digital delay line is a discrete element, which allows a signal to be delayed by a number of samples. The digital delay lines are often implemented as circular buffers, if the delay is an integer multiple of samples. This means that integer delays can be computed very efficiently. To simulate room acoustics, musical instruments and digital audio effects the digital delay lines are used. The DCDL are designed glitch free and it is implemented in the application for the better performance. A necessary condition to avoid glitching is designing a DCDL which have no-glitch in presence of a delay control-code switching. This is a major issue at the DCDL-design level. The project carries out delay elements which have no glitches and have good resolution which improves the performances in the digital applications. The delay element can be used to build a delay locked loop(DLL).The paper contribute to the glitch less DCDL with the driving circuits for the delay control bits of the glitch free DCDL implemented in the delay locked loop(DLL) by using gating technique.

II. EXISTING NAND BASED DCDL

The following figure shows the block diagram of the existing NAND based DCDL. It consists of a NAND based lattice delay units which is cascaded for larger delay lines in application.

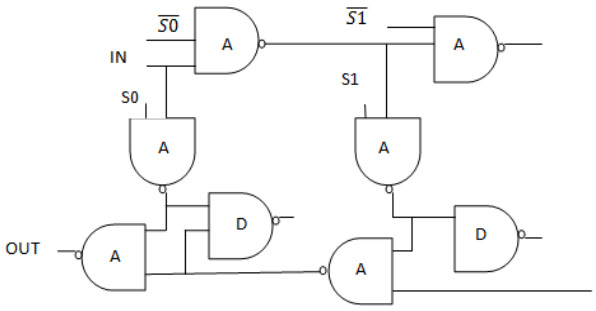

Fig. 1: Block diagram of the conventional DCDL with one control bit

The conventional DCDL was designed with NAND cell as lattice structure .In the figure 1 the cell which is denoted by "A" is the fast input of the NAND gate. Gates denoted by "D" is the dummy cell. The dummy cell is used for the load balancing. The delay elements are controlled by one bit control code c for the delay propagation. When the delay control code C incremented by 1, multiple propagation path within the DCDL structure generates leads to more glitching in the delay line. The control bit Si = 0 (pass state), Si = 1 (turn state). In DCDL applications, the switching of delay control-bits is synchronized with the switching of the input signal to avoid DCDL output glitching. Glitching can be avoided by lowering the arrival time of the control bits than the arrival time of the input signal of the first DE which switches from or to the turn-state.

III. GLITCH FREE NAND BASED DCDL WITH TWO CONTROL BITS

The structure proposed in this fig 2 has control bits to control the delay elements .In that "A" denotes the fast input of the NAND gate ,"D" denotes the dummy cell for the load balancing. Two control bits Ti and Si are used to synchronize the arrival of the input and the arrival of the control bits. The delay element has three possible conditions.

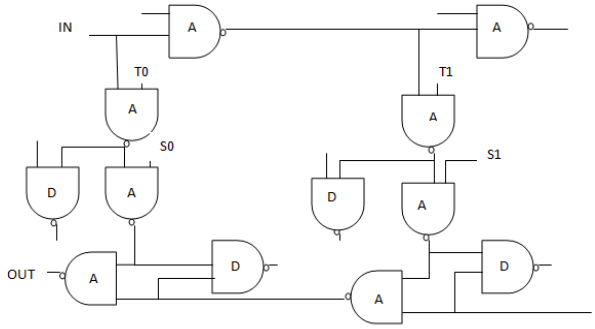

Fig. 2: Block diagram of the Glitch free DCDL with two control bit

TABLE I
LOGIC-STATES OF EACH DE IN PROPOSED DCDLS

S_i	T_i	DE state
0	1	*Pass*
1	1	*Turn*
1	0	*Post-Turn*

The DEs i<c with are in pass-state (Si =0,Ti =1). In this state the NAND "3" output is equal to 1 and the NAND "4" allows the signal propagation in the lower NAND gates chain. The DE with i=c is in turn-state (Si=Ti=0). In this state the upper input of the DE is passed to the output of NAND "3". The next DE(i=C+1) is in post-turn-state .In this DE the output of the NAND "4" is a fault called stuck-at 1, by allowing the propagation, in the previous DE (which is in turn-state), of the output of NAND "3" through NAND "4". All remaining DEs (for i>C+1) are again in turn-state .The three possible DE states of proposed DCDL and the corresponding Si and Ti values are summarized in Table. The simulation results shows that the proposed NAND based DCDL confirms the glitch less propagation in the delay elements.

IV. IMPLEMENTATION OF DCDL USING GATING TECHNIQUE

A Delay-Locked Loop (DLL) is implemented using gating technique. In the gating technique an AND gate is used. Through the AND gate the clock is given as one input and the control bit is given as the second input. The logic state of the delay element is shown in the above table. The glitch free DCDL is implemented in the gating technique. Glitches in the delay units are avoided by the clock signal feeding through the AND gate along with the control bits. Arrival of the input control code is designed in such a way so that the propagation of the signal through the gates does not produce glitches. Driving circuits for the control codes are also designed that the difference in the driving control bits are designed with the proper timing constraint and delay. Thus the NAND based delay line is implemented with glitches and without glitches for the comparison of the output. Thus with this, the glitches can be well studied and analyzed for the better delay circuits.

V. SIMULATION RESULT

	IMPLEMENTATION OF CONVENTIONAL DCDL	IMPLEMENTATION OF PROPOSED DCDL
Power(µw)	12.671	9.221
Delay (ns)	10.498	7.760

VI. CONCLUSION

A NAND-based DCDL which avoids the glitching problem of previous circuit has been presented. As an additional result, we add clock gating technique to reduce power consumption. The developed model provides also the timing constraints that need to be imposed on the DCDL control-bits in order to guarantee a glitch-free operation. Micro wind and Xilinx simulation results show our proposed technique reduces power consumption considerably.

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