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DESIGN AND SIMULATION OF QUADRATURE PHASE SHIFT KEYING SUB-SYSTEM USING REVERSIBLE LOGIC

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Abstract: Reversible logic is the emerging technology in digital era because of its high frequency of operation and small area utilization compared with conventional logic. QPSK (Quadrature Phase Shift Keying) is a type of modulation technique in a wireless communication system, as it supports faster transmission of data compared to other modulation techniques. In this paper, an implementation of QPSK using reversible logic is proposed with some design modifications. Verilog HDL used to implement the proposed QPSK modulators and it will be simulated on the Xilinx ISE 13.2 software platform. We compared existing modulator implemented with Boolean logic and it feasibility of using reversible logic is presented.

Keywords: Conventional logic and gates, Reversible logic and gates, QPSK, Verilog coding.

I. INTRODUCTION

QPSK modulation is a key feature commonly used in wireless communication for data transmission and to minimize antenna design. Baseband data of conventional QPSK modulator operates by separating I and Q phases and add them to get a QPSK signal. The generation of carrier wave for the operation of the modulator consumes high power. The quadrature form of the modulation equation is given by

$$s(t) = \sqrt{\frac{2E_s}{T}}\cos(\theta(t))\cos(2\pi f_c t) - \sqrt{\frac{2E_s}{T}}\sin(\theta(t))\sin(2\pi f_c t) \quad \text{... Eq (1)}$$

QPSK allows the signal to carry twice as much information as ordinary PSK using the same bandwidth. QPSK is used for satellite transmission of MPEG2 video, cable modems, video conferencing, cellular phone systems.

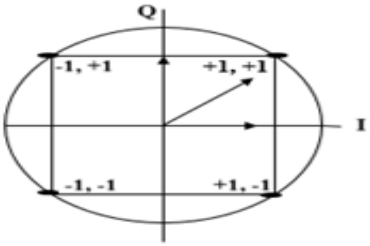


Fig. 1: QPSK Constellation

Figure 1 shows the constellation diagram [9] and the phases of the symbols and their relationship to each other. The x-axis projection is equal to I channel amplitude and the y-axis projection is equal to Q channel amplitude. The constellation diagrams are always done at baseband, i.e. fc = 0.

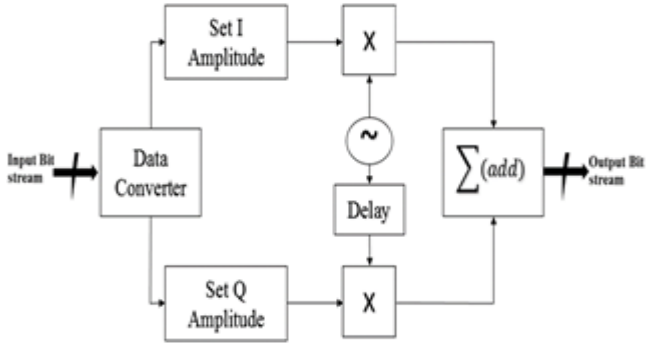


Fig. 2: QPSK Block Diagram

Figure 2 shows the block diagram of QPSK modulator [9], where Serial to parallel converter splits the incoming bit stream with a bit rate of Rb into two streams, each of half the bit rate. I and Q amplitudes are set from a table lookup function, depending on the dual bit pattern coming in. Carrier frequency ω is used to individually modulate I and Q bit streams. Next these are added to get the modulated QPSK signal.

Figure 3 shows the QPSK waveform [9], by modulating I channel with I carrier values and Q channel with Q carrier values. Then I and Q values are added to get the real modulated QPSK signal

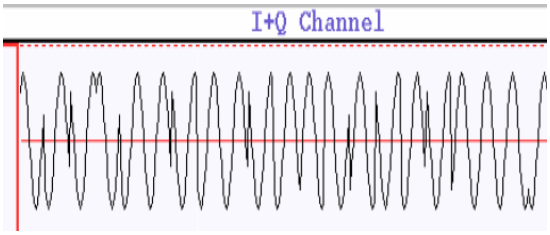


Fig. 3: QPSK Modulated Wave

II. REVERSIBLE GATES

Everyday new technology is developing rapidly, the clock frequency also increasing continuously to achieve greater speed. Hence Reversible logic is the efficient technique in the recent trends due to its high frequency of operation. Moore's law predicts exponential growth of heat generated due to information loss reduces performance and lifetime of the circuits. Several reversible gates are used to build the specific reversible logical functionalities. In this paper, we used

several gates like Feynman [6], Fredkin [7] and Toffoli [8].

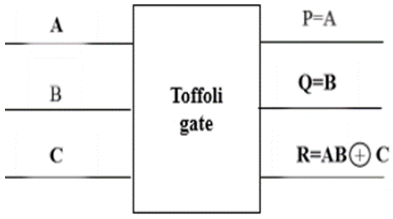


Fig. 4: Toffoli Gate

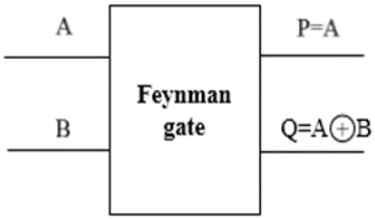


Fig. 5: Feynman Gate

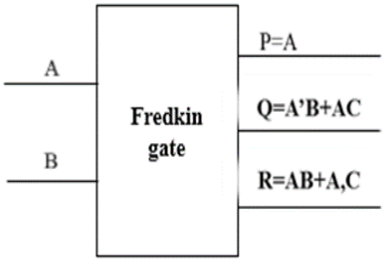


Fig. 6: Fredkin Gate

III. PROBLEM IDENTIFICATION

As by Kavita A. Monpara, Shailendrasinh B. Parmar [1], for high speed communication and space applications power and bandwidth are the most important parameters. The size of PCB and component count is also important parameters. To reduce these all parameters a new design approach of QPSK is needed. In this modulator design summation, orthogonal sub-carrier generation and mixing of subcarrier with data are all digitally implemented inside the FPGA. Naveen. K. B, Prashantha. N. C [10] presented the design and implementation of QPSK modulator using reversible logic of the traditional analog system. Here QPSK modulator unit modelled using HDL code and simulated by Modelsim 6.0 simulator to verify their functionality in the system. The digital QPSK modulator using reversible logic gates yields low power, small area and reduced amount of delay. Reversible logic is mainly used to construct low power circuits. Gordon. E. Moore [3] in 1965 stated that the numbers of components on the chip will double every 18 months. His prediction is only for 10 years, but due to growth in the integrated-circuit technology his prediction is still on the way with some changes. His work is called as the Moore's law. The effect of Moore's law made the researchers to conclude that as the number of components in the chip increases the power dissipation will also increase exponentially. Hence minimization of power factor has become an important factor for today's VLSI engineers. A lot of work has been done on implementing QPSK using MATLAB or by using software platforms but not with reversible computing. It is in this paper, a QPSK sub-system will be designed with Verilog and simulated using XILINX 13.2V tool. The feasibility of using reversible computation principles in implementing the QPSK sub-system will be researched in this paper.

IV. DESIGN DESCRIPTION

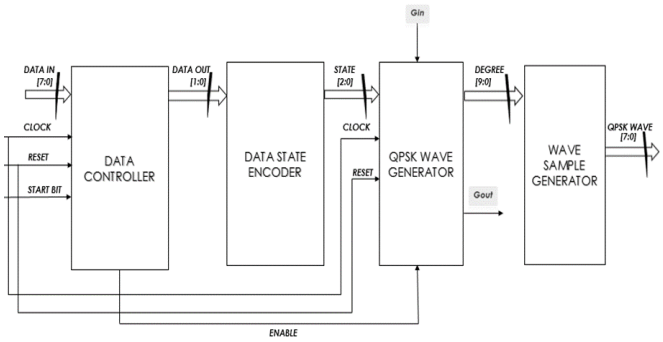


Fig. 4: Proposed Block Diagram

Data Controller: selects the input data based on the clock and reset condition, that is

If clock=0, data select=0

Clock=1, data select= input data

And

If reset=1, data select=0

Reset=0, data select= input data

Depending on the above conditions we group each two bits of input data to feed next stage using state machine shown in figure 5.

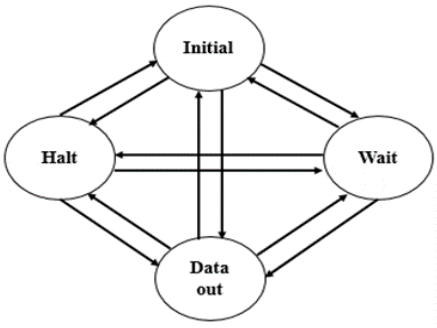


Fig. 5: Data Controller State Machine

Data State Encoder: This state encoder is based on combo logic, where depending upon the two bit input the state encoder makes the phase change for transmission of data.

Table. 1: States of Encoder

Input data	States	Corresponding Phase change in degrees
00	0	00
01	3	900
10	5	1800

11	7	2700

QPSK Wave Generator: Figure 6 shows Finite state machine functionality, which is used to select degrees with respect to the state encoder values. The binary equivalent of each degree is assigned using fixed decimal conversion to binary signed method, each of which ten bit wide.

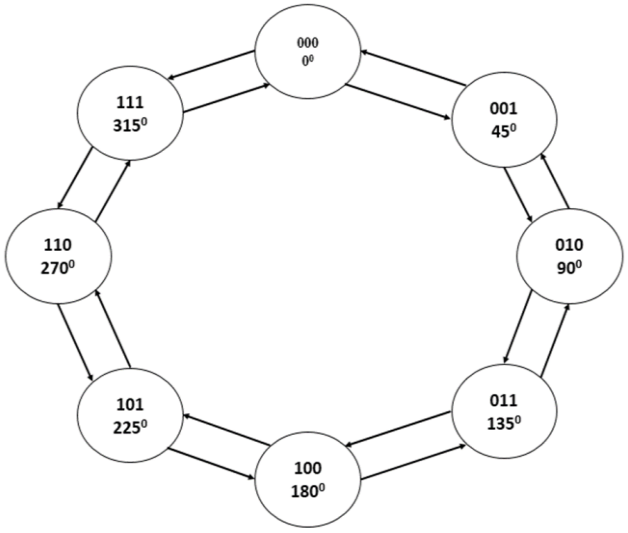


Fig. 6: Finite State Machine

Depending on the garbage input condition i.e.
If gin=0, state machine gives previous state (antilock wise).
If gin=1, state machine gives the next state (clock wise).

Wave Sample Generator: this block generates the 8 bit QPSK wavelets based on the 10 bit value fed by previous block equivalent to input data.

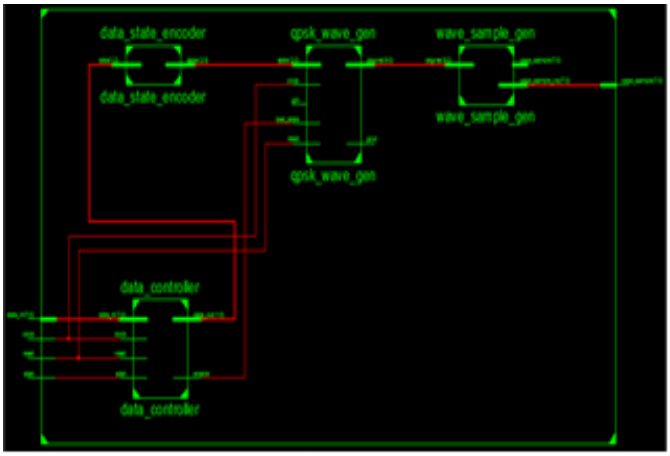


Fig. 7: RTL Schematic of Proposed Block Diagram

V. PROPOSED METHODOLOGY

The data controller in this design is modified with reversible MUX for data selection, counter using the Toffoli gate to create waiting time. Reversible mux is used to create the data state encoder block to change the phase of the signal with respect to two bit input data from a data controller. The functionality of QPSK wave generator is reversed by taking extra garbage input and output. Delay upon this gin value the operation of the generator is reversed.

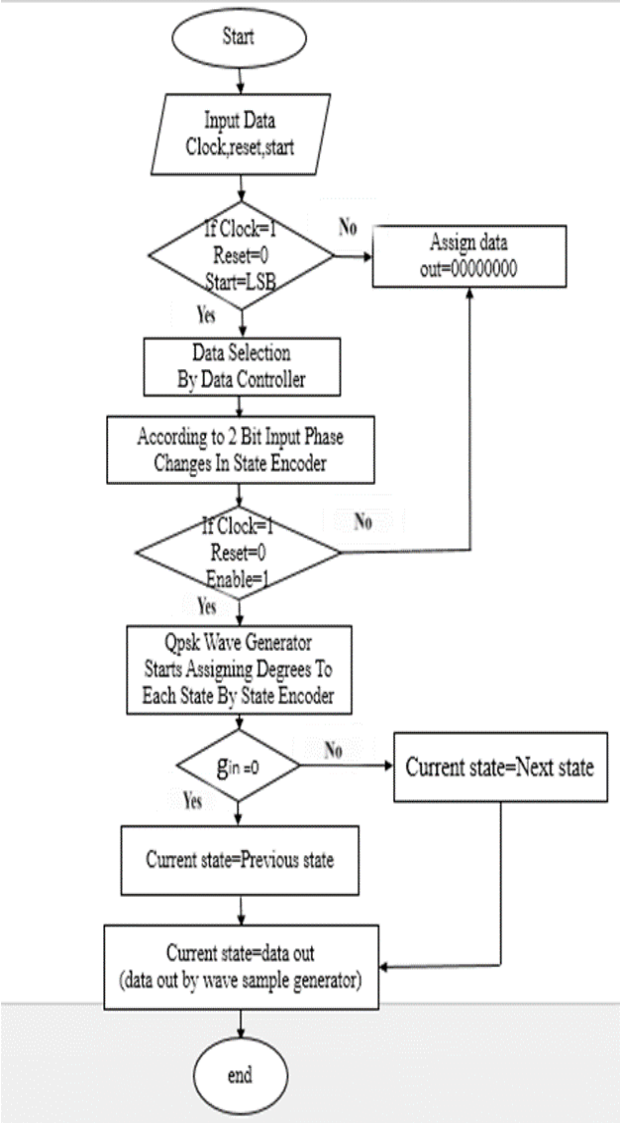


Fig. 7: Flow Chart

VI. EXPERIMENTAL RESULTS

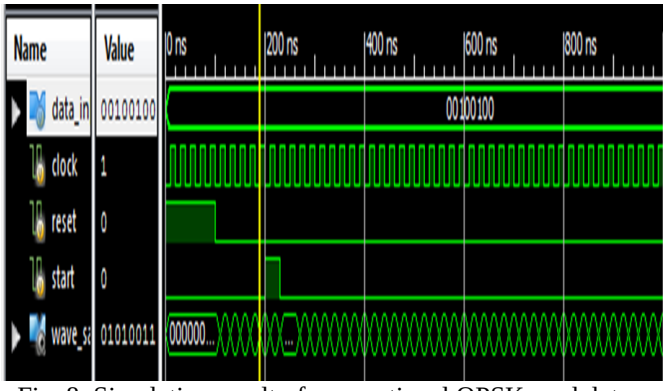


Fig. 8: Simulation result of conventional QPSK modulator

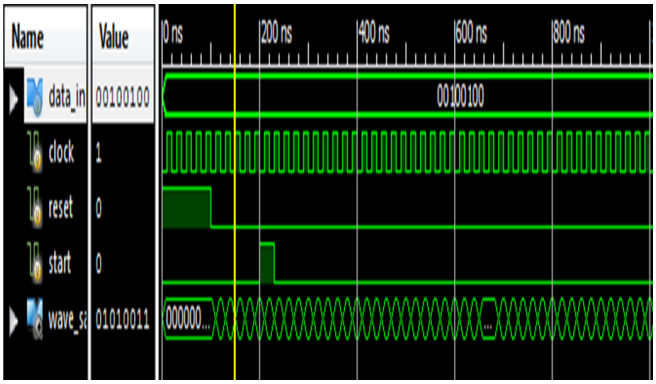
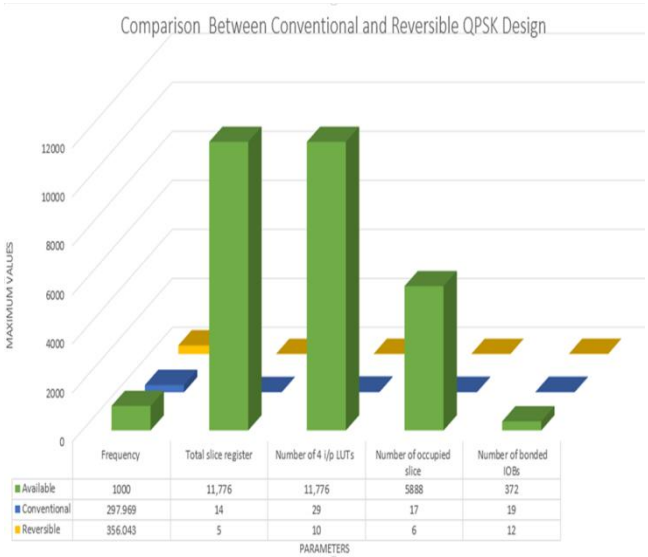


Fig. 9: Simulation result of reversible QPSK modulator

Figure 8 and 9 shows simulated result for both conventional and reversible QPSK modulator, where 8 bit data 00100100 with clock set to 1, reset set to 0 and start bit is 0 based on the input data stream is simulated based on the above methodology to get QPSK output stream 01010011.

Parameters	Available	Conventional design	Reversible design
Frequency	----	297.969MHz	356.043MHz
Total Number slice register	11,776	14	5
Number of occupied slices	5888	17	6
Number of 4 i/p LUT's	11,776	29	10
Number of bonded IOBs	372	19	12

Table. 2: Result comparison



Graph. 1: Comparison between Conventional and Reversible QPSK Design

VII. CONCLUSION

In this paper, we presented QPSK modulator designed using reversible logic and gates. Designed reversible QPSK modulator yields high frequency of operation and smaller area utilization with respect to conventional QPSK modulator design. The proposed design can be used for high speed communication system applications.

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