International Journal For Technological Research In Engineering
Volume 1, Issue 10, June-2014 *ISSN (Online): 2347 - 4718*

LOW-POWER HIGH-SPEED SAMPLE AND HOLD CIRCUIT BASED ON SWITCHED CAPACITOR

Harsh Thekdi[1], Mehul L. Patel[2] (Head)
Electronics & Communication
LCIT, Bhandu, Dist.: Mahesana, India

Abstract— Switched-capacitor techniques have been developed in order to allow for the integration on a single silicon chip of both digital and analog functions. Switched capacitor circuit replaces a resistor with switches and capacitors and works by passes charge into and out of a capacitor by controlling switches around it. They are suitable for on chip implementations because they replace a resistor with switches and capacitors. The sample and hold block is typically used as such analog to digital interface in front of ADC. The operation cycle of sample-and-hold block is divided into two phases: the sampling phase and the hold phase. Then by selecting appropriate circuits open-loop sample and hold circuit based on SC and closed-loop sample and hold circuit based on SC and is simulated in Mentor graphics tool. Open-loop S & H circuit gives less delay but less accurate. Closed-loop S & H circuit gives greater delay but more accurate. Circuit simulation, schematic has been done in generic 90nm Technology file TSMC 0.18µm and 0.35µm Technology file. SPICE code has been written in GEDIT, while simulated in ELDO SPICE Simulator. Layout and schematic has been drawn using ICSTUDIO, CALIBRE is used for post layout simulation.

I. INTRODUCTION

With the explosive growth of wireless communication system and portable devices, the power reduction of integrated circuits has become a major problem. With the rapid growth of internet and information on-demand, handheld wireless terminals are becoming increasingly popular. With limited energy in a reasonable size battery, minimum power dissipation in integrated circuit is necessary. Many of the communication systems today utilize digital signal processing (DSP) to resolve the transmitted information. Therefore, an analog-to-digital interface is necessary, between the received analog signal and DSP system. This interface achieves the digitization of received waveform subject to a sampling rate equipment of the system. Switched capacitor circuits are widely used in all signal processing and circuits due to their accurate parameters governed by capacitor ratio. Switched capacitor circuits play a critical role in mixed signal, analog to digital interfaces. They implement a large class of functions, such as sampling, filtering and digitization necessary. With increasing demand for high-resolution and high speed in data acquisition systems, the performance of the sample and hold circuit is becoming more and more important. The sample and hold block is typically used as such analog to digital interface in front of ADC. The use of sample and hold circuit allows most dynamic errors of ADC's to be reduced especially those occurring with high frequency input signals. So the sample and hold must exhibit the better performance than the ADC in terms of accuracy, speed, and power dissipation. The main application of this sample and hold circuit is in the low-power and high-speed pipelined ADCs.

II. TYPES OF SAMPLE AND HOLD CIRCUIT BASED ON SC

There are basically two types of the sample and hold circuits based on the switched capacitor.

- Open-loop sample and hold circuit based on switched capacitor
- Closed-loop sample and hold circuit based on switched capacitor

III. OPEN-LOOP S & H BASED ON SC

The simplest practical S&H circuit is shown in Figure 1.1, which is often referred to as the open-loop S&H architecture. The advantages of this open-loop S&H architecture are the high speed and the unconditional stability, since no global feedback is used. However, the accuracy of an open-loop S&H circuit is limited by signal-dependent errors due to the charge injection, switch on-resistance, and finite clock slope. Despite some early proposals to minimize signal-dependent errors (e.g., cascading a dummy transistor with the sampling switch or using a CMOS transmission gate for switching), the maximum achievable linearity of a standard open-loop CMOS S&H is limited to about 8 bits (i.e., with an overall SDR of about 48 dB). In practice, low-leakage and high-speed bipolar diode bridges are often adopted to build the sampling switches in open-loop S&H circuits for very high speed (up to 1.25 GHz) and high-accuracy (9 to 12 bits) sampling applications.

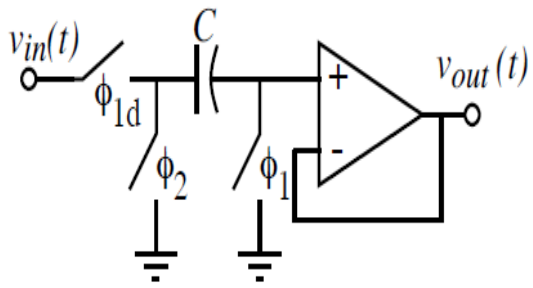


Fig. 1 Open-loop S & H based on SC

- Delayed clock used to remove input dependent through.
- Differential version has low PSRR (power supply rejection ratio), cancellation of even harmonics, and reduction of charge injection and clock feed-through.

IV. CLOSED LOOP S & H BASED ON SC

As an alternative to special source followers and bootstrapped clocks, a seemingly straightforward solution to the low accuracy of the CMOS S&H circuit in Figure 2 is to create a

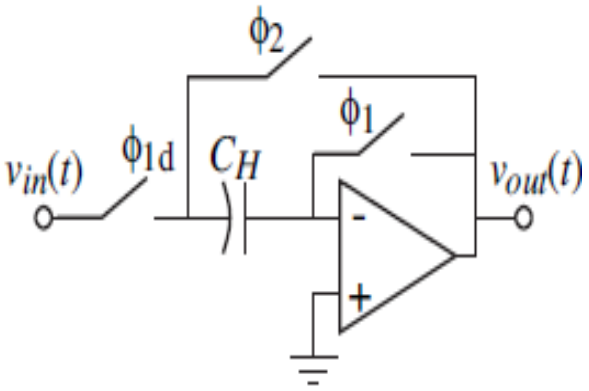


Fig.2 Closed loop S & H based on SC

- More accurate as compare to open-loop sample and hold circuit
- Signal-dependent feed through eliminated by a delayed clock
- Differential circuit keeps the output of the op amps constant during the Ø1 phase avoiding slew rate limits.

negative feedback path by connecting the output of A_2 to the negative input terminal of A_1. However, this modification does not really remove harmonic distortions since the voltages on both sides of M_1 still depend on the input signal. Moreover, the slew rate requirement for the input buffer A1 becomes rather stringent, because its output voltage level has to change significantly from one phase to the next. These problems can be alleviated by using the closed-loop S&H architecture. As shown, the op-amp G_2 creates a virtual ground in the loop, and the holding capacitor C_h is connected between this virtual ground and V_{out}. Once M_1 is turned off and M_2 is connected to ground, the channel charge of M_1 is distributed toward both directions: the charge to the left is grounded via M_2, while the one to the right is absorbed by the virtual ground. Thus, the majority of input dependent charge injection errors from M_1 are effectively neutralized. Also, the output node of G_1 is connected to the virtual ground via M_1 during the sampling mode ($\Phi_1 \rightarrow 1$), whereas it is grounded via M_2 during the holding mode ($\Phi_2 \rightarrow 1$). As a result, the time required for G_1 to slew from the holding to sampling mode (and vice versa) is reduced. The output voltage level of G_2 is also kept within a small range of its nominal value by the inner loop consisting of C_h and G_2.

V. SIMULATIONS AND RESULT ANALYSIS

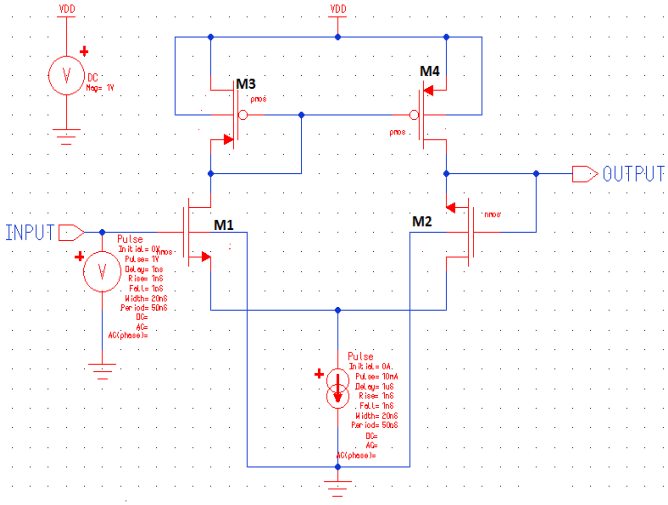


Fig.3 Schematic of Single stage unity gain op-amp

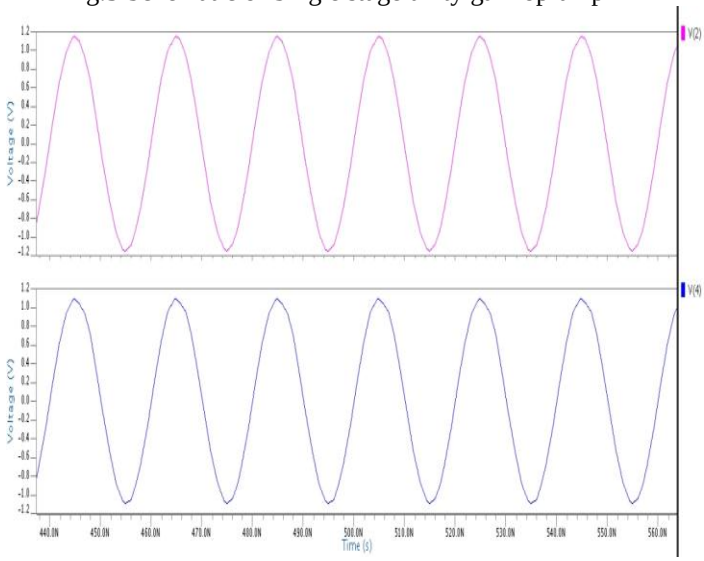


Fig.4 Output waveform of open loop unity gain op-amp

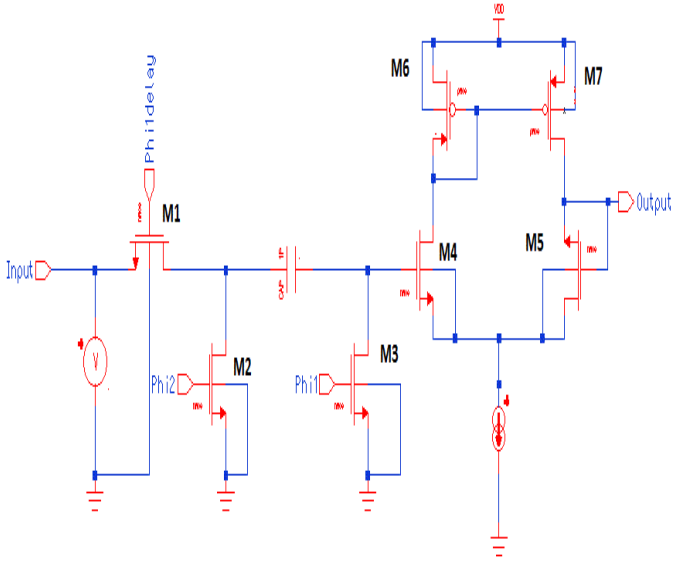


Fig.5 Schematic of Open loop S & H based on SC

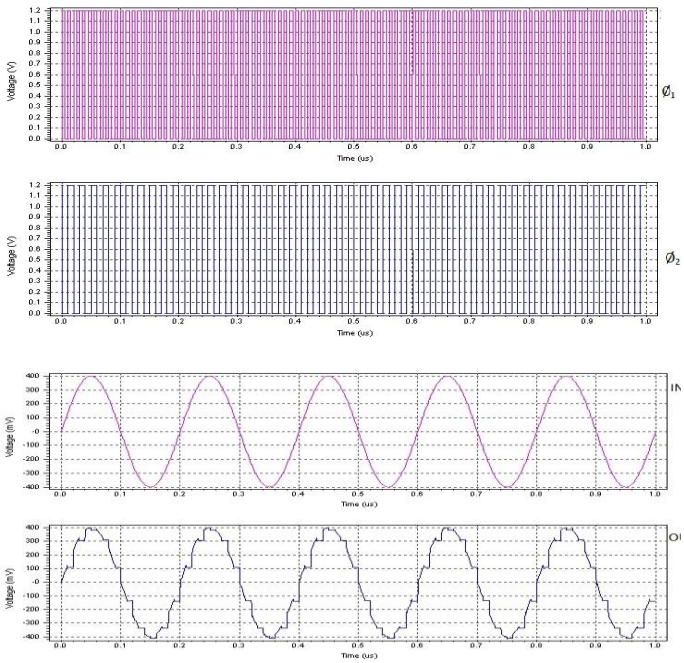


Fig.6 Output waveform of open loop S & H based on SC

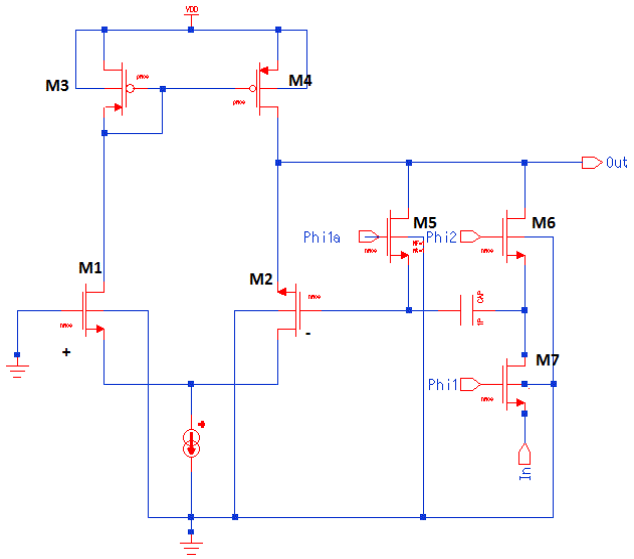
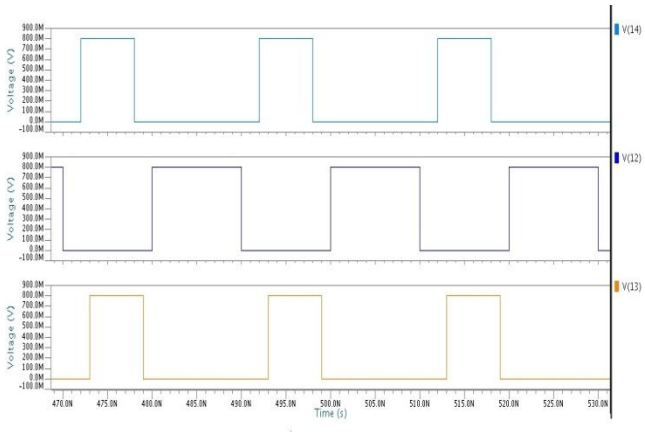


Fig.7 Closed loop S & H based on SC



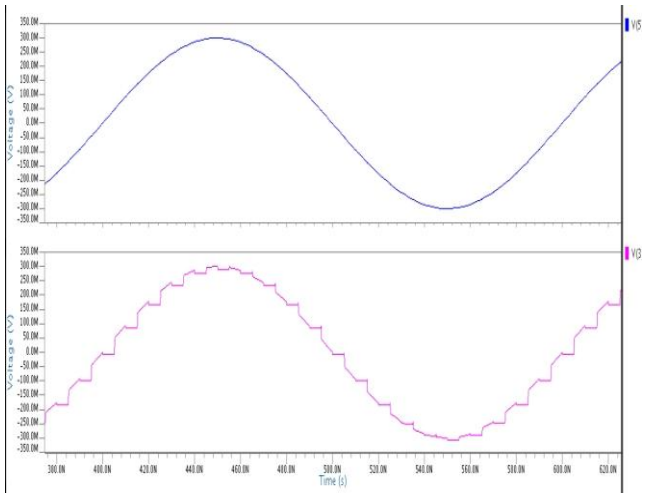


Fig.8 Output waveform of closed loop S & H based on SC

VI. COMPARATIVE RESULT ANALYSIS

Technology (nm)	Power Supply (V)	Propagation Delay (Ns)
90nm	0.9V	10.212 Ns
180nm	1.2V	10.232 Ns
350nm	1.8V	10.655 Ns

VII. ACKNOWLEDGMENT

I take this opportunity to express my profound gratitude and deep regards to my guide **Prof. Mehul L Patel** (Head of Electronics & Communication Department, **LCIT,Bhandu**) for his exemplary guidance, monitoring and constant encouragement throughout the course of this Dissertation. The blessing, help and guidance given by him time to time shall carry me a long way in the journey of life on which I am about to embark. His willingness to give his time so generously has been very much appreciated.

I am thankful to all the classmates for the valuable information provided by them. I am grateful for their cooperation during the period of my **M.E** Course.

REFERENCES

[1] Liang Dai and Ramesh Harjani, "CMOS Switched Op-Amp Based Sample-and-Hold Circuit" IEEE Journal of Solid-State Circuits, VOL.35, NO. 1, January 2000

[2] Mansi Patel, Mehul Patel, Nirali Shah, " A Review of Switched Capacitor Circuit (SC)" International Journal of Scientific Research, ISSN No-2277-8179,2012

[3] M.Rashtian, O.Hashemipour, K.Navi, "A Voltage-Mode Sample-and-Hold Circuit Based on the Switched Op-Amp Techniques" World Applied Science Journal (4), IDOSI Publications, 2008

[4] Ronak Trivedi, "Low-Power High-Speed Sample and Hold Circuit" IEEE International Conference Midwest Symposium on circuits and systems,

VOL.1,pp.453-456, August 2006
[5] Francesco Centurelli, Andrea Simonetti, Alessandro Trifiletti, "Near-Optimum Switched Capacitor Sample-and-Hold Circuit" IEEE NORCHIP Conference,pp.16-17, November 2009
[6] Francesco Centurelli, Andrea Simonetti, Alessandro Trifiletti, "Switched Capacitor Sample-and-Hold Circuit with Input Signal Range beyond Supply Voltage" IEEE NORCHIP Conference,pp.75-78, November 2008
[7] Christian Jesus B. FAYOMI, Gordon W. ROBERTS, Mohamad SAWAN, "Low-Voltage CMOS Analog Switch for High Precision Sample-and-Hold Circuit" Midwest Symposium on Circuits and Systems, VOL.2, pp.710-713 August 2000
[8] Andrei Danchiv, Mircea Bodea, Ana-Maria Luca, Ioan-Alexandru Tranca, "Charge Injection Induced Sample and Hold Error Analysis" IEEE Semiconductor Conference VOL.2, October 2009
[9] R. Jacob Baker, Harry W. Li, David E. Boyce, "CMOS Circuit Design, Layout and Simulation," IEEE Press Series on Microelectronic Systems, pp. 713-752,1997
[10] Phillip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design," Oxford University Press, Second Edition, pp. 492-600,2002
[11] Behzad Razavi, "Design of Analog CMOS Integrated Circuit," McGraw Hill Publication,pp. 405-447,2001
[12] Mingliang Liu, "Demystifying Switched-Capacitor Circuits," Newnes Elvister, pp.27-39,2006
[13] Joyce Cheuk Wai Wong, "CMOS Sample-and- Hold Circuits", Department of Electrical and Computer Engineering, University of Toronto, November 12, 2001.
[14] Haitao Wang, Hui Hong, Lingling Sun, and Zhiping Yu, "A sample-and-hold circuit for 1O-bit 1OOMS/s Pipelined ADC" , Key Laboratory for RF Circuits and Systems of Ministry of Education Hangzhou Dianzi University, Hangzhou 310037, China, IEEE 2011
[15] O. Hashemipour, and S. G. Nabavi, "A 1.5V,100MS/s,12-bit Current-Mode CMOS Sample-and-Hold Circuit" , International Journal of Engineering and Applied Sciences 3:2 2007
[16] Richard Schreier, Trevor Caldwell, "Switched Capacitor Circuits", ECE1371 Advanced Analog Circuits Lecture 7
[17] Insoo Kim, Kyusun Choi, "Sample & Hold Circuits" , Department of Computer Science & Engineering the Pennsylvania State University CSE 577 Spring 2011
[18] Behzad Razavi, "Design of Sample-and Hold Amplifiers for High-Speed Low-Voltage A/D Converters", Integrated circuits and systems laboratory, IEEE 1997
[19] Leonard Forbes, Harish Gopalakrishnan, and Weetit Wanalertlak, "Simulation And Analysis Of Noise In Switched Capacitor Amplifier Circuits, School of Electrical Engineering and Computer Science, IEEE 2005
[20] Takafumi Nasu, Kiyomichi Araki, "Noise Analysis of Switched Capacitor Networks in Direct Sampling Mixers", Graduate School of Engineering, Tokyo Institute of Technology, IEEE 2007

