International Journal For Technological Research In Engineering
Volume 1, Issue 11, July-2014 *ISSN (Online): 2347 - 4718*

CONCEPT AND DIGITAL MODELING OF POWER SWITCHED CAPACITOR FOR SMART GRID APPLICATIONS

Patel Dhaval B[1], Patel Hardik Kumar B[2], Patel Mihir[3]
[1,2]Lecturer, B.E Electrical, Swaminarayan College of Engineering, Saij, Kalol
[3]PG Scholar, MEC, Basna

Abstract: The electric utility industry and consumers of electrical energy are facing new challenges for cutting the electric energy cost, improving energy utilization, enhancing electric energy efficiency, improving supply waveform power quality, reducing safety hazards to personnel and protecting electronic sensitive computer and automatic data processing networks. The growing use of nonlinear type electric loads causes a real challenge to power quality for electric utilities. The deregulated electricity market where: competition, supply quality, security and reliability are now key issues for any economic survival. Electrical power network pollution is characterized by the nonlinear electric load ability to distortion modify and change the voltage and current wave form Root Mean Square (RMS) due to its inherent nonlinearity. All these devices will cause harmonic currents to flow and some devices, actually, directly produce voltage harmonics. Any ac current flow through any circuit at any frequency will produce a voltage drop at that same frequency. Harmonic currents, which are produced by power electronic loads, will produce voltage drops in the power supply impedance at those same harmonic frequencies.

I. INTODUCTION

The electric utility industry and consumers of electrical energy are facing new challenges for cutting the electric energy cost, improving energy utilization, enhancing electric energy efficiency & demand-side management, improving supply waveform power quality, reducing any safety hazards to personnel and protecting electronic sensitive computer and automatic data processing networks. All nonlinear electric loads fall in either one of two general categories, namely the arc (inrushhaturation) type and converter switching type power electronic switching. The proposed switched capacitor scheme can he used for single phase or 3 phase4 wires “Y” connected low voltage utilization computerized network in the range of (1KVA - 150 KVA). The reduction in quasi-steady harmonics and supply waveform power quality improvement has the added safety benefit of securing the computerized network against damage, data loss and other personnel-shock safety related issues related to hot neutrals and ground potential rise (GPR), and loop circulating neutral ground return currents. The growing use of nonlinear type electric loads causes a real challenge to any power quality and harmonic mitigation for Electric Utilities around the world, especially in the existing era of unregulated electricity market where: competition, supply quality, security and reliability are now key issues for any economic survival. Network pollution is characterized by the nonlinear electric load ability to distortimodify and changes the voltage and current waveforms due to its inherent nonlinearity. These nonlinear-type loads include fluorescent lighting, computers, adjustable speed drives, heating and lighting controls, industrial rectifiers, UPS (unintermptible power supplies), arc-welders and other process industry loads. These problems are more severe and challenging in the distribution utility networks, with industrial type loads. Nonlinear loads are sources of dynamic and quasistatic type harmonics, of integral, sub- and super hanmnic content. Other non-integer modulating type peculiar frequency signals: are introduced by load temporal nonlinearities. Their peculiar frequencies are generated by periodic and cyclical load variations along with the nonlinearity in the load. The nonlinearity is either analog or of the switching-type. Voltage drop calculations, reactive power compensation and power factor correction become &icky and complex issues in the presence of these non-common, non-sinusoidal feeder voltage and current waveforms. The use of distribution capacitor banks alone or as part of a low pass tuned arm, C-type, or a high pass damped type filter may not be either adequate or effective in providing the required reactive- compensation, voltage stabilization or targeted power factor correction level. This is caused by the generated uncommon' voltage and current harmonics that require new definitions of residual and generated type currents. The validation results using the MATLAB/Simulink/ Power System Blockset (PSB) indicated the effectiveness and simplicity of this low cost (USCS) solution to harmonic reduction. Total voltage and current distortions (THD)v, (THD)i indices were utilized to select the (USCS) compensator parameters using an off-line performance criterion "J" based on (THD) magnitude of offending harmonic and RMS value of source current:

J= Minimum {a, (THD)i+ a2 (THD), + a3 (Is0tla / IS"W) + a 4 II"/ Where all a are specified weighting factors and II,I is any offending dominant low order neutral (triplen or odd) harmonic intensified by any near-parallel resonance condition on the utilization grid network.

II. SWITCHED CAPACITOR COMPENSATOR

The proposed FACTS SCC filter/compensation device is a low cost switched/modulated filter which comprises a series switched capacitor bank and two shunt fixed capacitor banks connected to the AC side of a three-arm uncontrolled rectifier. Two mode operations are defined for the proposed FACTS device by two controlled switches, S1 and S2,

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installed on the DC and AC sides of the rectifier, respectively. These two switches follow NOT LOGIC command, that is, while S1 is on, S2 is off and vice versa. Switch S1 operation dictates on-off state of the series capacitor bank. On the other hand while S2 is on, SCC compensates reactive power like a shunt capacitor bank. Configuration of the proposed SCC is shown in Fig. 1.

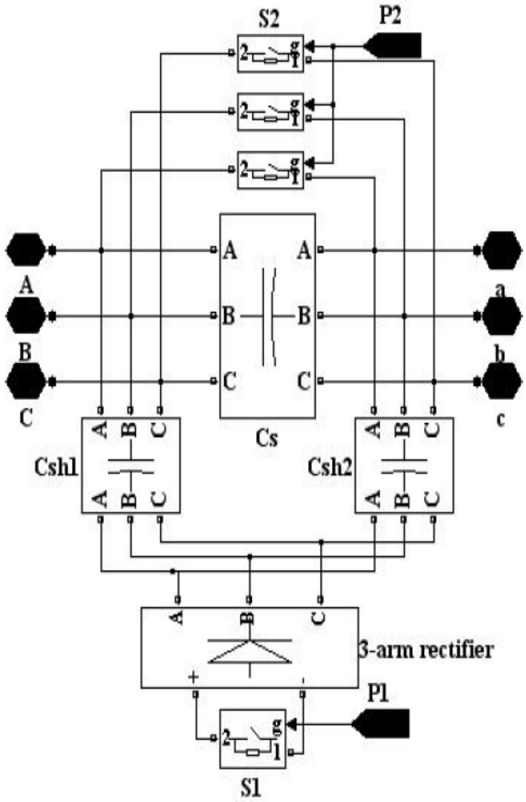

Fig.1 Proposed FACTS-Hybrid Series-Parallel SCC configuration

III. MULTI-LOOP DYNAMIC ERROR DRIVEN CONTROLLER

The multi-loop dynamic error driven decoupled and coordinated controller is a dual action controller to modulatetwo operating modes of the SCC. It comprises two main controller blocks which their outputs are indicated by e(A) and e(B) in Fig.2. The first controller block is a dynamic tracking regulator and includes three loops. The first loop is a voltage regulator that tracks reference voltage (Vg-ref). The second and third loops are dynamic tracking ones to stabilize current excursions and limit generator power excursions, respectively. The second controller block is a minimal ripple content regulator which minimizes ripple and sudden change contents caused by prime mover variations. This block does its responsibility by limiting the changes in Vg, Ig, and Pg loops. It is worthy to mention that the two blocks are time-decoupled weighted to ensure coordinated regulation action. The global output signal of the dynamic error driven controller is followed by a Weighted-Modified PID controller (WMPID) displayed in Fig. 3. WMPID includes an error sequential activation supplementary loop to ensure fast dynamic response and effective damping of large excursions, in addition to conventional PID structure. The output signal of the Weighted-Modified PID controller enters a PWM signal generator. On-off switching sequences produced by PWM define two operating modes of the FACTS device.

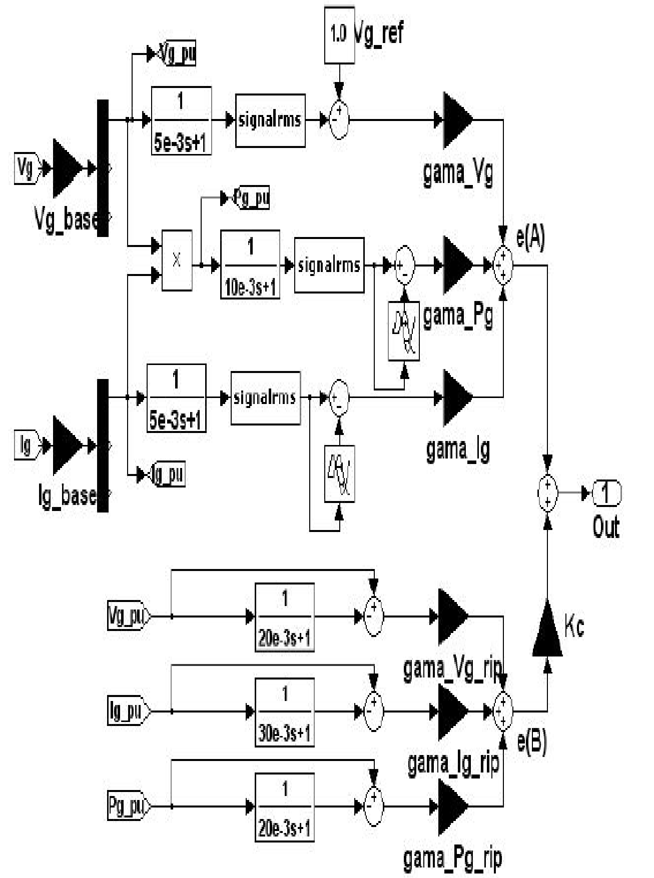

Fig. 2 Multi-loop dynamic error driven controller

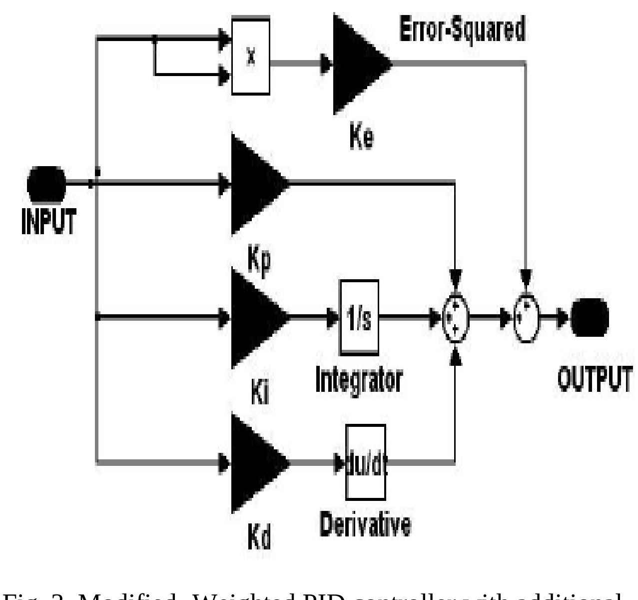

Fig. 3. Modified -Weighted PID controller with additional error squared compensating loop

IV. DIGITAL SIMULATION MODELS

Figure 4 depicts the single line diagram (SLD) of the utilization (single-phase) or (three-phase- 4-wire) feeder and the connection of the Unified Switched Capacitor Compensator (USCS) to the nonlinear temporal inrush /Arc type or SMPS-computer network loads.

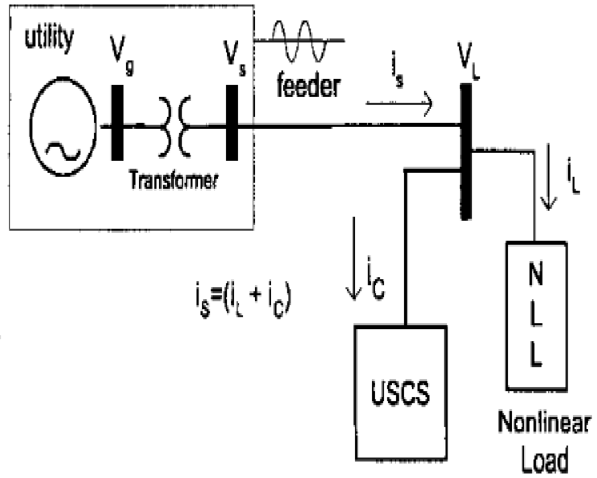

Fig 4 : SLD of the Utilization Feeder with the (USCS) Compensator at the nonlinear load bus

Figure 5 shows the proposed low voltage Unified Static Compensator (USCS) scheme. The USCS is a switched modulated capacitor bank using a pulse-width modulated (F'WM) strategy. The switching device uses either solid state switch (IGBT or GTO).

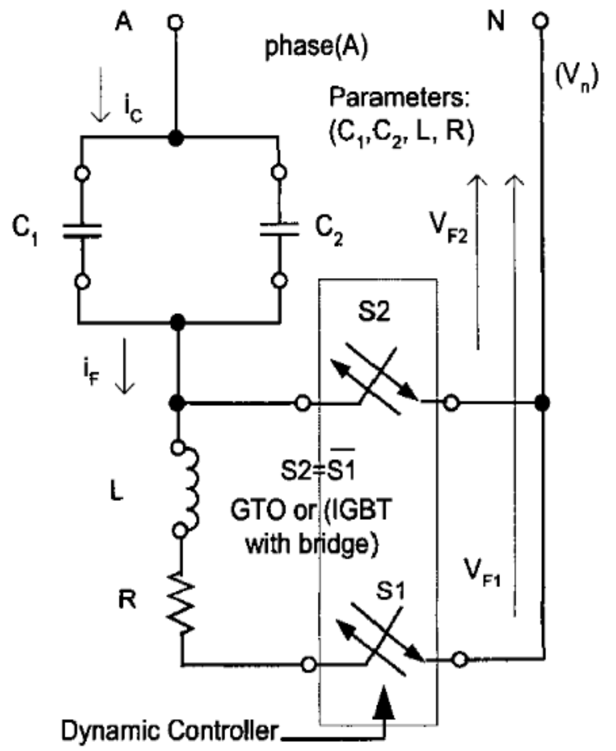

Fig 5: Low-Voltage Switchedhlodulated Static Comuensator

Figure 6 shows the proposed dual-loop dynamic tracking controller to ensure both objectives of (energy/power) saving as well as power quality enhancement of the supply system current and load bus voltage.

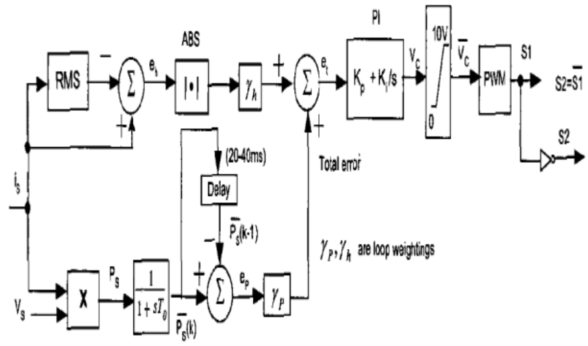

Fig 6: Dual-Loop Dynamic-Combined (Power and Ripple) Controller

V. DIGITAL SIMULATION RESULTS

To verify the dynamic effectiveness of the introduced SCC according to the goal of the purpose, operation of an AC grid (Fig.7) feeding three types of industrial loads (Fig.8) is investigated with and without SCC under different conditions that are normal and load excursion.

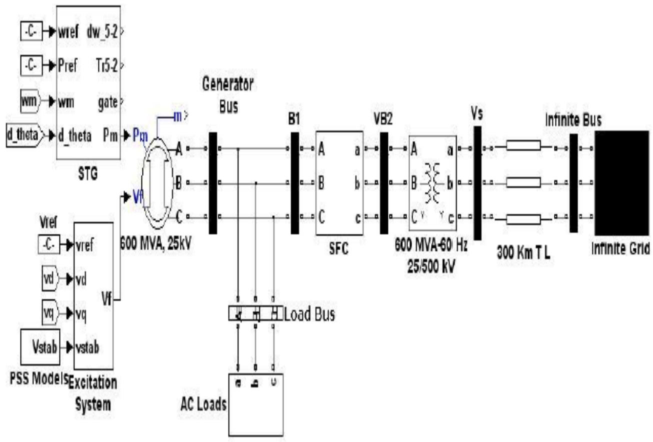

Fig. 7. AC grid as the case study

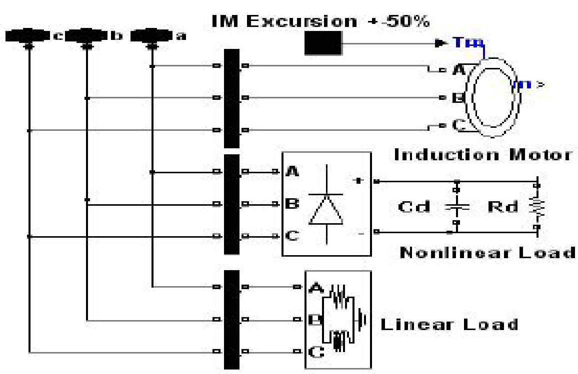

Fig. 8. Loads feed by AC Smart Grid

VI. CONCLUSION

This paper presents a novel low cost FACTS based switched filter compensation scheme for smart grid applications. The low-cost FACTS device developed by the First Author is effective in voltage stabilization, power factor correction at key AC buses, improving power quality, and limiting inrush current conditions. A decoupled coordinated multi-regulator, multi-loop dynamic controller is utilized to adjust the pulse width modulation switching patterns for the two solid state complementary switches to ensure fast bus voltage stabilization and power factor correction. The same FACTS device and dynamic control scheme, is now being extended for hybrid renewable Wind/Micro hydro green energy systems for robust interfacing to smart AC Grid. The FACTS filter/compensator was validated using the MATLAB-Simulink software. The digital simulation results validate the fast response and effectiveness of the proposed fast acting FACTS scheme in improving voltage regulation, limiting inrush current conditions, and modifying power factor.

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