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DESIGN AND IMPLEMENTATION OF DC-DC CONVERTER WITH ZVS AND ZCS FOR VARIOUS INTERACTING LOADS

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Abstract: ***The design and implementation of DC-DC converter which includes both high power digitally controlled bridge inverters to operate in full bridge power stage using different control method. It will operate upto nominal of minimum range of duty cycle for achieving Zero Voltage Switching (ZVS) and Zero Current switching (ZCS) in various interacting loads like R, L, C and motoring loads. This converter also functions under PWM mode for increased output regulation range. Here the efficiency can be increased by keeping one set of bridge inverter in OFF state for light loads. Due to this action the converter achieves no circulating current, reactive power and minimum semiconductor device stress. This circuit is more suitable for AC-DC power supply that pre-regulates intermediate DC bus. The main objective of this paper is to attain a high-efficiency dc–dc converter with wide-range ZVS & ZCS with efficiency improvement at both heavy and light loads. . A 1-kW 385–48 V converter designed to validate the concept achieved both 96+% efficiency and high power density. The overall system is designed, developed and validated by using SIMULINK.***

Index Terms: Dual half-bridge, full bridge, phase-shifted, zero voltage switching (ZVS).

I. INTRODUCTION

ONE of the most popular topologies for high-power and high-density switching converter designs is a phaseshifted full-bridge dc–dc converter (see Fig. 1). Favored because of its capability for zero-voltage switching (ZVS) operation, which minimizes switching losses, this converter configuration is described in detail in Texas Instruments application note U-136A [1]. However, a large circulating current in this topology causes significant conduction loss at heavy loads, while at light loads, the circulating current becomes too little for switches to achieve ZVS. Both characteristics impact the ability to achieve maximum efficiency. Reducing circulating current and extending soft switching over a wider load range are two key areas to improve a phase-shifted full-bridge converter's performance. To extend the soft-switching range and reduce switching loss at light loads, a resonant inductor is usually added to the converter's primary side. The inductor stores extra energy to extend the soft-switching range and reduce the reverse-recovery current of the secondary-side rectifier diodes. However, this extra energy can also cause a higher voltage spike across the rectifier diodes. A simple but effective clamping circuit can be used to mitigate this problem [2]. The clamping circuit substantially minimizes the converter's voltage ringing on both the primary and secondary sides and captures most of the transient energy on the primary side, which is utilized for soft switching and recycled back to the converter's dc input. For low output-voltage applications, such as 48 V or below, synchronous MOSFETs (SyncFETs) are often used to replace secondary rectifier diodes to minimize conduction loss. If the SyncFETs remain active, a converter can maintain continuous conduction mode (CCM) operation and a relatively stable duty cycle. Depending on the load, the converter's output-inductor current can be positive, zero, or negative at the end of a switching cycle. Both positive and negative currents actually help the primary switches to achieve soft switching [17]. At a certain load point, the output inductor current returns to zero at the end of each switching cycle. For this case, the primary can only rely on its magnetizing current for soft switching. Properly sizing magnetizing inductance and keeping SyncFETs active are good ways to achieve ZVS over a wide load range. At a very light load (especially at zero load), however, the negative current may become so significant that too much energy is cycled back to the primary side, resulting in efficiency loss. It becomes more challenging to extend the ZVS range when the output-rectification devices are diodes. Many circuits have been proposed to solve this problem. The circuits can be categorized into two types: the first type is an active switch-controlled resonant network [4]. Its auxiliary switch(es) can be usually turned ON at zero current. It activates a resonance to create a zero-voltage condition for the main switches to turn ON. The second type is a passive LC network connecting to the bridge switches [5]–[8], [10]. The network produces a loadindependent resonant current that helps the bridge switches achieve ZVS over a wider load range. These circuits do indeed increase the ZVS load range, but adding costly and bulky power components would become an issue for a cost-sensitive and space-constrained design. A load-dependent circulating current is one of the major drawbacks of the existing ZVS full-bridge dc–dc converters. The circulating

current passes through most of the converter's power train during the 1 − D period, while no energy is transmitted from the primary side to the secondary side. This causes a substantial power loss. Some resonant networks have been introduced to eliminate the circulating current [9]. However, the resonant network also removes the necessary circulating energy, which is needed for ZVS. These types of circuits would work well for low-frequency applications where low parasiticcapacitance devices, such as insulated-gate bipolar transistors, are often used. Another way to eliminate the circulating current is to use asymmetrical control [11]. An asymmetrical-bridge dc–dc converter does not have a circulating current but it is able to operate in ZVS mode. The circuit is quite simple and works well with a decent efficiency. It is generally suitable for applications.

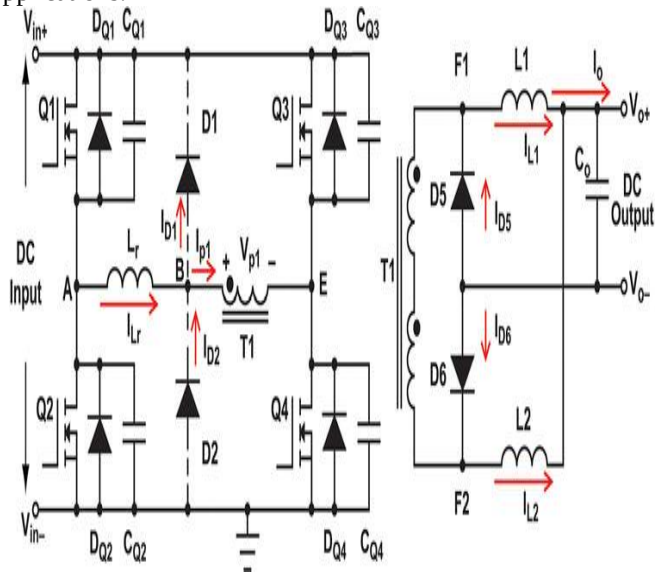

Fig. 1. Phase-shifted full-bridge dc–dc converter.

where the dc input and output voltage-variation range is narrow and loop bandwidth is low. Because its primary current passes through the bridge capacitor(s), the capacitance value needs to be relatively large. A large capacitance slows down voltage tracking to pulsewidth modulated (PWM) duty-cycle variation, while a large step load can easily cause power-transformer saturation. Not many applications based on this control have been seen recently. Most resonant converters [16], [18], [19], [21], [22] are able to utilize lagging resonant current to achieve ZVS and operate efficiently under certain conditions. While creating a ZVS condition, the lagging current unfortunately causes reactive power as well. The reactive power is processed by the power stage, but it is not delivered to the output. Too much reactive power can lead to efficiency loss. In the past few years, a 96% ac–dc telecom rectifier product inspired a wave of research and development of *LLC* converters [12]. It has been seeing that more and more server and telecom subkilowatt power supply designs started to adopt this topology lately.

II. TOPOLOGY AND CONTROL OF A DUAL HALF-BRIDGE DC–DC CONVERTER

Modified open-loop half-bridge bus converter can have a configuration like that shown in Fig 2. Its output is a current-doubler filter and its power transformer's secondary center tap is connected to power ground. When the primary switches, Q_1 and Q_2, operate complementally at a 50% switching duty cycle, the inverter outputs a symmetrical square voltage waveform. Because the secondary winding of the inverter's transformer is center tapped, it can be viewed as two interleaved forward-converter outputs—connected in parallel but with a 180º phase offset between the two outputs. This allows the current-doubler filter to fully cancel its output current ripple such that both the power transformer and the output inductors operate in an optimal 50% duty-cycle condition. With transformer design techniques that consider magnetizing inductance and proper-dead time control for the bridge primary switch, the primary switch's parasitic capacitance can be fully discharged by the transformer's leakage inductive energy before the switches are turned on. With such control, the converter can maintain ZVS over a wide load range. This open-loop bus converter is one of few topologies that can achieve both high efficiency and power density.

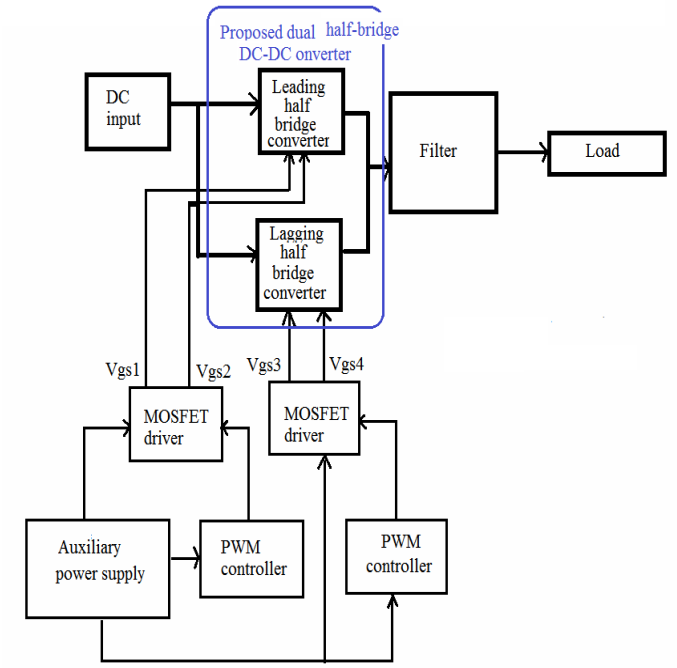

Fig 2 Block diagram of a dual half-bridge dc–dc converter.

The circuit shown in Fig. 3 has two half-bridge inverters; however, under phase-shift control, one will provide a leading phase while the other supplies a lagging phase. They will be identified as such, where the action of the leading half bridge initiates each output pulse and the lagging half bridge terminates it. A resonant inductor (L_r) and two clamping diodes

(D_1 and D_2) are added to the leading inverter to perform the same function as in a conventional phase-shifted full bridge. The inductor stores extra energy to extend the soft-switching range and reduce the reverse recovery current of the secondary-side rectifier diodes, while the clamping circuit minimizes converter voltage ringing on both the primary and secondary sides of the transformer. The two inverters can vary their phase offset from zero to 180°. When the phase offset is zero degrees, (the inverters are in phase) the two inverters operate in parallel, which works in the exact same way as a modified open-loop bus converter. At this operating point, the converter's duty cycle is 0.5 (50%). When the phase offset is 180°, the two inverters still output two square voltage waveforms, but since they are now out of phase, they superimpose on the current-doubler filter input nodes (F_1 and F_2), making the converter's duty-cycle effectively 1.0 (100%) and the output current very close to DC.

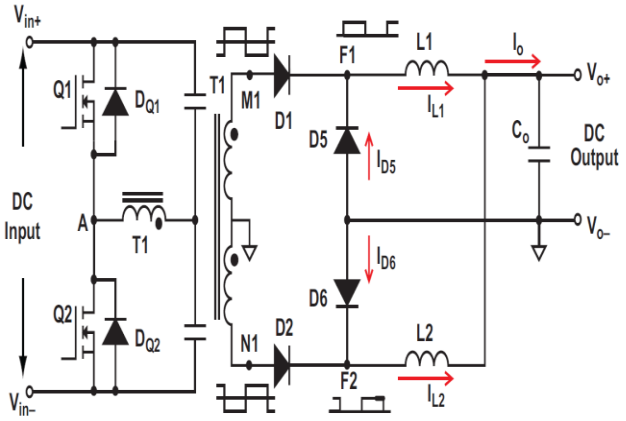

Fig. 3. Modified open-loop half-bridge bus converter.

Modified open-loop half-bridge bus converter can have a configuration like that shown in Fig.3. Its output is a current-doubler filter and its power transformer's secondary center tap is connected to power ground. When the primary switches, Q_1 and Q_2, operate complementally at a 50% switching duty cycle, the inverter outputs a symmetrical square voltage waveform. Because the secondary winding of the inverter's transformer is center tapped, it can be viewed as two interleaved forward-converter outputs—connected in parallel but with a 180º phase offset between the two outputs. This allows the current-doubler filter to fully cancel its output current ripple such that both the power transformer and the output inductors operate in an optimal 50% duty-cycle condition. With transformer design techniques that consider magnetizing inductance and proper-dead time control for the bridge primary switch, the primary switch's parasitic capacitance can be fully discharged by the transformer's leakage inductive energy before the switches are turned on. With such control, the converter can maintain ZVS over a wide load range. This open-loop bus converter is one of few topologies that can achieve both high efficiency and power density thick ground lead connects the motor case to the ground terminal of a switchboard via the cabinet frame of the power converter (rectifier and inverter) for safety. Note that the thick ground lead is removed from Fig. 4 for the sake of simplicity.

III. MODES OF OPERATION

The converter's two half-bridge inverters always operate at a 50% switching duty cycle when the output voltage is regulated above half of its maximum input voltage. The magnetizing currents of the power transformers reach a constant and stable peak value at the end of each half switching cycle, assuming that there is no magnetic flux walking and that the circuit operates in continuous conduction mode (CCM). When one half-bridge's switch is turned off (and during the dead time before the complementary switch is turned on), the magnetizing current and reflected-output current fast charge and discharge the switching devices' parasitic capacitance until the voltage across the power transformer windings decreases to zero. Both leading and lagging inverters work in the same way in this first part of the commutation period. After that, the lagging inverter continues its commutation by utilizing its magnetizing energy (since its transformer secondary is basically open), while the leading inverter relies on the energy of its power-transformer leakage inductance and resonant inductor to activate a resonation between the inductance and the switches' parasitic capacitance. A transformer's properly sized magnetizing inductance can usually store enough energy for the lagging bridge to achieve ZVS regardless of the output load. Because magnetizing current only applies to the lagging bridge's parasitic capacitance, the voltage slew rate of the lagging-bridge's switching node becomes much softer during this commutation period compared with a conventional phase-shifted full-bridge converter. The operation process of the circuit can be divided into five time intervals beginning with t1, which is the end of the last cycle in the sequence.

1. MODE 1 $t_1 <= t < t_2$

During this period, switches Q_1 and Q_4 are on. The t_1 time is the moment when freewheel diode D_7 ends its reverse recovery. The reverse recovery current of diode D_7 is reflected to transformer T_1's primary. Most of its corresponding energy, residing in inductor L_r, is captured by clamping diode D_1. The rest of the energy residing in the primary- and secondary-side leakage inductance of T_1 cannot be captured by the clamping diode, and could cause some voltage ringing at node N_1. To minimize the voltage ringing, the leakage inductance of T_1 should be minimized. The captured current (I_{D1}) circulates within the loop formed by Q_1, L_r and D_1 and begins to decline due to the conduction loss of the loop. Half-bridge capacitors, C_1 and C_2, are connected to T_1 and T_2's primary windings, respectively. Their voltages are coupled to the secondaries and then applied to the output filter through the output rectifiers (D_3 and D6). Energy is transferred from the primary sides to the secondary sides during this time period, therefore the inductor

currents (I_{L1} and I_{L2}) are increasing. C_1 and C_2 equally divide the bus voltage. Since the two transformers' primary currents cancel each other when they pass through capacitors C_1 and C_2, the capacitor voltage ripple can be controlled to a small value, with relatively small capacitance. The capacitors' peak-to-peak ripple can be calculated by the following equation:

$$V_{C\_ripple} = \frac{(2D-1)(1-D)\times V_o}{4n\times D\times L_o\times C\times f_s^2} + \frac{(1-D)\times I_o}{2n\times C\times f_s}$$

Where D is the converter's duty cycle, C is the total capacitance of half-bridge capacitors C_1 and C_2, n is the transformer turns ratio, and f_s is the switching frequency. The capacitor ripple reaches its peak value at full power with a 0.5 converter duty cycle.

2. MODE 2 $t_2 <= t <= t_3$

At t_2, transistor Q_4 is turned off. After Q_4 is turned off, capacitor C_{Q4} is charged up almost linearly by the reflected L_2 current (I_{L2}). After its voltage surpasses C_2's voltage and transformer leakage energy is fully discharged, the voltage across transformer T_2 reverses its polarity and becomes positive. Freewheel diode D_8 conducts and takes over the I_{L2} current from D_6 such that D_6 becomes electrically disconnected. The leading bridge maintains its previous state and continues to apply a voltage to node F_1 through diode D_3, while both output rectifiers D_5 and D_6 of the lagging bridge remain open. During this period, capacitor C_{Q4} is continuously charged up by T_2's magnetizing current. The worst-case scenario is when the load is zero. The magnetizing inductance is the only current to charge C_{Q4} and discharge C_{Q3}. To achieve ZVS, the lagging bridge's switch dead time should meet the following requirement:

$$t_{d\_lagging} \geq 8f_s \times L_{T2} \times (C_{Q3} + C_{Q4})$$

Where f_s is switching frequency and L_{T2} is the magnetizing inductance of transformer T_2. The reverse recovery of rectifier D_6 could cause D_6 and D_8 to conduct at the same time and T_2's output is essentially shorted for a short period. The short circuit can lock magnetizing current inside T_2 and affect the dead time selection. Before Q_3 is turned on at t3, C_{Q4} is fully charged up and switching node E is clamped to the input DC source by Q_3's body diode (D_{Q3}). Note that C_{Q3} is fully discharged when C_{Q4} is charged up to the DC input voltage. Therefore, Q3 is turned on with zero voltage across it. When C_{Q4} is charged up to the DC input voltage, T_2's output voltage (V_{M2}) reaches the same level of T_1's output (V_{M1}). Output rectifier diode D_5 conducts softly and the leading and lagging inverters begin to share their output current, I_{L1}.

3. MODE 3 $t_3 <= t <= t_4$

During this period, the two inverters share their output current (I_{L1}). Because the two transformer outputs (V_{M1} and V_{M2}) have almost the same voltage, the current shifting from the leading half bridge to the lagging half bridge is usually slow. Therefore, the leading half bridge usually shares more output current than the lagging half bridge during this time period. In the meantime, freewheel diode D_8 maintains its previous state such that conducting currents I_{L1} and I_{L2} start to decrease as V_o applies to L_2 with reverse polarity. The decrease of I_{L2} and the increase of I_{L1} lead to a partial current-ripple cancellation, minimizing output ripple voltage.

4. MODE 4 $t_4 <= t < t_5$

At t_4, Q_1 is turned off. Parasitic capacitance C_{Q2} is discharged. Parasitic capacitance C_{Q1} is charged by the resonant inductor current (I_{Lr}) which includes T_1's magnetizing current, the reflected inductor current (I_{L1}) shared by the leading inverter and the captured reverse recovery current of freewheel diode D_7 in Mode 1. With the current sharing shifting from the leading inverter to the lagging inverter, I_{Lr} decreases. D_3 maintains conduction until I_{Lr} decreases to the magnetizing current value.

During this period, C_{Q2} can be completely discharged if the converter output current reaches a certain level and the resonant inductor (L_r) has sufficient energy stored. If the stored energy is not sufficient, D_3 turns off softly before C_{Q2} is completely discharged. The voltage across T_1 (V_{p1}) starts to decrease and eventually reverses its polarity. Output inductor current (I_{L2}) is still passing through D_8 for CCM, so T_1's secondary is essentially shorted by D_4 and D_8. Therefore, T1's magnetizing current (energy) cannot further contribute to the discharge of C_{Q2}. Resonant inductor Lr, however, can continue to resonate with C_{Q1} and C_{Q2} to fully discharge C_{Q2} if the resonant inductor's value meets the following criteria:

$$\mathbf{L_r = 16 \times fs \times L_{T1} \times (C_{Q1} + C_{Q2})}$$

Where L_{T1} is the magnetizing inductance of leading inverter transformer T1. By inserting a proper dead time ($t_4 - t_5$), Q_2 can be turned on at t_5 with a zero voltage across it. Here we assume that clamping diodes D_1 and D_2 have no turn-off delay. For optimal operation, the leading bridge dead time should be:

$$t_{d\_leading} = \arcsin\left(\frac{V_{bus} / (I_{Lr\_m} \times X_r)}{\omega_r}\right)$$

and

$$t_{d\_leading} \leq \frac{0.5\pi}{\omega_r},$$

where

$$\omega_r = \frac{1}{\sqrt{L_r \times (C_{Q1} + C_{Q2})}},$$

$$X_r = \sqrt{\frac{L_r}{C_{Q1} + C_{Q2}}},$$

I_{Lr_m} is resonant inductor (L_r) current when resonation just starts and V_{bus} is the maximum voltage switching node A can swing. If clamping diodes D_1 and D_2 have significant turn-off delay compared with the dead time, V_{bus} should use V_{in} for the calculation, otherwise V_{bus} should be $0.5 \times V_{in}$.

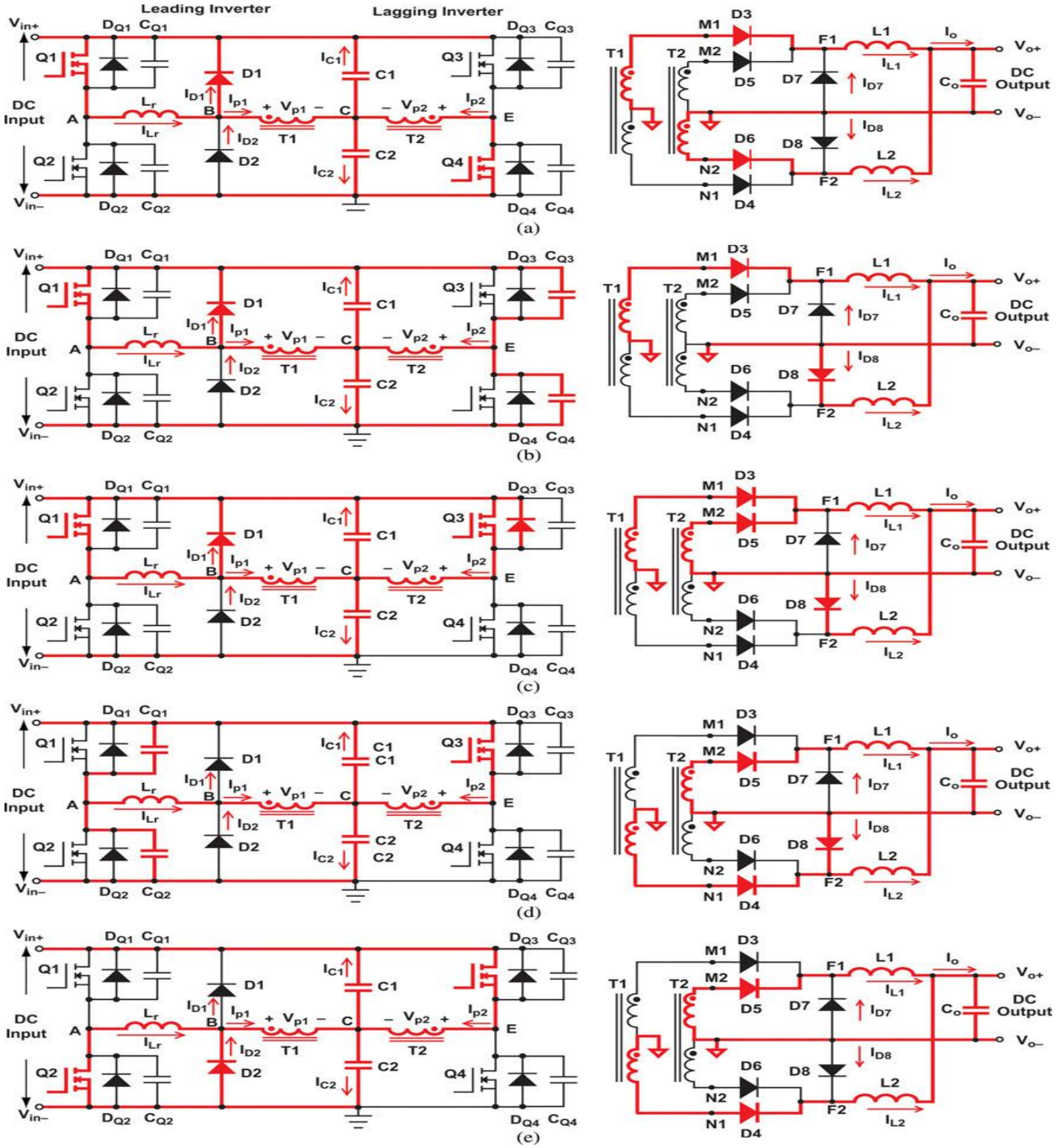

Fig 4 current paths of dual half bridge dc-dc converter in one cycle operation (a) MODE 1 t1 <= t < t2 (b) MODE 2 t2 <= t <=t3 (c) . MODE 3 t3 <= t <=t4 (d) MODE 4 t4 <= t < t5 (e) 5. MODE 5 t5<=t<t6

calculation, otherwise V_{bus} should be $0.5 \times V_{in}$. This calculation is a good starting point for dead timing best efficiency, the final dead time setting should be fine tuned p tuned per test results.

5. MODE 5 $t_5<=t<t_6$

After Q_2 is turned on at t_5, the inductor current (I_{Lr}) decreases to zero quickly and then begins to build up in the opposite direction. When its reflected current at the secondary surpasses output current (I_{L2}) and D_8's reverse-recovery current, D_8 stops conducting at t_6. Time t_6 is the end of one half-cycle. The process then repeats for the next half-cycle with the complementary components operational. Each complete switching cycle consists of two complimentary half-cycles.

IV PARAMETERS SPECIFICATIONS

The dual half-bridge converter has been simulated in Matlab/Simulink environment.

- Input Voltage (Vin) 400V
- Output Voltage(Vo) 48V
- Output Power(Po) 500W
- Switching Requency(fs) 20kHz

IV. SIMULATION MODEL AND RESULTS

A. SIMULATION MODEL FOR GENERATING PWM

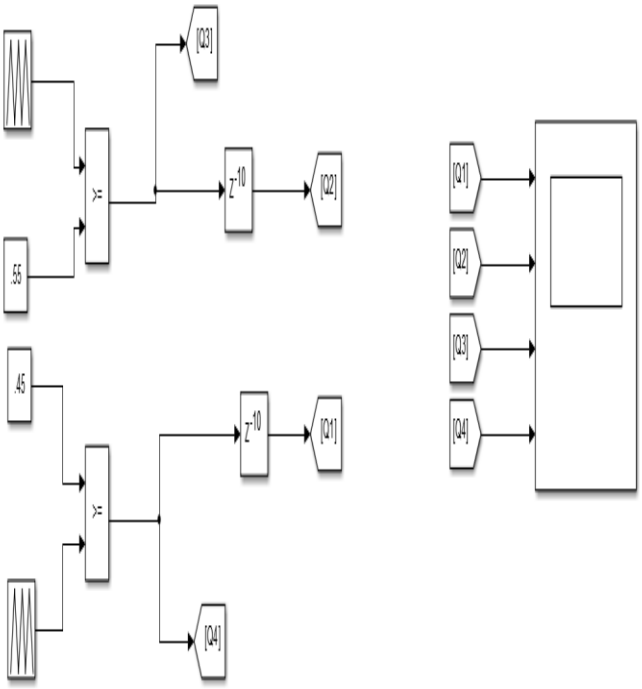

Fig. 5 Simulation model for generating PWM

Fig 5 shows the simulation model for generating PWM. This model shows the generating of pulses comparing the reference and carrier signals. Q4 is first turned on after a delay Q1 will be turned on. For generating pulses for Q3 carrier is higher than then the Q4. Q3 is turned on after a delay Q2 is turned.

B. FUNCTION BLOCK PARAMETERS FOR DELAY

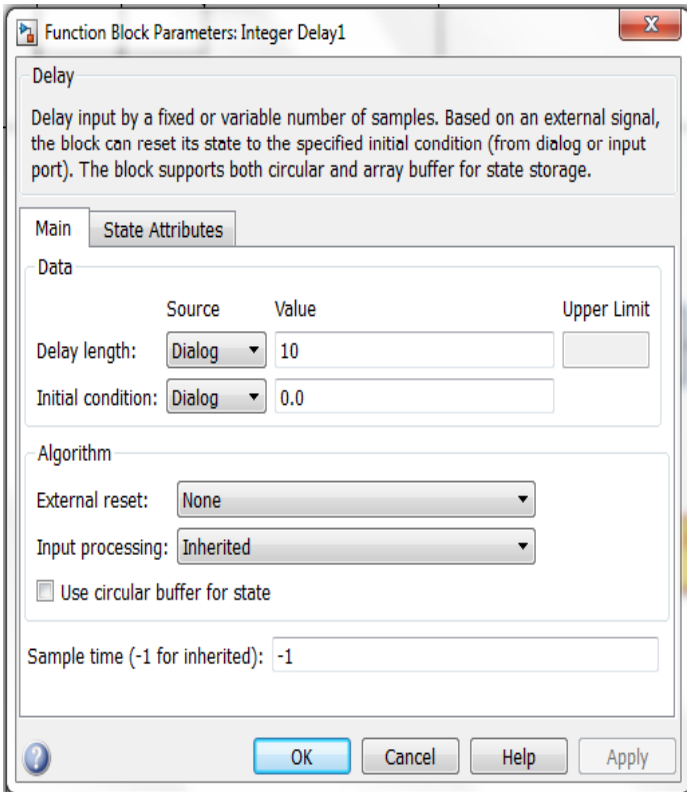

Fig 6. Function block parameters for delay

This block shows the integer delay, this will turning ON switch Q3 and Q1 after a delay. Fig 6 shows function block parameters of integer delay1.

C. SIMULATION OUTPUT FOR GATE TRIGGERING PULSE

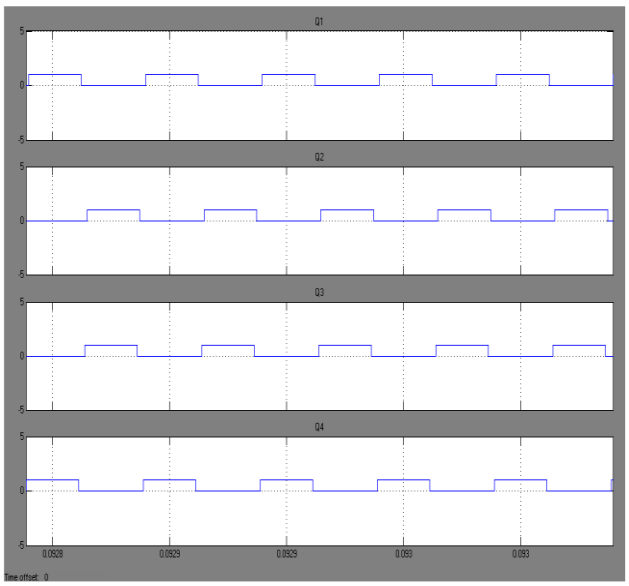

Fig 7 Gate triggering pulse of switch S1-S4 waveform

Fig 7 shows gate triggering pulse of switch S1-S4 waveform. A high frequency triangular carrier wave is compared with reference wave of the desired frequency. The intersection of carrier and reference waves has magnitude higher than the triangular wave then the comparator output is high otherwise it is low. The comparator output nis given as pulse to switch Q1, Q2, Q3 and Q4.

D. MAINSYSTEM SIMULATION MODEL FOR DUAL HALF-BRIDGE

The simulation Model shows the dual half-bridge converter in fig 10. An Dual Half -Bridge Converter uses two converter, leading and lagging half-bridge converter. It has isolated transformer with primary and secondary (acts as a step down transformer). Lagging bridge is turned to achieve ZVS and ZCS. Here 400V input is given and this system will buck the voltage and gives 48V DC output.

E. SCOPE FOR DRAIN VOLTAGE AND VOLTAGE AND CURRENT FOR TRANSFORMER

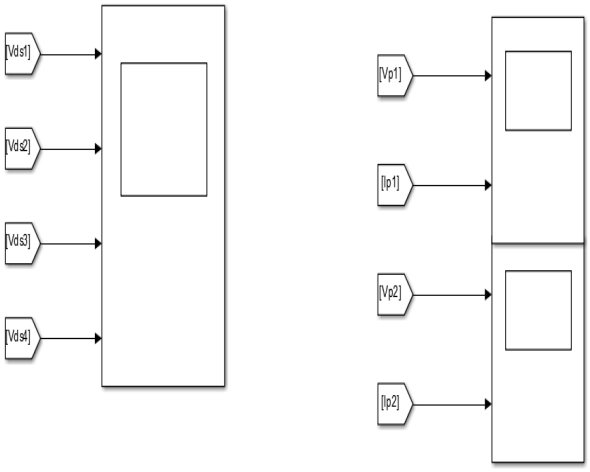

Fig 8 Scope for drain source, voltage and current

F. SIMULATION OUTPUT FOR DRAIN SOURCE AND VOLTAGE AND CURRENT FOR TRANSFORMER

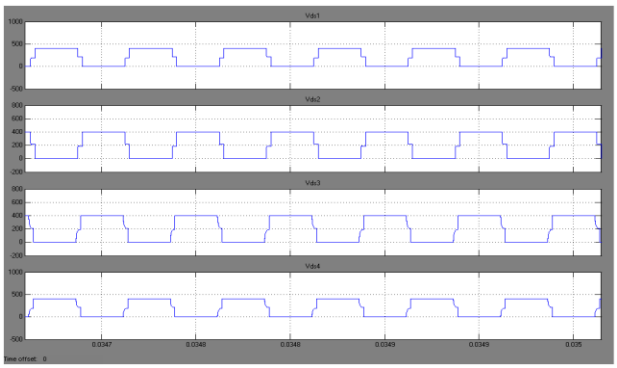

Fig.9 Waveform for voltage drain source for switches S1, S2, S3, S4

Fig 9 provides the efficiency data when the output rectification used diodes as well as SyncFETs. The curves show that the 48-V output circuit is able to achieve 95.2% maximum efficiency with diode-based output rectification, 96% maximum efficiency with a SyncFET rectification circuit, and 92% efficiency. The converter was switched to PWM mode and one halfbridge was actually turned OFF to prevent significant loss.

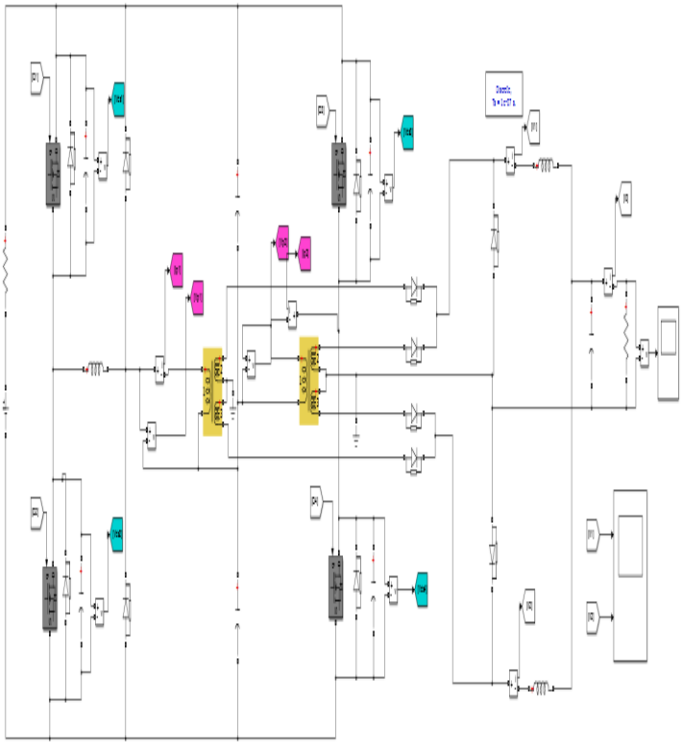

Fig.10 Mainsystem simulation model for dual half-bridge

G. WAVEFORM FOR TRANSFORMER-1 PRIMARY VOLTAGE AND CURRENT

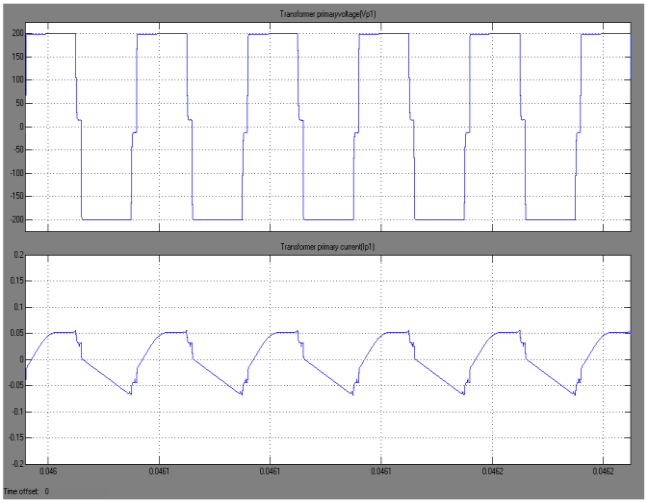

Fig 11 Transformer-1 primary voltage, current waveform

Fig 11 shows the transformer primary voltage and current experimental waveforms. Both the leading and lagging inverters operate in PWM mode. As shown Ip1 has some oscillation between the capacitance and the resonant inductor. The leading and lagging inverter operate in parrel. Either inverter can be turned off to save switching loss.

H. WAVEFORM FOR TRANSFORMER-2 PRIMARY VOLTAGE A ND CURRENT

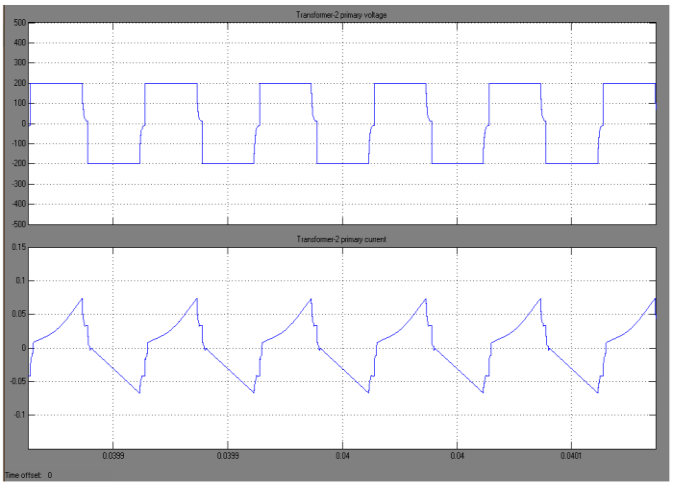

Fig 12 Transformer-2 primary voltage, current waveform

Fig 12 shows the transformer primary voltage and current experimental waveforms. Both the leading and lagging inverters operate in PWM mode. As shown Ip2 has some oscillation between the capacitance and the resonant inductor. The leading and lagging inverter operate in parrel. Either inverter can be turned off to save switching loss.

9. WAVEFORM FOR OUTPUT VOLTAGE

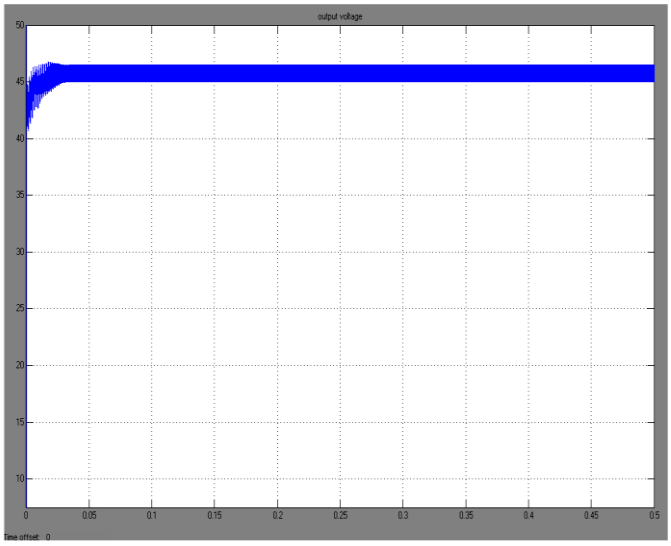

Fig 13 Output voltage waveform

The output DC voltage waveform of overall Dual Half-Bridge Converter is shown fig 13. The output voltage of 48V DC is obtained

V. PARAMETERS AND COMPONENTS

The circuit parameters and components used in this test were the following:

1) Primary power MOSFETs: SPW20N60CFD
2) Freewheel diodes: V20100
3) Output inductor: 34 μH
4) Magnetizing inductance: 625 μH
5) DC blocking capacitor: 2 × 0.22 μF
6) Secondary rectifier: FDP2532 (SyncFET) or V30200
7) Resonant inductor: 20 μH (at zero current)
8) Power transformer turns radio: 20:7:7
9) Half-bridge capacitors: 2 × 0.47 μF
10) Switching frequency: 100 kHz
11) Main controller: UCD3040 TI digital power controller.

VI. CONCLUSION

This paper deals with The test on the first prototype of the dual half-bridge converter built in the TI Digital Power lab has validated the new topology and control concept and demonstrated the high efficiency potential of this circuit. This topic explored a different approach to achieving the following goals: Loading dependent, wide-range ZVS with efficiency improvement at both heavy and light loads; no circulating current and reactive power; 100% time utilization for power transformation and optimal use of magnetic components; and minimum semiconductor device stress. These are the necessary design elements for a high power density and peak efficiency. The dual half-bridge topologies most suitable for AC/DC power-supply designs that have a pre-regulated input voltage for its DC/DC stage. It can also be used for DC/DC converter designs that have a relatively narrow voltage range for the input-voltage and regulated output. From a packaging point of view, this topology is also a good candidate for high-power, high-density and low-profile designs.

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