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A 2.4 GHZ CURRENT REUSE COMMON-GATE LNA USING VARIABLE CAPACITOR

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Abstract: This paper presents low power CMOS RF front-end LNA architecture, employing voltage controlled capacitor in input matching with inductive source degeneration topology and current reused technique. This LNA is designed for Bluetooth application that provide circuit performance at 2.4 GHz. we are using TSMC 0.18 µm CMOS for this architecture. From the simulation results, the fully integrated LNA exhibits a gain of 13.39 dB and a noise figure of 1.44 dB at 2.4 GHz, operated at a supply voltage of 1.5 V. The design process is simulated using Advance Design System (ADS).
Key words: Low noise amplifier, Low noise figure, Advance Design System.

I. INTRODUCTION

For the home user and commercial business 2.4 GHz is the primary band one uses for WiFi, Bluetooth, Cordless phone, printer, keyboard, mouse and gaming controller applications. Electronic devices using these technologies are continuously shrinking to provide portability and low power consumption to motivate renewable energy [4]. Manufacturers are interested to provide a number of wireless services in a small portable device by using system on chip (SOC) design and by integrating analog and digital blocks. The solution of all the above is CMOS RFIC (radio frequency integrated circuits)[2],[3].As receiver is concert the first and main part is LNA which technically plays a role of providing input matching, output matching with noise suppression, high amplification to degrade noise figure of upcoming blocks without degrading linearity and by using low power supply. Current reuse technique by using cascoded amplifiers is preferred in most of the LNA architectures to decrease power consumption. Here Author is using (CG-CS) topology to increase the bandwidth of operation with maintaining the noise figure nearly constant over a wide frequency range and this noise figure is lowest in compare to all studied LNA operating in this frequency range.

II. CIRCUIT TOPOLOGY

Low voltage LNA design's simulation and measured results were studied. Current reused two stage common source (CS-CS) topology was frequently used in these architectures to degrade power consumption. This topology provides sufficient gain with low power consumption, but the noise factor of the CS LNA is linear with the operating angular frequency and can be large in the GHz range with source inductive degeneration. Its output gate current noise increases with the increase in ω .while CG LNA noise factor is slightly higher as compared to CS LNA but it is almost independent of bandwidth and remains nearly constant in the required bandwidth. [5],[6].The CG stage provides noise figure that is almost independent of the frequency of operation .the common gate stage also eliminates the miller effect and hence provide better isolation from the output return signal. Fig.1 shows the proposed design of LNA using cascoded amplifiers ($M_1$and M_2). Input matching is provided by L_1 and a voltage variable capacitor which is also used to provide variable tuning. The drain of $M_1$is connected to the gate of $M_2$by a capacitor which provide low impedance path between drain of $M_1$and gate of M_2. Inductor L_3 is used to provide isolation between drain of M_1 and source of M_2.

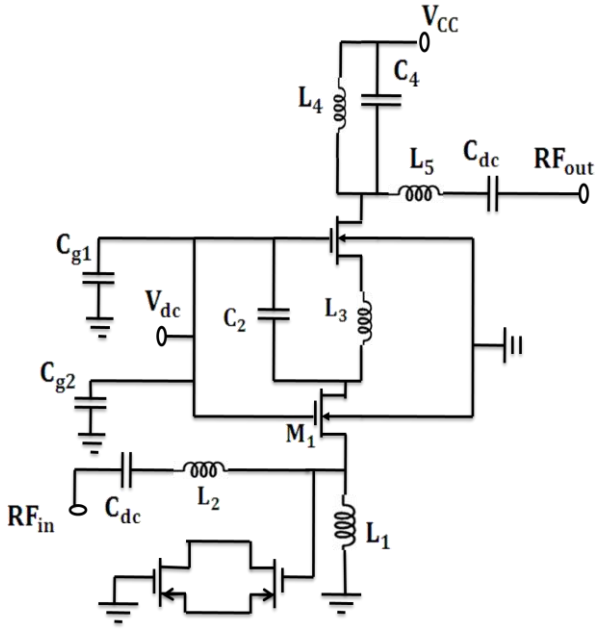
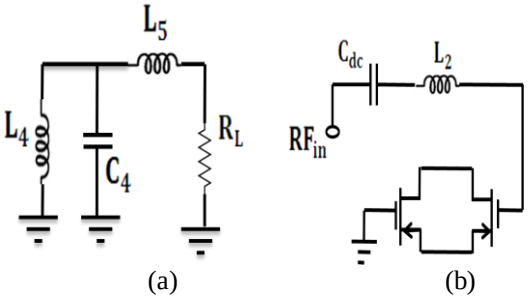


Fig. 1 Schematic of proposed LNA

As compared from previous LNA's we are using voltage variable capacitor to increase bandwidth.



(a) (b)

Fig.2 (a) Output matching (b) Input matching

$$Z_{in1} \approx j\omega L_s + \frac{1}{j\omega C_{gs}} + \frac{g_{m1}}{C_{gs}} L_s \quad (1)$$

Here ω is the operating frequecy and Z_{source} is defined as $z_{source} = R_{source} + j\omega L_{source}$ and they can be defined as

$$R_{source} = \frac{R_s \alpha + \omega^2 R_s C L_2}{\gamma} \quad (2)$$

$$L_{source} = \frac{\omega L_2 \alpha}{\gamma} - \frac{\omega R_s{}^2 C}{\gamma} \quad (3)$$

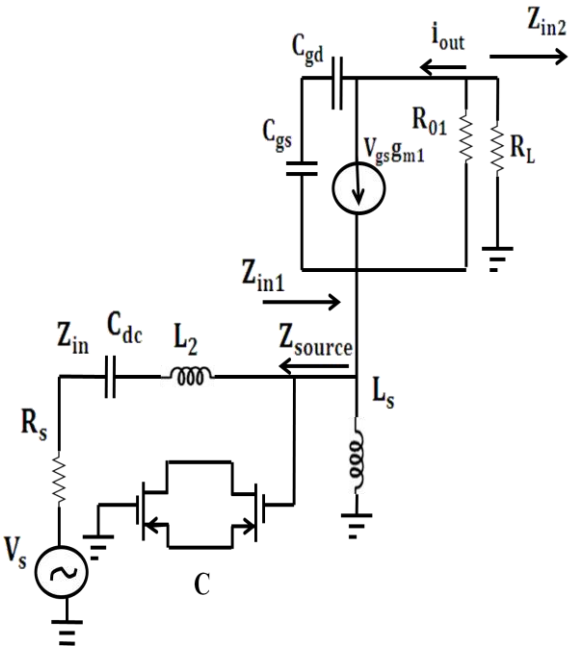


Fig. 3 Small signal model with input matching

Where α and γ are defined as

$\alpha = 1 - \omega^2 L_2 C$ and

$\gamma = (1 - \omega^2 L_2 C)^2 + (\omega R_s C)^2$

$$Z_{source} = Z^*in1 \quad (4)$$

by using eq. (4) we have

$$R_{source} = \frac{gm_1 L_s}{C_{gs}} \quad (5)$$

$$j\omega L_{source} = -j\omega L_s - \frac{1}{j\omega C_{gs}} \quad (6)$$

From real and imaginary part of Z_{in1} we obtained equation (5) and (6), the operating frequency ω can be derived as

$$\omega = \sqrt{\frac{1}{(L_{source} + L_s) C_{gs}}} \quad (7)$$

Simulation Results

The circuit simulations of the proposed design are completed in the environment of ADS (Advanced Design System). The simulation S-parameters are shown in Fig. 4(i)-4(iv). The maximal power gain S_{21} is 13.39 dB at 2.4 GHz, S_{11} is – 14.26 dB, S_{22} at -20.59 dB at 2.4 GHz. The noise figure reaches 1.44 dB at 2.4 GHz. The voltage supply is 1.5v. These simulation results show that the both input and output stage of the LNA achieve good matching, with a high gain and meanwhile the NF and power consumption are also very small, which satisfies the requirements of a RF circuit very well.

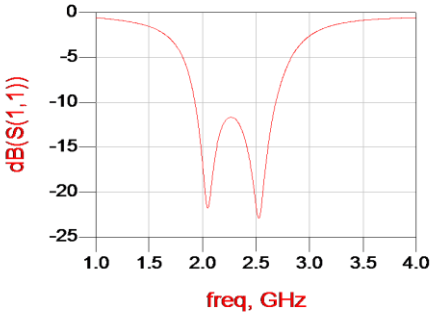


Fig. 4(i)

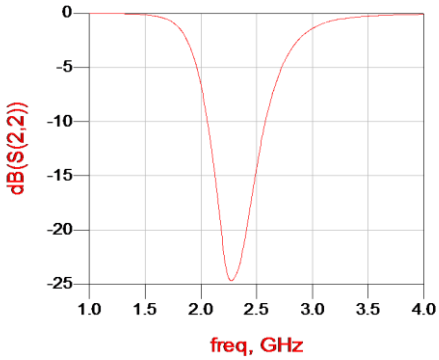


Fig. 4(ii)

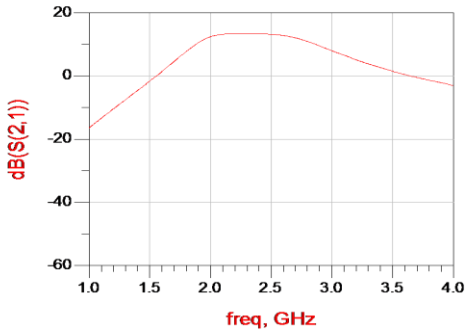


Fig.4(iii)

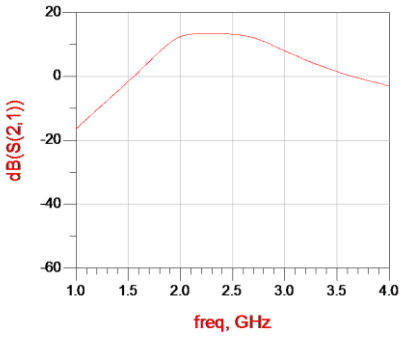


Fig.4(iii)

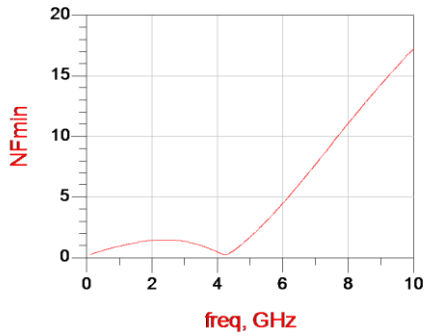


Fig.4(iv)

Reference	Gate length (μm)	Frequency (GHz)	S21 (dB)	S22 (dB)	S11 (dB)	NF (dB)
[1]	0.18	5.7	11.45	-17	-14	3.4
[6]	0.18	2.4	11.79	-12.47	-10.37	3.89
[8]	0.13	2.4	24	N.A.	-10.7	2.0
[14]	0.18	2.4	14.4	-12.7	-18.1	1.6
This work	0.18	2.4	13.39	-20.59	-14.26	1.44

III. CONCLUSION

A low-voltage CMOS Low Noise Amplifier (LNA) in a standard 0.18 µm CMOS technology is designed. To substantially reduce the DC power consumption, we present modified current-reused two-stage common gate common source architecture at 1.5 V power supply. This 2.4 GHz LNA has a simulation gain of 13.39 dB and noise fig. of 1.44 dB. Under this bias condition the S_{11} –14.26 dB. These simulation results show that the LNA has the best gain at frequency 2.4 GHz.

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