DESIGN AND IMPLEMENTATION OF DSP OPERATIONS USING VEDIC MATHEMATICS

Nadiya. K[1], V.Teju[2], K.Venkateswarlu[3]
[1]M. Tech, [2]Assoc. Professor, [3]Assoc Professor and HOD
Department of Electronics and Communication Engineering, Jawaharlal Nehru Institute of Technology,
Affiliated to JNTU-Hyderabad, India

ABSTRACT: Digital Signal Processing (DSP) operations are very important part of engineering as well as medical discipline. Designing of DSP operations have many approaches. For the designing of DSP operations, multiplication is play important role to perform signal processing operations such as Convolution and Correlation. The new approach of this implementation is mentally and easy to calculate of DSP operations for small length of sequences. In this paper a fast method for DSP operations based on ancient Vedic mathematics is contemplated. The implementation of high speed DSP operations of two finite length sequences using Vedic Urdhava-Triyagbhayam Multiplication Sutra (approach/method) is done. Urdhava-Triyagbhayam Sutra is very efficient multiplication formula applicable for all types of multiplication. This algorithm is implemented in XILINIX It reduces the 40-60% time from inbuilt function and this algorithm operates in concept of Vedic multiplier

Index Terms: DSP, Vedic mathematics, Vedic Multiplier, Vedic Convolution, Vedic Correlation

I. INTRODUCTION

DSP operation is the heart of the mobile communication and satellite communication system. The convolution plays a preciously role in Digital Signal Processing and Image Processing. It is used for designing of digital filter and correlation application. The linear convolution effectively designs by using simple Vedic multiplier. Convolution is basic concept to designing the finite impulse response filter, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT) [1]. Linear Convolution of two finite length sequence normally Computed by using the application of Discrete Fourier Transform [2, 3]. Design of all DSP operations with the help of high speed Vedic multiplier which increase the efficiency of system and reduces the processing time. This DSP implementation is design on Xilinx .which is user friendly and easy to use. In this method compute the 2N-1 point convolution sequence from N point discrete time sequence and N-point circular convolution of using 2N-1 point Convolution of discrete time sequence. To reduce the processing time of DSP such as Right–angle circular convolution is operation proposed alternative method [4].

II. VEDIC MATHEMATICS

Vedic mathematics is an ancient fast calculation mathematics technique which is taken from historical ancient book of wisdom. Vedic mathematics is an ancient Vedic mathematics which provides the unique technique of mental calculation with the help of simple rules and principles. Veda rediscovered by the holiness Jagad Guru Shree Bharti Krishna Tirtha Ji Maharaj (1884-1960) in between 1911-1918. According to Swami-Ji all Vedic mathematics is based on 16- Sutra (Algorithm) and 16- up-sutra (Sub-algorithm) after broadly research in Atharva Veda [5]. It computes all the basic as well as complex mathematical operation easily and quickly also provides a power full mantel technique. It is more consistent than modern mathematics and provides an expeditious solution. The term Vedic mathematics is evolving from the word "Veda" which means warehouse of all knowledge. It is based on sixteen sutras which transact different branches of mathematics i.e. algebra, geometry, arithmetic [6]. Former Shankrachrya Shree Bharti Krishna Tirtha of India was developed in to the ancient Vedic text and established the new method of this system in his pioneering work in Vedic mathematics (1965). Which was the starting point of the new work in Vedic math's era? A batter deal of research is also being transport how to develop more powerful and easy application of the Vedic sutras geometry, calculus, trigonometric, computing application (property). Modern mathematics is an integral part of the technical education most of the engineering system design is based on the various mathematical approaches. The necessity for expeditious processing speed used following Vedic mathematics algorithm.

- Ekadhikena Purvena – By one more than the previous one.
- Chalana-Kalanabyham – Differences and Similarities.
- Ekadhikina Purvena – By one more than the previous One.
- Ekanyunena Purvena – By one less than the previous one.
- Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.
- Gunitasamuchyah – The product of the sum is equal to the sum of the product.
- Nikhilam Navatashcaramam Dashatah – All from 9 and last from 10.
- Paraavartya Yojayet – Transpose and adjust.
- Puranapuranabyham – By the completion or noncompletion.
- Sankalana- vyavakalanabhyam – By addition and by subtraction.

- Shesanyankena Charamena – The remainders by the last digit.
- Shunyam Saamyasamuccaye – When the sum is the same that sum is zero.
- Sopaantyadvayamantyam – The ultimate and twice the penultimate.
- Urdhva-tiryakbhyam – Vertically and crosswise.
- Vyashtisamanstih – Part and Whole.
- Yaavadunam – Whatever the extent of its deficiency.

These methods and ideas can be directly applied to trigonometry, plain and spherical geometry, conics, calculus (both differential and integral), and applied mathematics of various kinds. As mentioned earlier, all these Sutras were reconstructed from ancient Vedic texts early in the last century. Many Sub-sutras were also discovered at the same time, which are not discussed here. The beauty of Vedic mathematics lies in the fact that it reduces the otherwise cumbersome-looking calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing. The multiplier architecture can be generally classified into three categories. First is the serial multiplier which emphasizes on hardware and minimum amount of chip area. Second is parallel multiplier (array and tree) which carries out high speed mathematical operations. But the drawback is the relatively larger chip area consumption. Third is serial- parallel multiplier which serves as a good trade-off between the times consuming serial multiplier and the area consuming parallel multipliers.

III. PROPOSED WORK:- URDHVA TIRYAKBHYAM SUTRA:

The multiplier is based on an algorithm Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The parallelism in generation of partial products and their summation is obtained using Urdhava Triyakbhyam explained in fig 1. The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Thus the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. The net advantage is that it reduces the need of microprocessors to operate at increasingly high clock frequencies. While a higher clock frequency generally results in increased processing power, its disadvantage is that it also increases power dissipation which results in higher device operating temperatures. By adopting the Vedic multiplier, microprocessors designers can easily circumvent these problems to avoid catastrophic device failures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers. Therefore it is time, space and power efficient. It is demonstrated that this architecture is quite efficient in terms of silicon area/speed.

*A. Multiplication of two decimal numbers- 325*738*

To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers (325 * 738). Line diagram for the multiplication is shown in Fig.1. The digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result and a carry. This carry is added in the next step and hence the process goes on. If more than one line are there in one step, all the results are added to the previous carry. In each step, least significant bit acts as the result bit and all other bits act as carry for the next step. Initially the carry is taken to be zero. To make the methodology more clear, an alternate illustration is given with the help of line diagrams in figure 2.2 where the dots represent bit „0" or „1".

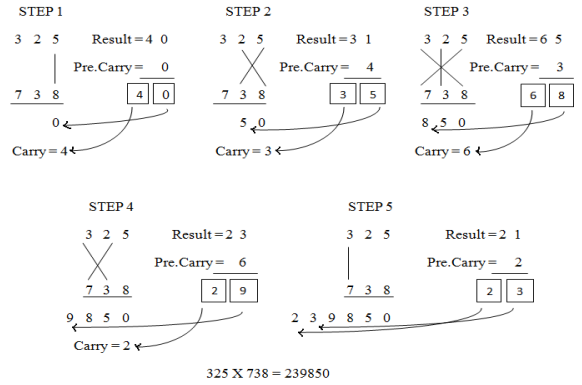

Figure.1: Multiplication of two decimal numbers by Urdhva Tiryakbhyam

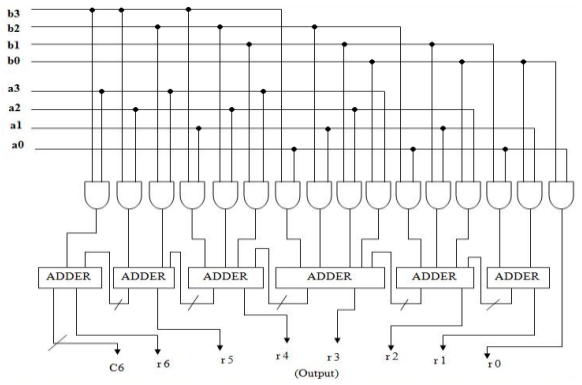

Figure 2: Hardware architecture of the Urdhva tiryagbhyam multiplier [4]

The hardware realization of a 4-bit multiplier is shown in

figure.2. This hardware design is very similar to that of the famous array multiplier where an array of adders is required to arrive at the final product. All the partial products are calculated in parallel and the delay associated is mainly the time taken by the carry to propagate through the adders which form the multiplication array

IV. PERFORMANCE AND SIMULATION RESULTS

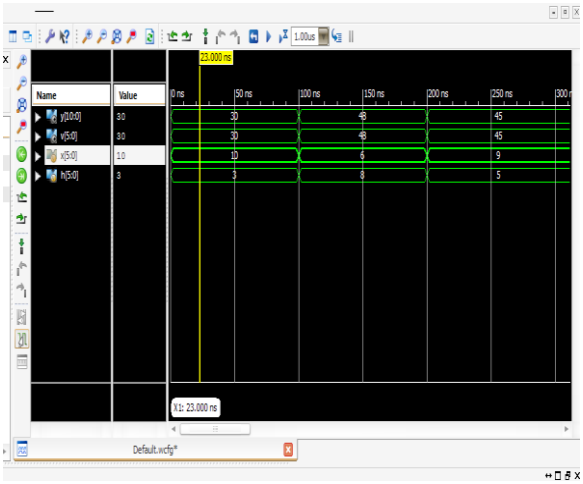

Figure.3.Simulation Result

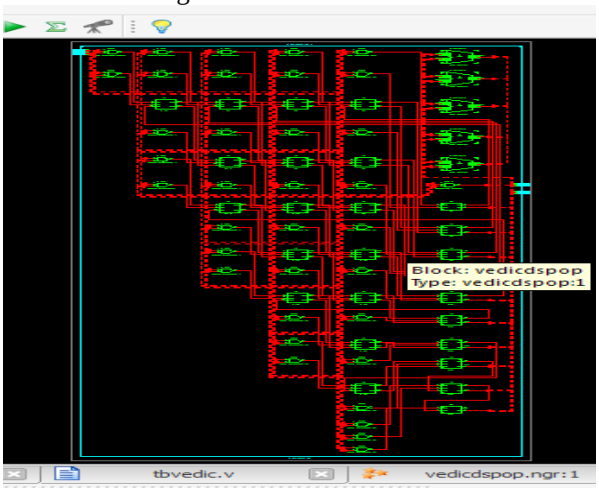

Figure.4.RTL TOP Module

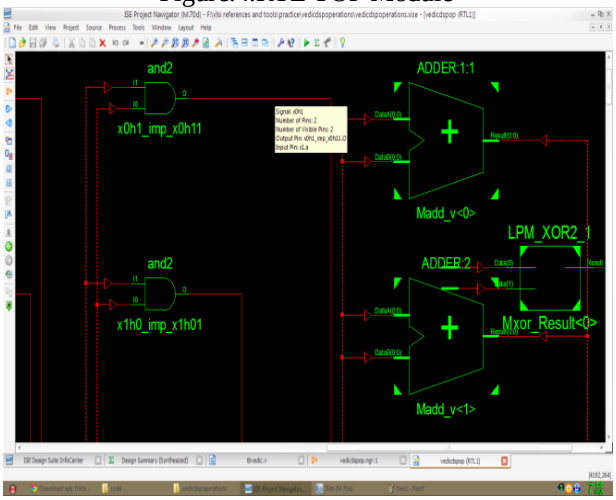

Figure.5. RTL Internal Module

V. CONCLUSION

A fast computation of DSP operations of two finite length sequence implemented in Xilinx. DSP operations are based on Urdhva-Tiryagbhyam method of Vedic mathematics, which reduces the processing time as compare to inbuilt function of Matlab. Proposed algorithm provide average processing time in micro second and conventional operation provide average time in milli seconds. In future, the Fast Fourier Transform and Filter operations are designed with the help of Vedic Urdhva- Tiryagbhyam method.

REFERENCES

[1] A.Kumar, A. Raman, Dr. Sarin, "Small area reconfigurable FFT design by Vedic math" in Proc. 2nd IEEE Int. Conf. Computer and Automatic Engineering, India vol. 5, 2010, pp.836-838.

[2] L. R. Rabiner and B. Gold, "Theory and Application of Digital Signal Processing". Englewood Cliffs, NJ: Prentice-Hall, 1975.

[3] J.G. Proakis and D.G. Monolakis, "Digital Signal Processing". Prentice- Hall International, Inc., 1996.

[4] W.Li, "The Modified fermat number transform and its application" in Proc. IEEE Int. Symposium on Circuit and System, Bethlehem, 1990,vol.3, pp. 2365-2368.

[5] Jagadguru Swami Sri Bharath, Krishna Tirathji, "Vedic Mathematics or Sixteen Simple Sutras from The Vedas", Motilal Banarsidas, Varanasi (India), 1992.

[6] Jeganathan Sriskandarajah, "Secrets of Ancient Maths: Vedic Mathematics", Journal of Indic Studies Foundation, California, 2003 pp. 15-16.

[7] Parth Mehta, Dhanashri Gawali, "Conventional versus Vedic mathematical method for Hardware implementation of a multiplier" ; in Proc. IEEE Int. Conf. Advances in Computing, Control, and Telecommunication Technologies, India, Dec. 2009, pp. 640-642.

[8] Sophocles J. Orfanidis "Introduction to Signal Processing" Prentice Hall, Inc.,1996–2009

[9] Sumantra Dutta Roy, Poonam Suryanarayan, "The Relation between discrete convolution /correlation and string matching, and exploring the possibility of a deterministic linear-time algorithm for discrete convolution/correlation" in Proc. IETE Journal of education, vol.51,April 2010.

[10] Isabella1and Emi Retna, "Study paper on test case generation for GUI based testing" in proc. Int. Journal Software Engineering & Applications, Vol.3, Jan 2012, pp. 3-8.

