LOW POWER FIR FILTER USING FIFTH APPROXIMATION ADDER

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Abstract: The demand for power efficient design has increased with the portable multiple devices employing various signal processing algorithms and architectures. In previous approach, voltage over scaling has emerged as one of the most effective technique for reducing power in digital designs, this technique is to mitigate the resulting errors. In this paper, propose a logic complexity reduction at the transistor level as an alternate approach to voltage overscaling. Based on this concept, propose various approximate adder cells with reduced complexity at the transistor level. The fifth approximate adder is reduced full adder having least number of transistors. By using this arithmetic unit design architecture like FIR filter. Simulation results indicate up to 97% power saving using the proposed approximate adder, when compared with existing accurate adder.

Index terms: CADENCE VIRTUSO, MATLAB, finite impulse response filter

I. INTRODUCTION

Digital signal processing (DSP) blocks form the backbone of various multimedia applications used in portable devices. Most of these DSP blocks implement image and video processing algorithms, where the ultimate output is either image or video compression. Human beings have limited perceptual abilities when interpreting an image or a video. This allows the outputs of these algorithms to be numerically approximate rather than accurate. This relaxation on numerical exactness provides some freedom to carry out imprecise or approximate computation either an image or a video for human consumption.

Therefore, using approximate arithmetic in such a scenario will not provide much energy benefit when considering the complete processor. Programmable processors are designed for general-purpose applications with no application-specific specialization. Therefore, there may not be many applications that will be able to tolerate errors due to approximate computing. This also makes general-purpose processors not suited for using approximate building blocks. This issue has already been discussed in [1].

Therefore, in this paper, we consider application-specific integrated circuit implementations of error-resilient applications like image and video compression. We target the most computationally intensive blocks in these applications and build them using approximate hardware to show substantial improvements in power consumption with little loss in output quality. Approximate computing enables voltage over scaling in Multimedia hardware, obtaining substantial power savings by allowing graceful degradation in output quality since the important computations and data bits remain unaffected. Voltage over-scaling (VOS) [2] deliberately lowers VDD to a value for which the circuit is known to occasionally produce erroneous outputs. VOS is applicable to resilient applications, which can tolerate error-induced output deviations. Key concept of this paper is low-power design using simplified and approximate logic implementations. Since DSP blocks mainly consist of adders and multipliers, we propose several approximate adders, which can be used effectively in such blocks. In this paper, fifth approximate adder is used because it consumes less power or saving power than the other four approximate adders. Steps done in this paper can be summarized as follows.

- Accurate adder and four other approximations are designed and simulated by using TSMC 180nm technology.
- Propose the fifth approximate adder which is reduced complexity of full adder and less number of transistors.
- The fifth approximate adder is designed and simulated.
- The FIR filter which is algorithm and architecture has designed with constraints. By using RTL compiler RTL top module block designed.
- The fifth approximation is added to the FIR filter to get the power consumption results.

II. APPROXIMATE ADDERS

In this section, step by step procedures for coming up with various approximate full adder cells with fewer transistors. Removal of some transistors will facilitate faster charging/discharging of node capacitances. Moreover, complexity reduction by removal of transistors also aids in reducing the αC term (switched capacitance) in the dynamic power expression Pdynamic = αCV2DDf,where, α is the switching activity or average number of switching transitions per unit time and C is the load capacitance being charged/discharged. This directly results in lower power dissipation. Area reduction is also achieved by this process. The conventional MA implementation followed by the proposed approximations.

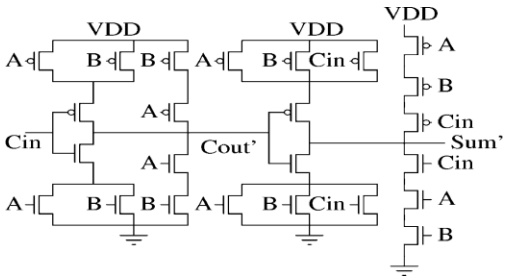

Fig 1: Conventional adder

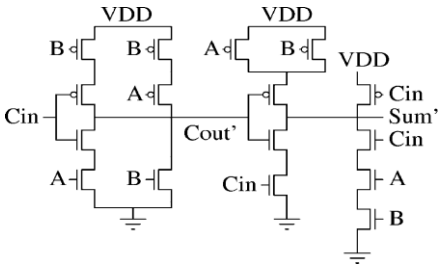

Fig2:Approximation1

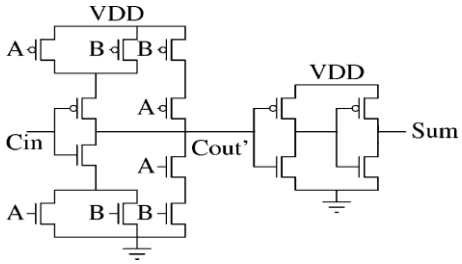

Fig3:Approximation2

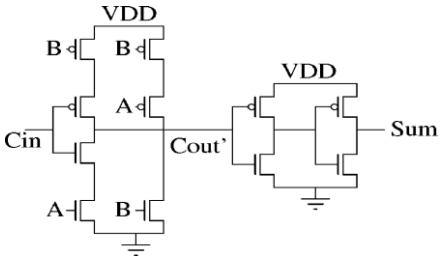

Fig4:Approximation3

A. Conventional MA:

Fig.1 shows the transistor-level schematic of a conventional MA(Mirror adder)[3],which is a popular way of implementing an FA. It consists of a total of 24 transistors. Since this implementation is not based on complementary CMOS logic, it provides a good opportunity to design an approximate version with removal of selected transistors.

Sum=ABCin+A'B'Cin+A'BCin'+AB'Cin'

Cout=AB+A'BCin+AB'Cin.

B. Approximation 1:

In order to get an approximate MA with fewer transistors, we start to remove transistors from the conventional schematic one by one. However it cannot do this in an arbitrary fashion. The need to make sure that any input combination of A,B and Cin does not result in short circuits or open circuits in the simplified schematic. Another important criterion is that the resulting simplification should introduce minimal errors in the FA truth table.

Sum = A1B1Cin+ ABCin.

Cout=ABCin+ABC1in+AB1Cin+A1BC1in.

C. Approximation 2:

The truth table of an FA shows that Sum= Cout' for six out of eight cases, except for the input combinations A = 0,B = 0,Cin = 0 and A = 1,B = 1,Cin = 1. Now, in the conventional MA, Cout' is computed in the first stage. Thus, an easy way to get a simplified schematic is to set Sum= Cout'. However, we introduce a buffer stage after Cout'(see Fig. 3) to implement the same functionality. The reason for this can be explained as follows. If we set Sum= Cout' as it is in the conventional MA, the total capacitance at the Sum node would be a combination of four source–drain diffusion and two gate capacitances. This is a considerable increase compared to the conventional case or approximation 1. Such a design would lead to a delay penalty in cases where two or more multi-bit approximate adders are connected in series, which is very common in DSP applications.

Sum = Cout1.

Cout = AB+A'BCin+AB'Cin.

D. Approximation 3:

Further simplification can be obtained by combining approximations 1 and 2. Note that this introduces one error in Cout and three errors in Sum. The corresponding simplified schematic is shown in Fig. Approximation 3 has 11 numbers of transistors. The sum is followed buffer. The sum is complement of the Cout.

Cout = ABCin +ABCin'+AB'Cin.

Sum = Cout'.

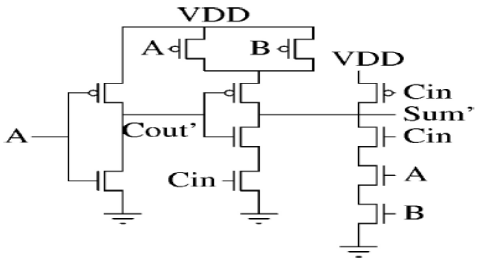

Fig5:Approximation4

E. Approximation4:

A close observation of the FA truth table shows that Cout=A for six out of eight cases. Similarly, Cout=B for six out of eight cases. Since A and B are interchangeable, here consider Cout = A. Thus, propose a fourth approximation where just use an inverter with input A to calculate Cout' and Sum is calculated similar to approximation 1. This introduces two errors in Cout and three errors in Sum. The corresponding simplified schematic is shown in Fig. In all these approximations, Cout is calculated by using an inverter with Cout' as input.

Sum = A'B'Cin+A'BCin+ABCin.

Cout =A.

F. Approximation5:

In approximation 4, it finds that there are three errors in Sum. By extend this approximation by allowing one more error, i.e., four errors in Sum. The use approximation Cout = A, as in approximation 4.Since the proposed approximate FA cells have fewer transistors, this also results in area savings. Approximation 5 provides maximum area savings among all approximations. The proposed approximations also help in reducing the overall propagation delay.

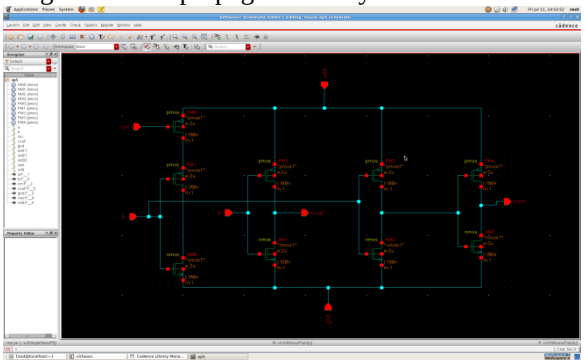

Fig6: Proposed schematic of Approximation5

Sum = B, Cout = A

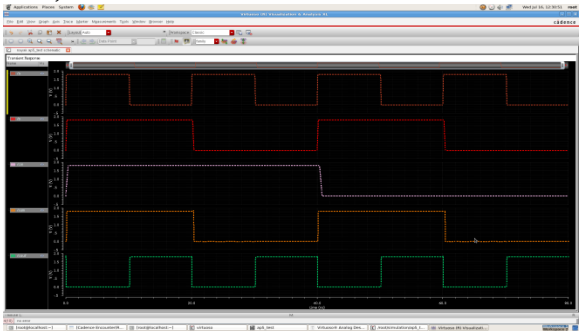

Fig7: output waveform of Approximation5

Table1: Truth table of Approximation5

Choice 1		Choice 2	
Sum= *A*	C_{out} = *A*	Sum= *B*	C_{out} = *A*
0 ✓	0 ✓	0 ✓	0 ✓
0 ×	0 ✓	0 ×	0 ✓
0 ×	0 ✓	1 ✓	0 ✓
0 ✓	0 ×	1 ×	0 ×
1 ✓	1 ×	0 ×	1 ×
1 ×	1 ✓	0 ✓	1 ✓
1 ×	1 ✓	1 ×	1 ✓
1 ✓	1 ✓	1 ✓	1 ✓

III. FIR FILTER

Filter is an electronic device is circuit that allows selected frequencies to pass through it. The objective of filtering is to improve the quality of a signal by removing the noise or to extract the required information from signals. The nature of filtering depends on the frequency response characteristics H(ejw). The filters which are designed by using finite samples of impulse response are called Finite Impulse Response (FIR) filters. In FIR filters, the samples response sequence is of finite duration i.e., it has a finite number of non-zero terms.

i.e., h(n) = 0 for n < 0 for n ≥ N

This unit sample response exits only for the duration from 0 to N – 1. Therefore, this is a FIR system.

A. Implementation Of Fir:

Consider a 25 tap low-pass equiripple FIR filter with the following specifications: Fs =48 000 Hz, Fpass = 10 000 Hz, Fstop = 12 000 Hz. The coefficients of this filter c0, . . . , c24 were obtained using the MATLAB FDA tool [4].

The filter coefficients are….Radix= 16;Coefficient width=16; Coefficients Data=F5 , F780, 0526,0512, FDD5 ,F6D0, 00CD, 0D87, 0355, EAB3, F1DB, 2CE4, 6B5E, 6B5E, 2CE4, F1DB, EAB3, 0355, 0D87, 00CD, F6D0, FDD5, 0512, 0526, F780, FBF5;

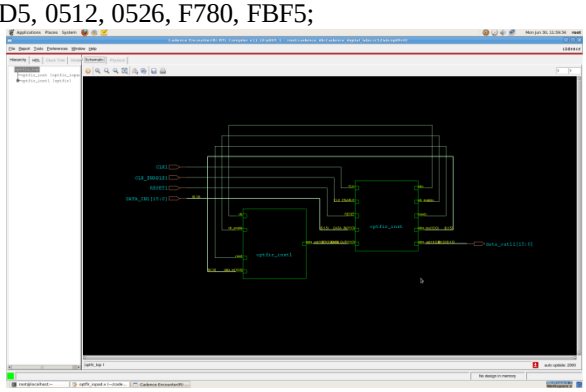

Fig 8:FIR filter RTL diagram

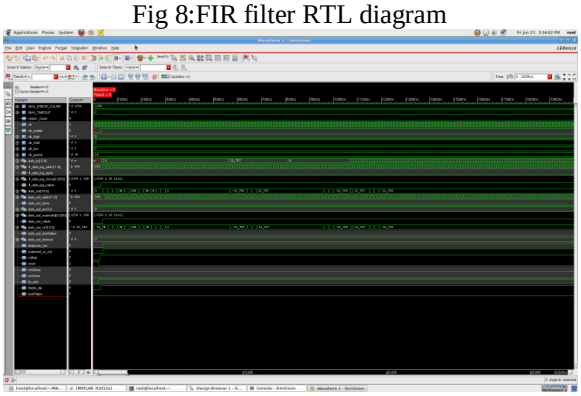

Fig.9: output waveform of FIR filter

Table 2 : Power Results for FIR Filter

Approximation type	Power consumption (mW)
Conventional MA	21.370
Approximation 1	20.195
Approximation 2	16.340
Approximation 3	14.866
Approximation 4	10.940
Approximation 5	10.933

It shows Approximation5 consumes less power compared to other approximation adders and % of power saving upto 97%.

IV. CONCLUSION

In this paper, we proposed several imprecise or approximate adders that can be effectively utilized to trade off power and quality for error-resilient DSP systems. Our approach aimed to simplify the complexity of a conventional MA cell by reducing the number of transistors and also the load capacitances. This approach differed from previous approaches where errors were introduced due to VOS[5]-[6]. Using these models, we discussed how to apply these approximations to achieve maximum power savings subject to a given quality constraint. This procedure has been illustrated for FIR filter. We believe that the proposed approximate adders can be used on top of already existing low-power techniques.

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