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DESIGN AND POWER OPTIMIZATION OF A LOW VOLTAGE CASCODE CURRENT MIRROR WITH ENHANCE DYNAMIC RANGE

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Abstract: ***The cascode current mirror is one of the most necessary part in both in analog and mixed mode VLSI circuits. it is suitable for operation at low voltage levels is presented And the mirror has high input and high output voltage swings. The presented current mirror circuit combines the advantages of wide input - output swing and large output resistance capability which makes it attractive for low-voltage and low power application. It is Based on IBM 0.18um MOS model parameters, TSPICE simulation results show that the input current range of 1uA to 2mA with 882.83MHz bandwidth for the presented level shifted low voltage current mirror circuit. The power consume has improved by more than forty percentage (40%).***

Index Terms—simple current mirror, Low voltage current mirror, level shifted Current mirror, Level shifted low voltage current mirror, Dynamic range

I. INTRODUCTION

Now a day, microelectronics (VLSI) is dominant in every sphere of electronics and communications forming the backbone of modern electronics industry in mobile communications, computers, state-of-art processors etc. So the portable electronics has made low power circuit design extremely desirable. All efforts eventually converge on decreasing the power consumption entailed by ever compacted size of the circuits enabling the portable gadgets. Reducing the power supply voltage is a straightforward method to achieve low power consumption. The low power and low voltage CMOS techniques were applied extensively in analog and mixed mode circuits for the compatibility with the present IC technologies. Designing high – performance analog circuits is becoming increasingly challenging with the persistent trend towards reduced supply voltages. The current mirror (CM) is one of the most basic building blocks both in analog and mixed mode VLSI circuits especially for active elements like op-amps, current conveyors, current feedback amplifiers etc. At large supply voltages, there is an exchange speed, power and gain. The main characteristics under consideration are power, voltage, dynamic range, bandwidth, low offset voltage, high output voltage swing. The desire for portability of the electronic equipment generated a need for low power systems in battery operated products like hearing aids and implantable cardiac pacemakers and cell phones and hand held multimedia terminals. Low power dissipation is attractive, and perhaps even essential in these applications to have reasonable battery life and weight. The main objective of design is close to having battery- less systems, because the battery contributes greatly to volume and weight.

II. LOW VOLTAGE CURRENT MIRROR

The Low Voltage current mirror is the basic building block of analog integrated circuit. Current mirror enables a single current source to supply mirrors are output impedance and voltage headroom. The output impedance determines the variation of the mirrored current when the applied voltage varies. Higher output impedance implies less current variation with applied voltage and hence more stable current source Voltage headroom specifies how much voltage drop across the current mirror is required to operate the current mirror reliably. This is important for low voltage circuit design [2].

Low voltage cascode current shown in Figure 1.

We assumes that the current mirror transistors (M1) and (M2) have identical. Ascept ratio

$A_m = \frac{W_1}{L_1} = \frac{W_2}{L_2}$ Where 'W1' and 'W2' are showing the transistor channel width and L1 and L2 are the transistor length.

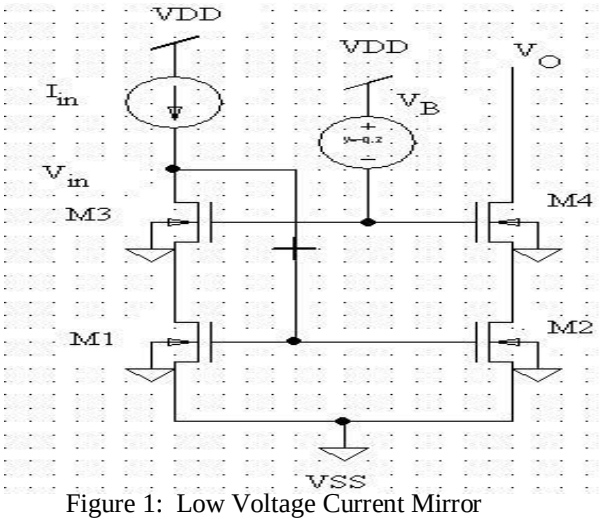

Figure 1: Low Voltage Current Mirror

Similarly the transistor (M3) and (M4) are assumed the same aspect ratio

$$A_c = \frac{W_3}{L_3} = \frac{W_4}{L_4}$$

the aspect ratio A_m may be different from the aspect ratio A_c. The partition of the dynamic range the same aspect ratio of A_m and A_c and we use standard Schman –Hodges transistor model for the transistor in the saturation region and

we neglected the bulk effect and assume that all the NMOS transistors have the identical. Low voltage current mirror input current I_{in} we find the gate- source voltages and drain - source voltages [3]

$V_{Gs1} = V_{tn} + \sqrt{\frac{2I_{in}}{KA_M}}$ ..... (1)

Gate to source voltage of transistor (M3).

$V_{GS3} = V_{tn} + \sqrt{\frac{2I_{in}}{KA_C}}$ ..... (2)

Drain to source voltage of transistor ((M1)) is

$V_{DS1} = V_{BC} - V_{tn} - \sqrt{\frac{2I_{in}}{KA_C}}$.....(3)

Drain to source voltage of transistor ((M3))is

$$V_{DS3} = V_{GS1} - V_{DS1}$$

$= \boldsymbol{2V_{tn} - V_{BC} + \sqrt{\frac{2I_{in}}{K}}\ \frac{1}{\sqrt{A_M}} + \frac{1}{\sqrt{A_C}}}$..... (4)

Where,(Vtn) is the transistor threshold voltage, (VBC) is the bias or gate voltage of transistor (M3) , (M4) and K is the transconductance parameter. Requiring $V_{GS} - V_{tn} \leq V_{DS}$ for both (M1) and (M3) result in :

$\sqrt{\frac{2I_{in}}{K}}\ \left(\frac{1}{\sqrt{A_M}} + \frac{1}{\sqrt{A_C}}\right) + V_{tn} \leq V_B$ .....(5)

Biasing voltage

$V_B \leq 2V_{tn} + \sqrt{\frac{2I_{in}}{KA_M}}$ ----------(6)

In Figure 1 low voltage current mirror, biasing voltage VB is fixed when Iin increases, voltage of the gate –source voltage VGS3 of transistor (M3) and Vin will increase, and voltage level at the drain terminal of (M1) decrease. There by (M1) enter the triode region which determine the upper limit of Iin.below equation (7) ensure the saturation (M1) and determine the maximum value of Iin for given value of the cascade bias voltage VB we find

$$I_{in,max} = \frac{k}{2} A_M (\mathrm{V_B} - \mathrm{V_{tn}})^2 \left(\frac{\sqrt{\frac{A_C}{A_M}}}{1 + \sqrt{\frac{A_C}{A_M}}}\right)^2 \ldots (7)$$

Equations(7) ensure the saturation of (M3) and determine the minimum value of Iin we find

$$I_{in,min} = \frac{k}{2} (\mathrm{V_B} - 2\mathrm{V_{tn}})^2 \mathrm{A_M} \ldots\ldots\ldots (8)$$

the value of AC and AM which determined the saturation of (M1) and the maximum value of input current . The Saturation operation of transistors (M1) and (M3) the input current range determined by

$$\frac{k}{2} A_M (\mathrm{V_B} - 2\mathrm{V_{tn}})^2 \leq \mathrm{I_{in}} \leq \frac{k}{2} A_M (\mathrm{V_B} - \mathrm{V_{tn}})^2 \left(\frac{\sqrt{\frac{A_C}{A_M}}}{1 + \sqrt{\frac{A_C}{A_M}}}\right)^2 \ldots\ldots\ldots\ldots\ldots (9)$$

In a practical design procedure equation(8) can be used to determine the maximum value of the bias voltage which will ensure saturation of (M3) even at the minimum value of input current, and equation (6) can then be used to determine values of AC and AM which will ensure saturation of (M1), even at the maximum value of input current. In the important special case of Iin,minim= 0 we find from (8) VB ≤ 2Vtn .From equation (7) we then find the following design constraint on AC and AM

$A_M \left(\frac{\sqrt{\frac{A_C}{A_M}}}{1+\sqrt{\frac{A_C}{A_M}}}\right)^2 \geq \frac{2I_{in,max}}{{V_T}^2 K}$ .....(10)

Assuming as a typical case W1 = W3 and L1 = L3 i.e. identical aspect ratios for the mirror transistors and the cascode transistors, we find that

$A_M = A_c = \frac{W}{L} \geq \frac{2I_{in,max}}{{V_T}^2 K}$ .....(11)

In this case of effective gate source voltage of the mirror transistors (M1) , (M2) is

$V_{Gs1} - V_{tn} = \sqrt{\frac{2I_{in}}{KA_M}} = \frac{V_{tn}}{2} \sqrt{\frac{I_{in}}{I_{in,max}}}$.....(12)

In this case the minimum output voltage of the current mirror is and is independent of the input

$$V_{out,min} = V_B - V_{tn} = V_{tn} \ldots\ldots\ldots (13)$$

In a high precision current mirror one would like to have as large an effective gate-source voltage as possible in order to minimize the effect of threshold voltage dissimilarity.This obvious that the effective gate source voltage VGs1 -Vtn can be increase the value of above given by equation (15) if Ac isincreased, i.e. a larger aspect ratio is used for the cascade transistor. This case the(cascode transistor) requires a smaller effective gate-source voltage for a given value of input current and leaving more headroom for the drain source voltage of the mirror transistor. Introducing

N= AC /AM We find

$A_M = \left(\frac{1+N}{N}\right)^2 \frac{2I_{in,max}}{(V_B - V_{tn})^2 K}$ .....(14)

And

$$V_{Gs1} - V_{tn} = \frac{N}{(1+N)} (V_B - V_{tn}) \sqrt{\frac{I_{in}}{I_{in,max}}}$$

.....(15)

The (small signal) output resistance of the mirror is given by:-

$$r_{out} = \frac{1}{g_{ds2}} \left(1 + \frac{g_{dm4}}{g_{ds4}}\right) \frac{1}{g_{ds2}} \frac{g_{m4}}{g_{ds4}} \ldots (16)$$

As $\frac{g_{m4}}{g_{ds4}}$ is inversely proportional to the square root of ($A_{C)}$ .we find that the output resistance is inversely proportional to (N). Thus, the higher effective gate-source voltage of the mirror transistors is achieved at the expense of a reduced output resistance.

III. LEVEL SHIFTED CURRENT MIRROR

Shown in figure 2 level shifted current mirror, the simple current mirror topology [10] requires input voltage (V_{in}) at least one V_{tn} and unsuitable for low voltage application. Level shifted current mirror operates at low voltage with the advantage of low input output voltage requirement, incorporates a level shifter PMOS transistor (M5) (biased

through a current I_{bias1}) at input port. For this structure, we have

$V_{DS1} = V_{GS1} - V_{GS5}$ .....(17)

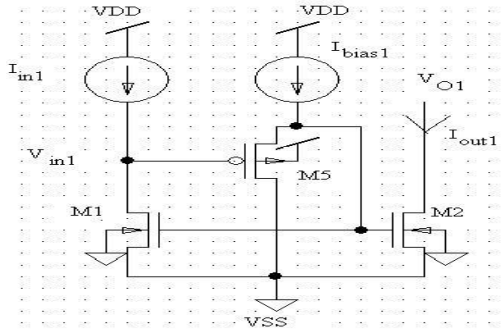

Figure 2: Level Shifted Current Mirror

Where VDS1 drain to source and VGS1 gate to source voltage of (M1), VGS5 is the gate to source voltage of (M5). A level shifted current mirror circuit structure is shown in Figure 2 (M3) is used to shift the voltage level at the drain terminal of (M1). Vin is a characteristics parameter of a low voltage current mirror and decides the range of input voltage swing in such circuits. The bias current (Ibias1) decide the operation region of (M1). For example, low value of(Ibias1) forces (M3) to operate in sub threshold region, (Ibias) high (Ibias1) ensures transistor (M5) operates the triode region. For high value, transistor (M2) operates in saturation region. Gate voltage of transistor (M1) is high correspondingly input current is also high.Hence Vin can be calculated for this circuit structure if we must idea about the values of (VGS1) and (VGS5) since (Vtp ≥ Vtn) , there is a main difficulty to keep the condition ($V_{GS1} - V_{GS5} > 0$) valid in a level shifter based circuit over a wide range of (Iin1) . One solution of this is to use a lateral p-n-p transistor(bjt) for level shifting, and now ($V_{in1} - V_{GS1} - V_B > 0$) approximates as(0.7V) and V_{GS1} is always more than(0.8v) (if we assume Vtn =0.8v). As the device sizes are reducing and (Vt) is also reducing and there will be a situation where ($V_{GS1} - V_B > 0$) will not be valid and hence we can not be able to use p-n-p transistor. Therefore , there is a need to must have an alternative a p-n-p transistor and the use of a PMOS transistor is the most obvious choice..

IV. LOW VOLTAGE LEVEL SHIFTED CURRENT MIRROR

The Fig 3 is show the level shifted low voltage cascode current mirror ,It is the mainly combination of low voltage and level shifted current mirror and The combined the low voltage and level shifted current mirror present a result , level shifted low voltage current mirror. In this topology mainly achieve larger dynamic range for low voltage operation. The operation of transistor (M5) and transistor (M3) are similar shown in the Figure 2 of transistor(M 5) and transistor (M1), we adopt the same assumptions as above in low voltage in this current mirror. We assume figure 3.5 the threshold voltage of (M5) is (V_{tp})when the level shifted current mirror transistor (M5) and transistor (M1) on must be conditions satisfied(VGS3 > V_{tn}) and (VGS5 > V_{tp}) , but when (V_{tp} > V_{tn}) there is a little difficulty to the condition satisfy (VDS3 >0) wide range of input current (I_{in2}.). we can find the most suitable operation mode of (M5) is in sub threshold region because here is low input current and in the saturation region high input current of (M1) and(M3). The assumption under the ($V_{SD5} > 3V_t$) ,the sub-threshold drain current of transistor (M5) can be expressed as following:-

$$I_{bias2} \approx \frac{W_5}{L_5} I_{DO5} \exp\left(\frac{V_{SGS} - |V_{tp}|}{nV_T}\right) \text{.....(18)}$$

In the above equation (18) ,(W5) and (L5) represent the channel width and length of transistor (M5) respectively, and V_t (approximately ≈26mv at room temperature), equqtion [2] is thermal voltage. The Constant 'n' and (I_{do5}) are process parameters. Typically value of(I_{DO5} ≈20nA) and 'n' lie between 1.2 and 2.0 . For the sub-threshold operation of (transistor) M5 (V_{SGS} ≈$|V_{tp}|$) and saturation operation of transistor (M1) and transistor (M3), find

$$I_{in2} \leq \frac{KA C V_{scs}}{2} \leq \frac{KA C V_{tn}}{2} \quad \text{.....} \quad (19)$$

$$V_{tn} \leq V_{in2} \leq V_{SG5}\sqrt{\frac{A_C}{A_M}} + V_{tn} \leq V_{tn}\left(1 + \sqrt{\frac{A_C}{A_M}}\right) (20)$$

When transistors (M1), (M3), (M5) respectively are in sub-threshold region and the gate to source voltage of transtitor (M1),(M3) and (M5) are almost near to their threshold voltages, we can find

$$I_{in2} \leq \frac{I_{DD1} W_1}{L_1} \quad \text{.....} \quad (21)$$

$$V_{in2} = nV_T \ln \frac{I_{in2}}{I_{DD1}} \frac{L_1}{W_1} + V_{tn} \leq V_{tn} \quad \text{.....} (22)$$

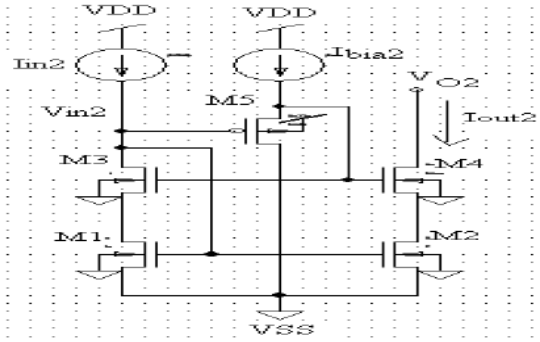

Figure 3:- Level Shifted Low Voltage Cascode Current Mirror

The Sub threshold operation of transistor (M5), when the input current (I_{in2}) increases the input voltage (Vin2) is also increases, transistor (M5) shifts the voltage level at gate terminal of transistor(M3), there for this current mirror must be improved the upper limit of the input current, compared to low voltage cascode current mirror. The current through transistor(M5) should be small enough to keep in transistor (M5) in sub-threshold region. Correspondingly the channel width and length ratio of the transistor (M5) should also be large. The current through transistor (M1) and M3 should be large to keep it in saturation region. Level shifted low voltage cascode current mirror input current (I_{in2}) is low, The transistor (M1) and (M3) are operate in sub-threshold region. When input current (i.e. I_{in2}) is low, transistor (M3) and (M1) will operate in sub- threshold region. If only transistor (M5)

operates in sub-threshold region and transistor (M1)-(M4) are restricted to operate in saturation region, this current mirror will possesses better frequency response and the lower limit of the input current is slightly higher And the minimum output voltage of the level shifted low voltage cascode current mirror is equal to following :-

$$V_{O2,min} = V_{GS2} + V_{GS4} - 2V_{tn} = \sqrt{\frac{2I_{in}}{KA_M}} + \sqrt{\frac{2I_{in}}{KA_C}} \quad ...(23)$$

V. SIMULATION RESULT

The above circuit shown in Figure-1, Low voltage current mirror and in Fig-3 level shift low voltage current mirror is simulated by using '0.18µm IBM MOS model parameters technology' with DC supply voltage of 1V. The biasing voltage ($V_{B)}$ in figure-1 and the biasing current (I_{bias}) in figure-3 are (-0.2v) and (0.3µA) respectively. Transistor (M1) and transistor (M3) ensure that the saturation operation biasing voltage (V_5) and ($I_{bias)2}$ selected ensure the operate transistor (M5) sub-threshold region gate to source voltage (M5) is slight lower than. The Table.1 summarizes the (W/L) ratios of MOSFETs used in circuits. The input characteristics of CCM is shown in the figure.4 and the current transfer characteristics shown in figure.5 and the Power dissipation of CCM is shown in Figure.6 and the Frequency Response shown in Figure.7. The figure 8 showing LVCM maximum input current of low voltage current mirror here input current is sweep 0 mA to 5 mA with supply voltage 1V.Figre.9 shows power dissipation results of LVCM. The Power dissipation result of LSLVCM is supply voltage (1) volt and I_{in} of (1)mA. Width and length of transistors (M3) & (M4)and (M1) & (M2) are kept same. The Transient analysis is used to calculate the power dissipation in the current mirror. In the Figure.10 shows power dissipation results. The Power results are reported at the end of transient simulation in the output file.

A. Width and Length Used In Low Volatge, Level Shifted, Low Voltage Level Shifted Current Mirror

Table I: - Aspect Ratio(W/L) of transistors used in LVCM current mirrors

MOSFETs	Type	Width	Length
M1,M2,M3,M4	NMOS	20µm	0.5µm
M5	PMOS	10µm	0.3µm

Table 2:- Parameters used in Low Voltage Current Mirror (LVCM)

Parameter	Unit
Supply voltage	1.0 volt
V_{bias} (Voltage bias)	-0.2 volt
Threshold voltage V_{tn} (NMOS)	0.44 Volt
Trans conductance	156.8µA

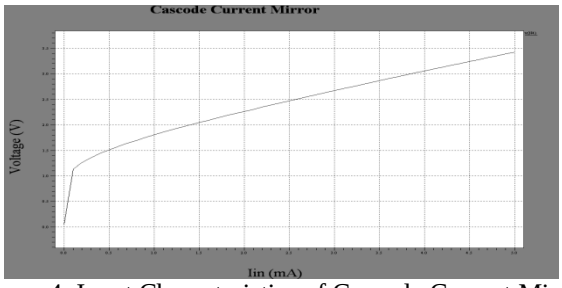

Figure 4: Input Characteristics of Cascode Current Mirror (CCM)

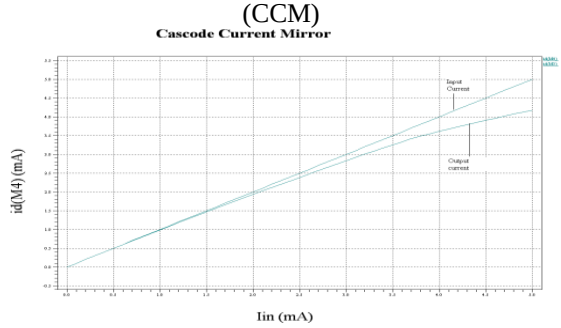

Figure 5: Current transfer characteristics of cascade current mirror (CCM)

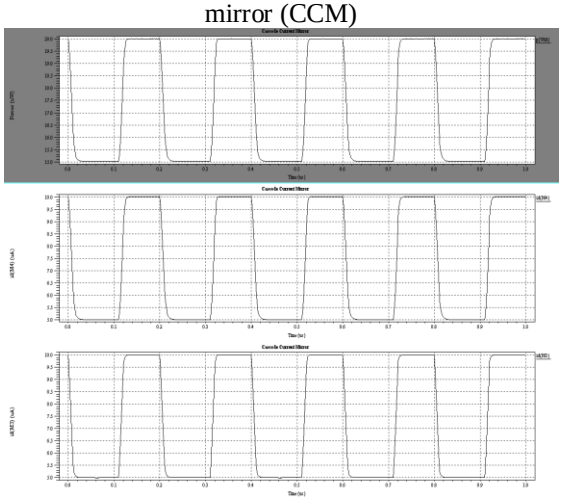

Figure 6: Power dissipation of Cascode Current Mirror (CCM)

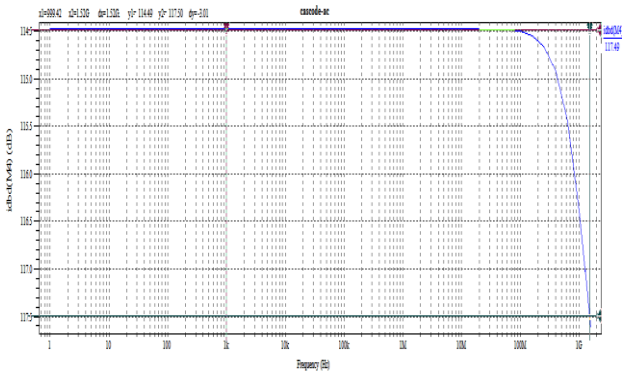

Figure 7: Frequency Response of Cascode Current Mirror (CCM)

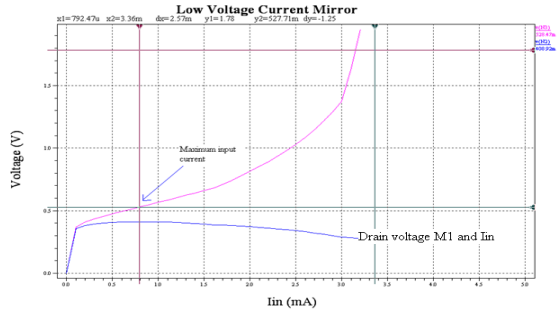

Figure 8: Low voltage current mirror maximum input current

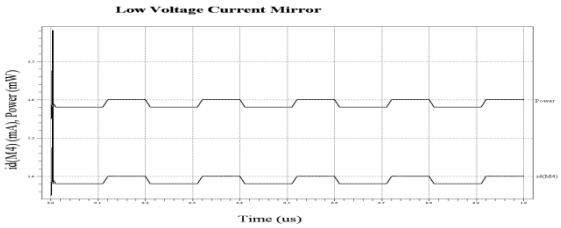

Figure 9: Power dissipation of LVCM

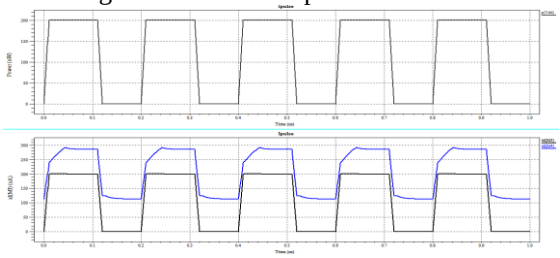

Figure 10: Power dissipation of LSLVCM

VI. CONCLUSION

Due to the nature of the wide research topic, there are still several area of improvement for future works in current mirrors. Many new current mirror topologies has been recently reported based on regulated cascode current mirrors. These new topologies provide improved current mirror characteristics. I have simulated some of these topologies to realize improvement that can be achieved. The main objective of this work was to reduce the power dissipation and also to improve bandwidth and the dynamic range in CMOS current mirror operating on a supply voltage of 1V.The bandwidth has been improved 160 MHz and Dynamic range has been improved by a factor of 800µA as compared to the reference work. The power dissipation has also improved by greater than 40%.

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