VLSI DESIGN OF HALF-BAND IIR INTERPOLATION AND DECIMATION FILTER

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Abstract: This paper presents a straight forward hardware optimization method for the half-band Infinite-Impulse Response (IIR) filter and multiplier free half-band IIR filter. This methodology provides a fast style choice at the system level, but not the requirement for computing complex simulations and calculations. The structure of the multiplier-free IIR half-band filter deals with a systematic approach to sharpen the half-band IIR filters. Starting from a half-band IIR sub filter, this systematic approach makes use of several algebraic composition sub filters to design a composite half-band IIR filter. Multipliers are most often used in digital signal processing applications and many VLSI computational units. In this paper a half band IIR Filter is proposed using Array multiplier, Wallace tree multiplier. Delay is reduced by 19.43%, 21.06% by implementing Array multiplier, Wallace multiplier respectively. Half-band IIR filter by using Wallace multiplier is delay and area efficient, when compared with array multiplier. Synthesis and simulation is achieved through Xilinx ISE 13.2

Keywords: Interpolation, low power, Infinite-Impulse Response (IIR) filter, Half-band filter sigma delta Σ−Δ modulator, multiplier-free structure, wallace tree.

I. INTRODUCTION

Computational and signal processing tasks are now implemented predominantly by digital means, since digital circuits are powerful and can be realized by significantly small and easy structures which can in turn be combined to acquire very exact, complex and quick systems. Because the physical world nonetheless remains stubbornly analog, data converters are needed to interface with the digital signal processing (DSP) system. In signal processing system with a central digital engine, analog input and output signals, the analog input signal (usually after some amplification and filtering) enters in to analog to digital converter (ADC) which converts it into a digital data stream. This stream is processed by the DSP core, and the resulting digital output signal is reconverted into analog form by a digital-to-analog converter (DAC). DAC output is generally also filtered and amplified to obtain the analog output signal. Data converters (both ADCs and DACs) can be classified into two main categories: Nyquist-rate and oversampled converters. In the first category, there exists a one-to-one correspondence between the input and output samples. Oversampling analog to digital converters will be discussed. The two types of oversampling modulators are delta modulator and the sigma delta modulator. A fundamental delta modulator used as an ADC. It is a feedback loop, contains an internal low-resolution ADC and a loop filter (an integrator) in addition to DAC. In delta modulator output depends on the difference between a input sample and a predicted value of that sample. In the normal case, the loop filter may be a higher-order circuit that produces a more exact prediction of the input sample u(n) than u(n-1), to subtract from the actual u(n). For oversampled signals the difference (u(n) - u(n - 1)) is much lesser than u(n), and hence larger input signals can be permitted. This is very advantageous. There are disadvantages also. The loop filter (integrator) is in the feedback path, and hence its non-idealities limit the achievable linearity and accuracy. The differencing at the input, and next the addition in the loop filter, and thus it is a delta-sigma modulator.

II. EXISTING SYSTEM

a) Half band IIR Filter

Delta-sigma modulator is used to relax the circuit prerequisites like pairing the elements, at the cost of high-frequency behavior. On account of oversampling behavior of delta sigma modulators, former to the modulator we are using an interpolation filter.

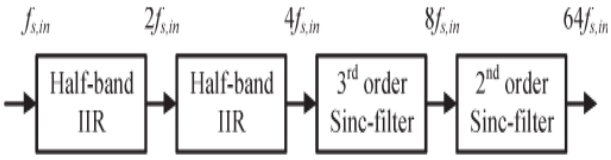

Fig.1. Multistage interpolation filter consisting of four stages

The interpolation filter is implemented by the digital to analog converter as multistage filter to minimize the hardware demands and power consumption [1]. Fig 1 provides an example that raises the sampling frequency of input signal from fs to 64fs using interpolation filter which consists of four stages. By using this filter as a first section in interpolation filter this becomes the hardware challenging factor [1], [2]. Alternatively half-band IIR filter is implemented if the phase linarites are not taken in to consideration to minimize the hardware demands and power consumption [3].To achieve this motive, initially an optimization technique was designed to convert the sampling rate using a polyphase IIR structure [4](in Figs. 2 and 3).

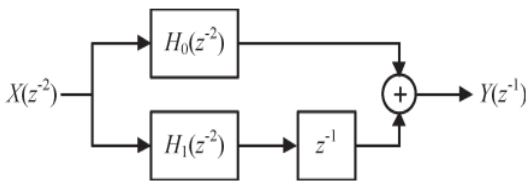

Fig.2. Half band IIR filter structure

Fig 2 shows two all-pass filters H_0 (z^{-2}) and $H1$ (z^{-2}), connected in parallel. The input signal is $X(z^{-2})$,output signal is $Y(z^{-1})$ respectively. Half band IIR filter is running at 2*fs*, in frequency. This filter is used as the initial stage of the filter in Figure 1.

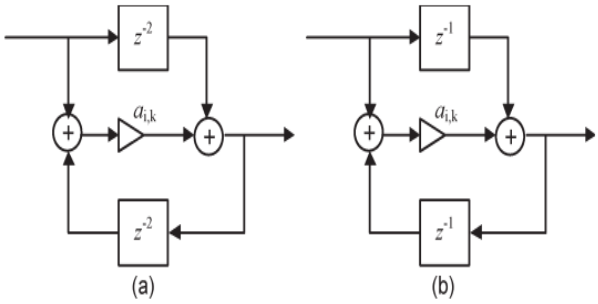

Fig.3. Second order all pass filter which runs at (a) 2*fs*, in and (b) *fs*, in.

In Fig 2 as shown the filter is used to achieve the interpolation .By make use of all-pass filters of second order, $H0(z^{-2})$ and $H1(z^{-2})$ that is shown in Fig. 1 are designed , producing in a half band IIR filter [3], that is

$$H(z) = H0(z^{-2}) + z^{-1}H1(z^{-2}) \qquad (1)$$

$$= \prod_{k=1}^{K_0} \frac{a_{0,k} + z^{-2}}{1 + a_{0,k}z^{-2}} + z^{-1} \prod_{k=1}^{K_1} \frac{a_{1,k} + z^{-2}}{1 + a_{1,k}z^{-2}}$$

Here, K0 and K1 give the quantity of the all pass filter cells of second-order which are employed in every section of the filter in Fig 2. Fig. 3(a) shows the all-pass filters of order two are often designed by solely 2 adders. This half-band IIR filter has 2 blessings. First one is that, the quantity of adders and coefficients is less providing the chance for efficient optimization. Second one is because the all-pass units are implemented by using H0(z^{-2}) and H1(z^{-2}), they will be completed, runs at half of sampling rate, which is shown in Fig. 4,therefore the ensuing figure for all-pass filter of order two is shown in Fig. 3(b).

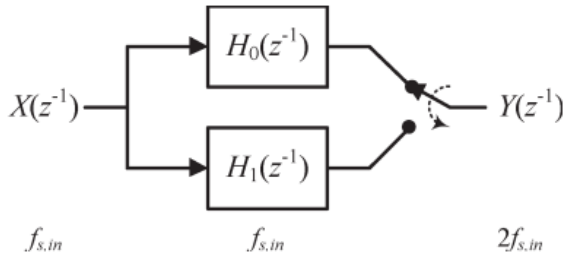

Fig.4. Half band IIR filter where the filters $H0(z^{-2})$ and $H1(z^{-2})$ are running at $f_{s,\,in}$.

Area and current consumption is an initial thought in any implementation, which makes this filter is well suited to this design like hearing aids [2]. In order to scale back the requirements of the hardware within this filter, the existing design specialize in filter coefficients and implementation as an add of whole number powers which is of 2.Generally adders amount to the bulk of the equipment which is required to design the filter. Thus decreasing the quantity of adders may be a smart efficient level enhancement technique to attain each power potency and large amount of hardware within the device implementation. So the complexness of this half band IIR filter within the progressive work is decided by enumeration the quantity of adders which is required to design the coefficients. The world of associate degree adder is non-essential In an exceedingly fashionable Complementary Metal-Oxide Semiconductor(CMOS) method except for some powerful applications, appreciate hearing aids, facility utilization is of utmost importance. Thus using less number of adders is preferable. The two all-pass filters which are connected in parallel then that the perfect structure to implement digital filters. This filter class is represented by less coefficient sensitivity. Moreover the number of multipliers used gives the order of the filter in contrast to the other implementation methods, such as in the standard direct-form realizations requires about double the number of multipliers. The resulting filter structures are highly compatible, thereby making them capable for VLSI design implementations. This section represents a methodology for implementing recursive digital filters with less coefficient word length by all pass filters filter cells which are connected in parallel.

b) Multiplier free half band IIR Filter

With advancement in high rate digital integrated circuit methodology, it is better to design a filter with a cascade of multiple less expensive stages on behalf of a separate more complex stage. Reconfigurable also programmable filter system with less round-off error sensitiveness, easy coefficients and low dynamic range is also mostly required. Coefficients containing terms as an add of a less number of signed power which is of two are extremely fascinate for a low complicated implementation. The design of an efficient cascaded half-band IIR filter structures is given in this section which need exclusively binary shifts and additions rather than multiplications that are used in regular direct-form structures. By the multiple utilization of the same half-band IIR sub filter multiplier-free structures for half- band IIR filter is designed in this section. A fully multiplier less structure as a sub filter is shown in figure 5. A compound half-band IIR filter is designed for sharpening which utilizes algebraic composition of several sub filters. The IIR filter which is obtained is also a half-band.

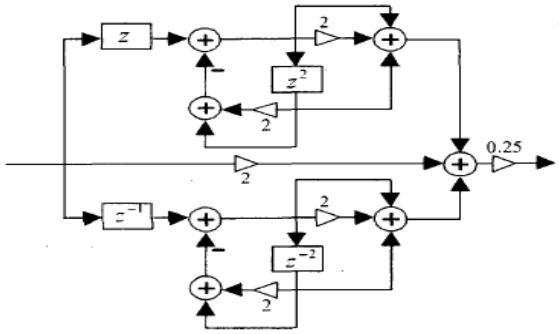

Fig.5. Multiplier-free half-band IIR filter

As shown in fig 6 the obtained filter is totally multiplier-free and is not subjected to fixed word length effect. Like this approach, we can synthesize some more half band IIR filters by the addition of a few more stages. Certainly an added stage will give an enhancement of response. Within a less number of iterations a remarkable development is obtained.

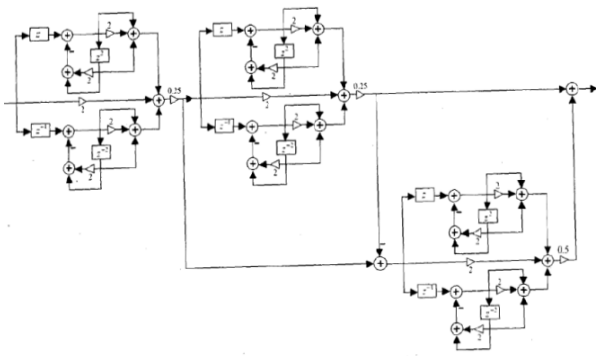

Fig.6. Multiplier-free multi-stage structure half-band IIR filter

III. PROPOSED HALF BAND IIR FILTER

In digital signal processing applications and many VLSI computational units multipliers are frequently used. With the current advances in technology, a number of multiplication techniques have been performed for attaining the need of producing less area, high speed.

a) Array Multiplier structure

Array multiplier is familiar because of its design. By using add and shift methodology this multiplier is implemented. By the multiplying the multiplicand with one multiplier bit each partial product is generated. In accordance with their bit orders the partial product are shifted and then added. The addition can be implemented with normal carry propagate adder. N-1 adders are needed where N is the multiplier length. Even though the method is easy, the addition is done serially also in parallel. The CRAs are replaced with Carry Save Adders to enhance on the delay and area, in which each carry and sum signal is passed to the adders of the following stage. The end product is obtained in a final adder by some fast adder (generally carry ripple adder). Here we need to add, as many partial products as there are multiplier bits.

				A3	A2	A1	A0	Inputs
			x	B3	B2	B1	B0	
			C	B0 x A3	B0 x A2	B0 x A1	B0 x A0	
		+	B1 x A3	B1 x A2	B1 x A1	B1 x A0		
		C	sum	sum	sum	sum		
	+	B2 x A3	B2 x A2	B2 x A1	B2 x A0			Internal Signals
	C	sum	sum	sum	sum			
+	B3 x A3	B3 x A2	B3 x A1	B3 x A0				
C	sum	sum	sum	sum				
Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Outputs

Fig.7. Array Multiplier

b) Wallace Tree Multiplier structure

A Wallace tree multiplier is an efficient hardware implementation of a digital circuit. Multipliers based on Wallace reduction tree give an area-efficient approach for high speed multiplication

This method has three steps.

1. Partial Product Generation Stage: Multiply (AND operation) every bit of one of the arguments, by every bit of the other.

2. Partial Product Reduction Stage: Groups of three following next to rows are collected. By using full adders and half adders each group of three rows is minimized. Where there are three bits, Full adders are used in every column, whereas half adders are used in every column where there are two bits. Without processing any single bit in a column is pass on to the following section in the same column. In every successive stage this reduction procedure is repeated till only two rows remain. The bit product matrix is reduced to a two row matrix by using adders.

3. Partial Product Addition Stage: To produce the product the remaining two rows are added up utilizing a fast carry propagate adder.

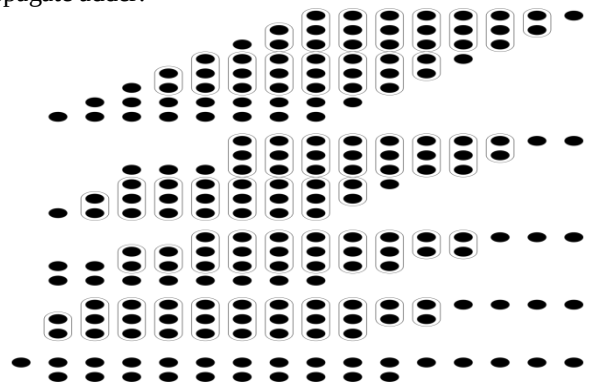

Fig.8.Wallace multiplier

IV. SIMULATION RESULTS AND PERFORMANCE COMPARISONS

The programming has been done in Verilog HDL and it is simulated using Xilinx ISE Tools and ISim simulator. The simulation results of multiplier free half band IIR filter is and half band IIR filter is designed by using various multipliers is shown in figure 9, 10, 11 .Table I summarize the performance metrics of the half band IIR filter and multiplier free half band IIR filter. The area, and delay comparisons of half band IIR Filter using different multipliers are presented in Table II and table III.

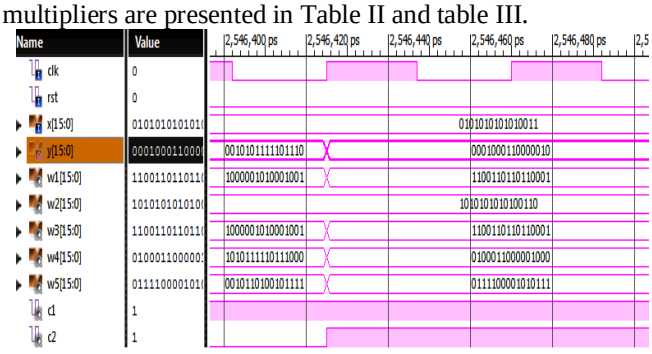

Fig.9. Simulation results of multiplierless half band IIR filter

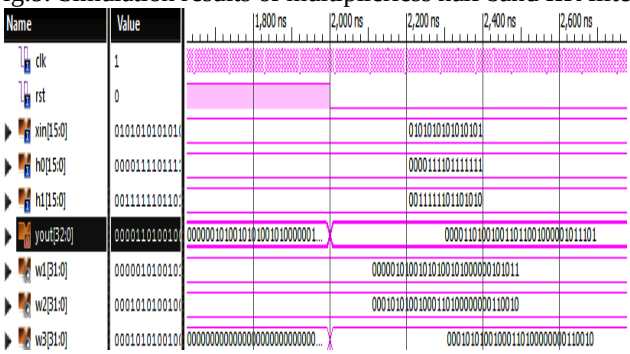

Fig.10. Simulation results of half band IIR filter using Array Multiplier

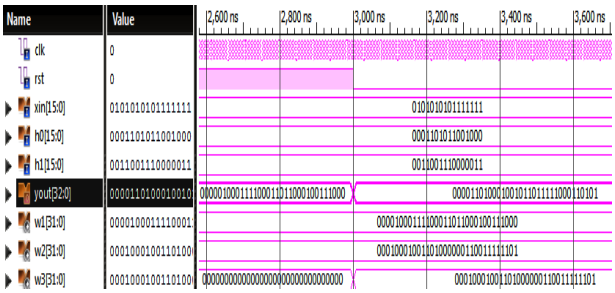

Fig.11.Simulation results of half band IIR filter using Wallace Multiplier

TABLE I. Area, Delay comparisons of different Half band IIR Filters

Design	Area		Delay(ns)
	slices	LUTs	
Half Band IIR Filter	1157	2146	86.741
Multiplier free Half Band IIR Filter	182	339	53.882

TABLE II. Area comparison of Half band IIR Filter with different multipliers

Design	All pass filter cell		Half Band IIR Filter	
	Slices	LUTs	Slices	LUTs
Half Band IIR Filter	659	1253	1157	2146
Half Band IIR Filter using Array multiplier	490	835	832	1304
Half Band IIR using Wallace multiplier	382	735	715	1266

TABLE III. Delay comparison of half band IIR Filter with different multipliers

Design	All pass filter cell	Half Band IIR Filter
Half Band IIR Filter	70.192	86.741
Half Band IIR Filter using Array Multiplier	59.605	69.892
Half Band IIR Filter using Wallace multiplier	57.860	68.476

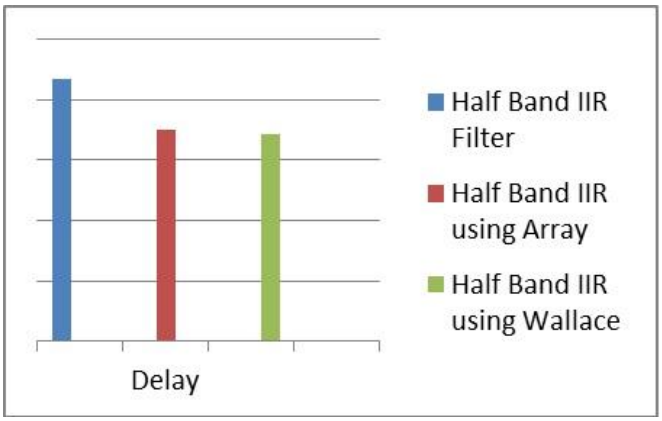

Fig.12.Delay Comparison

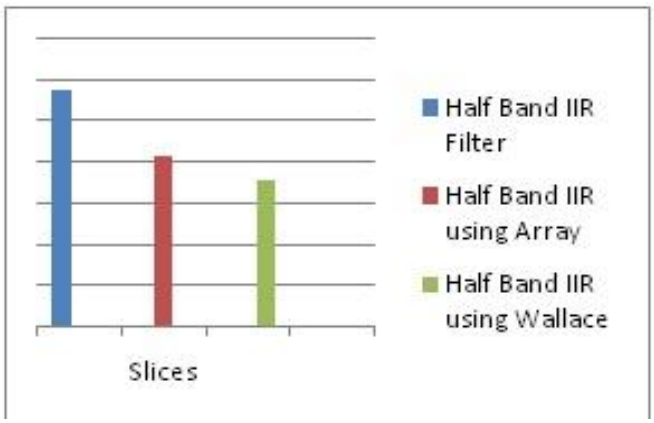

Fig.13.Slices Comparison

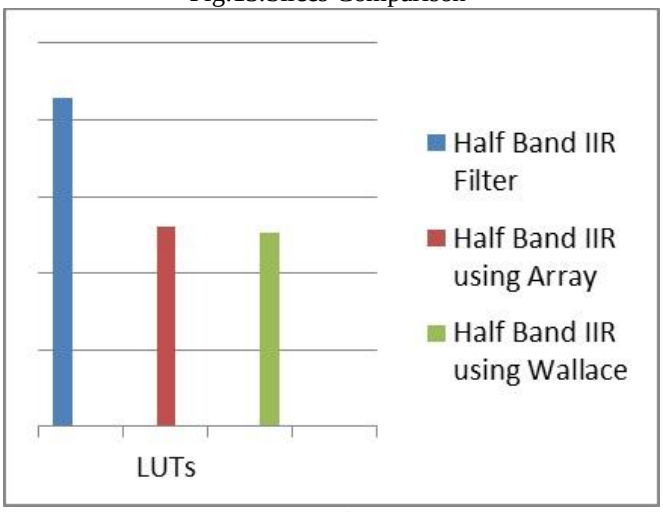

Fig.14. LUTs Comparison

V. CONCLUSION

A straight forward improvement methodology which is bestowed for a half band IIR filter so as to get a less difficulty hardware of the filter that is computed with reference to the amount of adders. For sharpening, a multiplier-free of the IIR half-band IIR filter is designed by multiple utilization of the same IIR half-band sub filters with much lesser arithmetic caliculations. Half band IIR Filter is implemented using Array multiplier and Wallace tree multiplier and multiplier. Half band IIR filter is achieving 19.43 %, 21.06% of delay reduction by using Array

multiplier, Wallace multiplier when compared to existing half band IIR Filter. Hence half band IIR Filter by Wallace Tree has better optimization in terms of speed and compared to the array multiplier.

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