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DESIGN OF LOW POWER-HIGH SPEED BINARY ADDER USING REVERSIBLE LOGIC

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ABSTRACT: Reversibility plays a fundamental role when computations with minimal energy dissipation are considered. In recent years, reversible logic has emerged as one of the most important approaches for power optimization. A reversible logic design will not result in loss of information; this avoids the unwanted heat generated. For power not to be dissipated in an arbitrary circuit, it must be built from reversible gates. In computers and other kinds of processors, adders are used not only in the ALU(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, and in digital electronics, adder performs addition of two numbers. This research proposes a new implementation of adder in reversible logic. The power requirements of traditional methods used to increase performance are too great. It has been proven that use of traditional irreversible logic gates, leads to power dissipation regardless of underlying technology. The proposed design reduces the number of gate operations compared to the existing adder reversible logic implementations. So, this design gives rise to an implementation with a reduced area and delay. We can use it to construct more complex systems in nanotechnology. The high speed adder circuit using Hardware Description Language (HDL) is constructed and verified in the platform Xilinx ISE 9.2i and synthesized using nc-sim and virtuoso of cadence in 180nm Technology to analyze the design parameters.

Keywords: High Speed Adder, Reversible logic, Garbage output, irreversible gates.

I. INTRODUCTION

The core of every microprocessor, digital signal processor (DSP), and data- processing application-specific integrated circuit (ASIC) is its data path. It is often the crucial circuit component if die area, power dissipation, and especially operation speed are of concern. At the heart of data-path and addressing units in turn are arithmetic units, such as comparators, adders, and multipliers. Finally, the basic operation found in most arithmetic components is the binary addition. Besides of the simple addition of two numbers, adders are also used in more complex operations like multiplication and division. But also simpler operations like incrementation and magnitude comparison base on binary addition.Therefore, binary addition is the most important arithmetic operation. [2] It is also a very critical one if implemented in hardware because it involves an expensive carry-propagation step, the evaluation time of which is dependent on the operand word length. The efficient implementation of the addition operation in an integrated circuit is a key problem in VLSI design.

1.1 Adder circuits

Several types of adders are used in computing systems. A ripple carry adder has the simplest structure. In a ripple carry adder, full adders connected in series generate the sum and the carry outputs based on the addend bits and the carry input. The disadvantage of a ripple carry adder is that the carry has to propagate through all stages.

1.2 Full Adder

A Full Adder (FA) is a logical circuit that performs an addition operation on three binary digits. The full adder produces a sum and a carry value, which are both binary digits. The logical diagram of full adder is shown in figure 1.

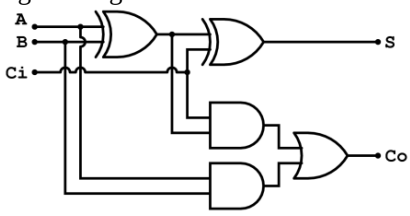


Figure 1. Full adder

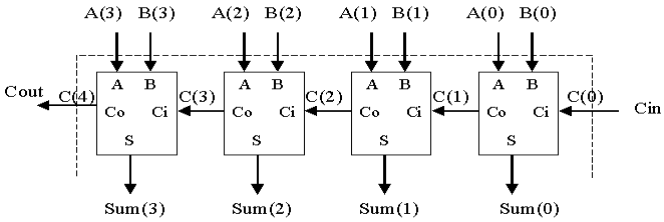


Figure 2. Ripple carry adder

A FA adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as A, B, and C_i here A, B are the operands, and C_i is a bit carried in (in theory from a past addition by [3]). The circuit produces a two-bit output sum typically represented by the signals C_o (Carry) and S (Sum). The Boolean equation and truth table are shown bellow.

(1) S = a xor b xor c; (2) Co = ab + bc + ca ;

1.3 Ripple carry adders

The basic building block of a ripple carry adder is a full adder block. A full adder computes the sum bit *Si* and the carry output *c i+1* based on addend inputs a and b and carry input c. The output expressions for a ripple carry adder are

(1) Si = a xor b xor c; (2) Ci+1 = ab + bc + ca ; (i = 0,1,2,....)

It is possible to create a logical circuit using multiple full adders to add *N*-bit numbers. Each full adder inputs a carry

C_{in} that is the C_{out} of the previous adder. This kind of adder is a Ripple Carry Adder (RCA) in [3], since each carry bit "ripples" to the next full adder. However, the ripple carry adder is relatively slow, since each full adder must wait for the carry bit is which coming from the previous full adder. The RCA is shown in figure. 2.

1.4 Carry – Select Adder

Carry Select Adders (CSLA) use multiple narrow adders to create fast wide adders. Consider the addition of two n bit numbers with a = $a_{n-1}.....a_0$, and b = $b_{n-1}.....b_0$. At the bit level the adder delay increases from the least significant 0^{th} position upward, with the $(n-1)^{th}$ requiring the most complex logic. A carry select adder breaks the addition problem into smaller groups. A carry-select adder provides two separate adders for the upper words, one for each possibility. A multiplexer (MUX) is then used to select the valid result. The figure 3 shows the block diagram of CSLA. As a concrete example, consider an 8-bit adder that is split into two 4-bit groups. The lower order bits a_3 a_2 a_1 a_0 and b_3 b_2 b_1 b_0 are fed into the 4-bit adder to produce the sum bits S_3 S_2 S_1S_0 and a carry-out bit C_4 as shown.

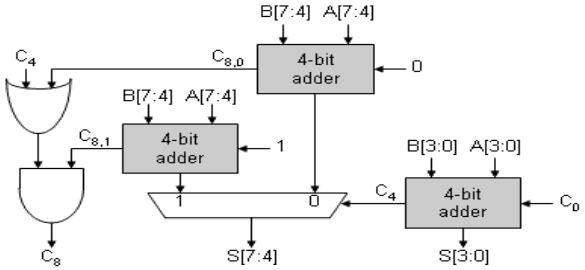


Figure 3. Carry Select Adder

II. INTRODUCTION TO REVERSIBLE LOGIC

A Reversible circuit/gate can generate unique output vector from each input vector, and vice versa, i.e., there is a one to one correspondence between the input and output vectors. Thus, the number of outputs in a reversible gate or circuit has the same as the number of inputs, and commonly used traditional NOT gate is the only reversible gate. Each Reversible gate has a cost associated with it called Quantum cost. The Quantum cost of a Reversible gate is the number of 2*2 Reversible gates or Quantum logic gates required in designing. One of the most important features of a Reversible gate is its garbage output i.e., every input of the gate, which is not used as input to other gate or as a primary output is called garbage output. Minimization of the number of Reversible gates, Quantum cost and garbage inputs/outputs are the focus of research in Reversible logic [3].

Reversible logic is a promising computing design paradigm, which presents a method for constructing computers that produce no heat dissipation. Reversible computing emerged as a result of the application of quantum mechanics principles towards the development of a universal computing machine. Specifically, the fundamentals of reversible computing are based on the relationship between entropy, heat transfer between molecules in a system, the probability of a quantum particle occupying a particular state at any given time, and the quantum electrodynamics between electrons when they are in dose proximity. A reversible logic gate is an N-input N-output logic device that provides one to one mapping between the input and the output. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs.

- Garbage outputs are those, which do not contribute to the reversible logic realization of the design.
- Quantum cost refers to the cost of the circuit in terms of the cost of a primitive gate.
- Gate count is the number of reversible gates used to realize the function.
- Gate level refers to the number of levels which are required to realize the given logic functions.

The following are the important design constraints for reversible logic circuits. [1]

1. Reversible logic gates do not allow fan-outs.
2. Reversible logic circuits should have minimum quantum cost.
3. The design can be optimized so as to produce minimum number of garbage outputs.
4. The reversible logic circuits must use minimum number of constant inputs.
5. The reversible logic circuits must use a minimum logic depth or gate levels.

III. III PROPOSED DESIGN

Basic operation, structure, Quantum cost has been explained in many papers. So the available designs of full adder using basic reversible logic gates take more area, power and have more delay.

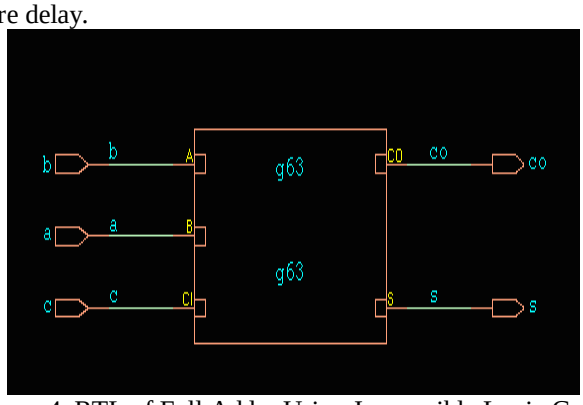


Figure 4. RTL of Full Adder Using Irreversible Logic Gates

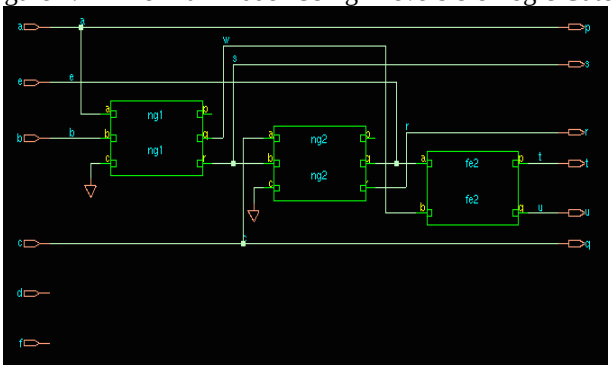
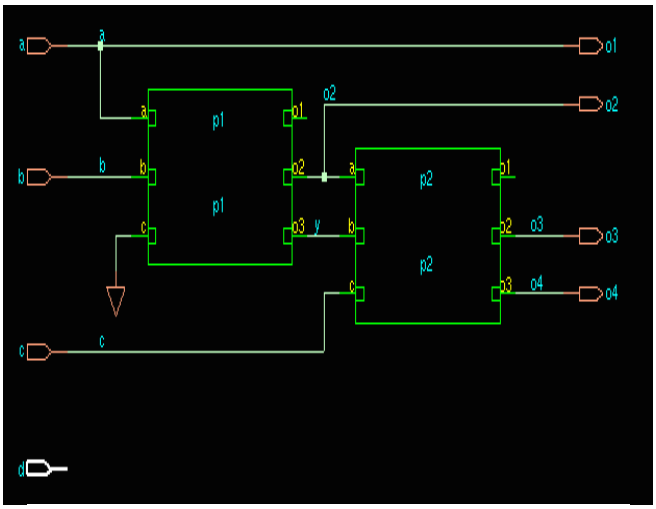


Figure 5. RTL of Full Adder Using Proposed NGFE Logic



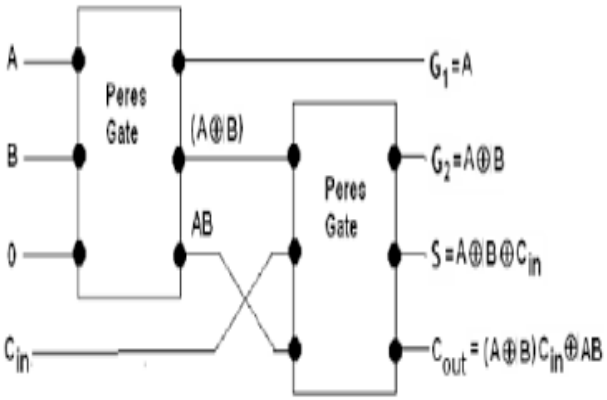


Figure 6. RTL of Full Adder Using Peres Gates

A new design for full adder is proposed in this paper, which uses the conventional new gate, and Feynman gate but results with less area, power and delay. Also when compared with irreversible logic gates it provides all the parameters with less values. The proposed full-adder is designed in Verilog HDL and synthesized using cadence nc-sim simulator. The parameter results, shows a drastic improvement when compared to irreversible logic gates and conventional design using peresgate. The full adder features are specified in Table I for designs using irreversible logic, conventional peresgate and proposed NGFE logic based full adder. Figure 4 shows the schematic of full adder using basic logic gates with specified three inputs a, b, cin and two outputs cout, sum. This full adder design is universal consisting of EXOR gates, AND gates and OR-gate and the design factors are specified in table. The Figure 6 shows the schematic of full adder designed using two three input peres gates making it a 4 input 4 output full adder with inputs a, b, cin and one constant input with logic-0 and outputs sum and carry with two more garbage outputs. The design has comparatively improved design factors than a basic irreversible logic based full adder. Figure 5 shows Proposed new gate and Feynman gate based adder making it a 6 input 6 output circuit. The RCA is used to design the 4bit CSA, which is constructed using logic gates, peres gate and proposed adder too. The constraint parameters of VLSI design are listed in table-II for RCA. Figure 7,8 and 9 shows the schematic structure of RCA and RCA based CSA respectively.

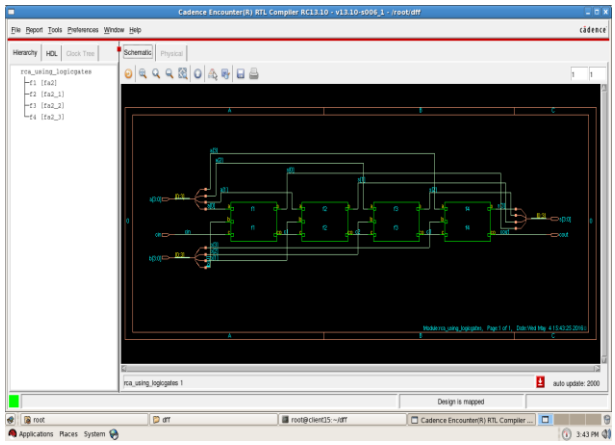


Figure 7(a). RTL of RCA Using Irreversible Logic Gates

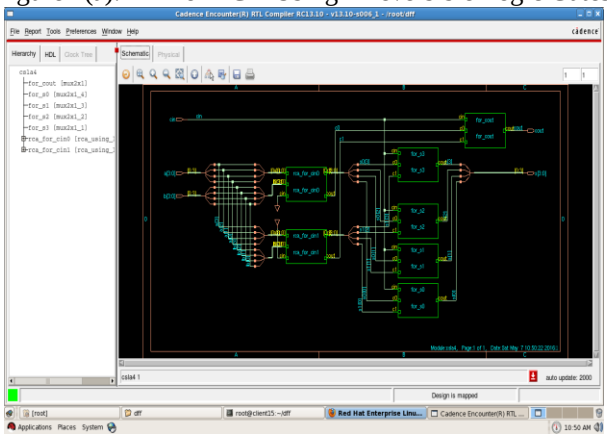


Figure 7(b). RTL of CSA Using Irreversible Logic Gates

TABLE-I

Full Adder	Area (um 2)	Power (nW)			Delay (nS)	No. of Instances
		Leakage Power	Dynamic Power	Total Power		
Using Irreversible Logic gates	70	3.632	4.439	4.443	0.491	1
Using Peres Gate	96	4.116	3.546	3.55	0.686	3
Using NGFE Logic	53	2.422	0.971	0.973	0.477	3

TABLE-II

Ripple Carry Adder	Area (um 2)	Power (uW)			Delay (nS)	No. of Instances
		Leakage Power	Dynamic Power	Total Power		
Using Irreversible Logic gates	279	0.0153	21.644	21.659	1.484	4
Using Peres Gate	386	0.0164	16.125	16.142	1.378	12
Using NGFE Logic	213	0.00968	3.939	3.949	0.476	12

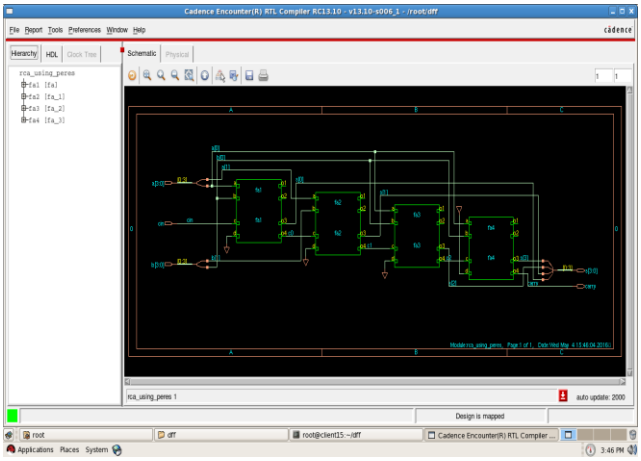


Figure 8(a). RTL of RCA Using Peres Gate

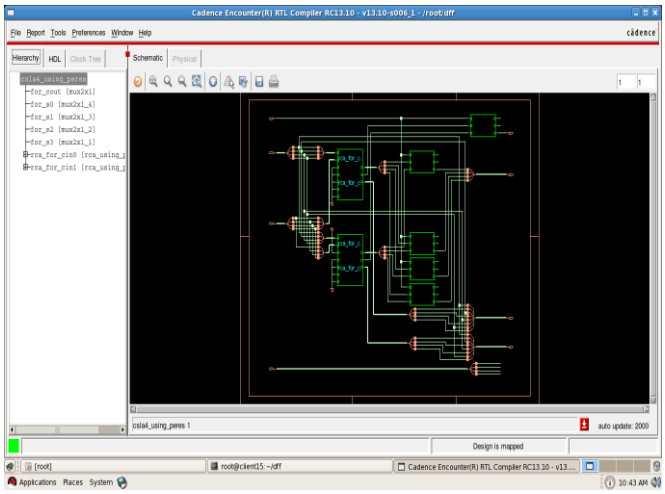


Figure 8(b). RTL of CSA Using Peres gate

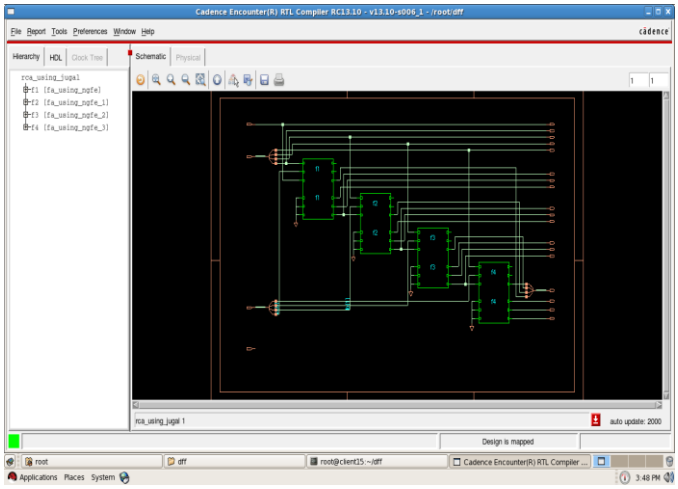


Figure 9(a). RTL of RCA Using Proposed NGFE Logic

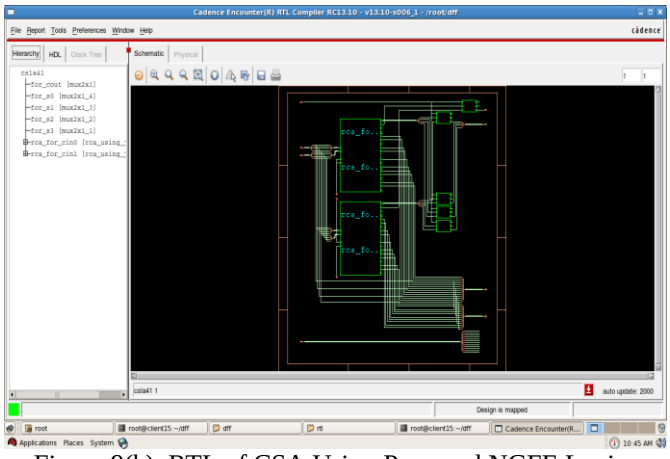


Figure 9(b). RTL of CSA Using Proposed NGFE Logic

IV. ANALYSIS AND TOOL SIMULATION

To evaluate performance; the adder structures discussed in this paper are designed using 180nm CMOS technology using cadence-virtuoso and ncsim. The virtuoso tool integrates traditionally separated front-end and back-end chip design into an integrated flow, accelerating the design cycle and reduced design complexities.

TABLE-III

Carry Select Adder (CSA) based on	Area (um 2)	Power (uW)			Delay (nS)	No.of Instances
		Leakage Power	Dynamic Power	Total Power		
Using Irreversible Logic gates	669	0.2830	33.532	33.560	1.523	32
Using Peres Gate	858	0.03765	29.222	29.260	1.454	27
Using NGFE Logic	639	0.03509	9.1216	9.1567	0.744	29

It tightly integrates mixed-signal implementation with digital implementation, circuit simulation, transistor level extraction and verification. All simulations are carried out at nominal conditions: VDD=1.8V, I/O supply voltage: 1V. Table I shows the drastically reduction in all the major parameters for making a useful design. Table III shows the comparison of area power and timing of irreversible logic gates, peres gate and reversible logic gate. This Proposed design has very less consumption of area and power with less delay from input to carry output.

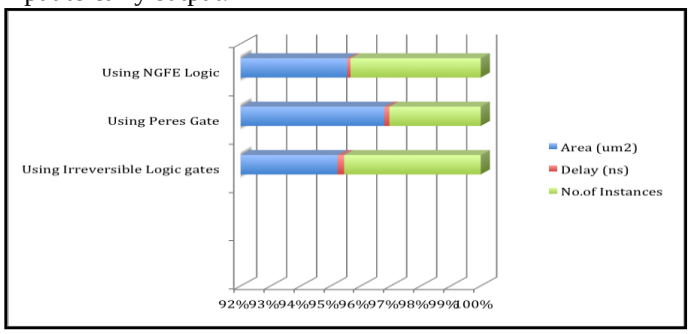


Figure 10. Graphical representation of % of area covered, Power consumed and speed in comparison with logic gates and peres gate.

V. CONCLUSION

The implementations of three types of adders, ripple carry adder, and carry select adder, using reversible logic gate is shown. Results show that the proposed design in more efficient adder in terms of area and power consumption with account of more garbage outputs than those using the logic gates and better in all terms when compared to adder using peres gate.

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