International Journal For Technological Research In Engineering
Volume 4, Issue 2, October-2016 *ISSN (Online): 2347 - 4718*

CMOS REALIZATION OF A LOW POWER SHIFT REGISTERS USING PULSED LATCHES

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Abstract: The timing elements and clock interconnection networks such as flip-flops and latches, is One of the most power consuming components in modern very large Scale integration (VLSI) system. The area, power and transistor count will compared and designed using several latches and flip flop stages. Flip Flop is a circuit which is used to store state information. Power consumption is one of the main objectives in designing a flip flop.The power consumption are reduced by replacing flip-flops with pulsed latches. In the standard system, shift register uses single pulsed clock signal for data transition, which consumes additional power. The shift register uses a small number of the pulsed clock signals and combine the latches to many sub shifter registers and exploitation further temporary storage latches. To minimize power consumption various non overlap delayed pulsed clock signal design is proposed for data synchronization in an exceedingly multi bit shift register. The proposed system is designed by using a popular Schematic and layout capture tool with 90nm technology.
Keywords: Low Power, flip-flop, pulsed clock, pulsed latch, shift register

I. INTRODUCTION

In digital design flip-flops and latches are basic storage elements. Flip flops are precarious timing elements in digital circuits which have a great impact on speed and power consumption [6]. In VLSI chip design reducing power has become a important consideration of an performance and area. ASHIFT register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters [2], communication receivers [3], and image processing ICs [4]–[5]. Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs.The Shift register is a type of sequential circuit it is mainly used for storage or transfer digital data. An N-bit shift register consists of N -data flip-flops which are connected in series form [1]. The implementation of the N-data flip-flop is less important element to regulate the capability of the total synchronous circuit than the area and power consumption as a result there is no circuit present between flip-flops within the register. To reduce the area and power consumption, the smaller flip-flop is used for the register [3]. In this flip flops the transistor are more compared to pulsed latches so that the circuit has more switching and power consumption is high. Flip-flops are replaced by pulsed latch in several applications, because pulsed latches are smaller than flip flops. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. The rest of the paper describes the proposed shift register architecture in section II. Result measures are presented in section III. Conclusion is given in section IV.

II. PROPOSED ARCHITECTURE

The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. Shift registers can have both parallel and serial inputs and outputs. These are often configured as 'serial-in, parallel-out' (SIPO) or as 'parallel-in, serial-out' (PISO). There are also types that have both serial and parallel input and types with serial and parallel output. There are also 'bidirectional' shift registers which allow shifting in both directions:
L→R or R→L. The serial input and last output of a shift register can also be connected to create a 'circular shift register.

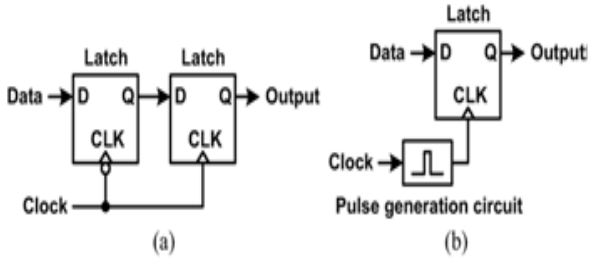


Figure 1: (a) Master-slave flip-flop. (b) Pulsed latch.

A master-slave flip-flop using two latches in Fig.1(a) can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal in Fig. 1(b)[6]. All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for small area and low power consumption. The pulsed latch cannot be used in shift registers due to the timing problem, as shown in Fig. 2. The shift registers in Fig. 2(a) consists of several latches and a pulsed clock signal (CLK_pulse). The operation waveforms in Fig. 2(b) show the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the input signals of the first latch (IN) is constant during the clock pulse width (TPULSE). But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width.

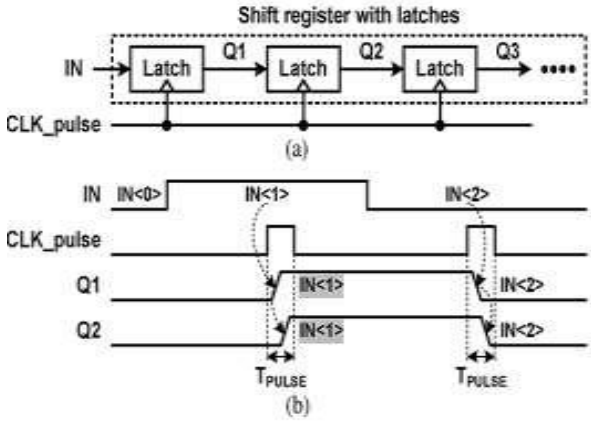


Fig. 2. Shift register with latches and a pulsed clock signal. (a) Schematic. (b)Waveforms

One solution for the timing problem is to add delay circuits between latches, as shown in Fig. 3(a). The output signal of the latch is delayed and reaches the next latch after the clock pulse. As shown in Fig. 3(b) the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width , but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. As a result, all latches have constant input signals during the clock pulse and no timing problem occurs between the latches. However, the delay circuits cause large area and power over heads.

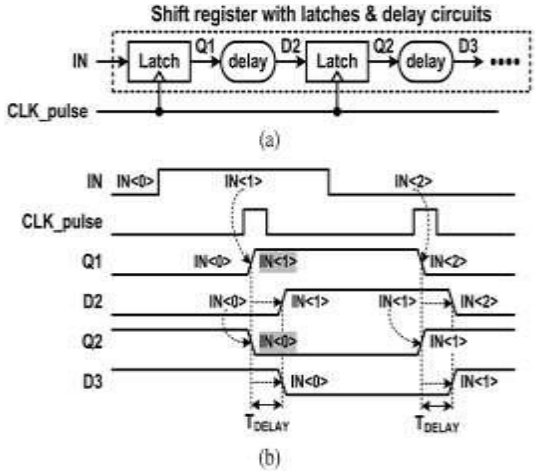
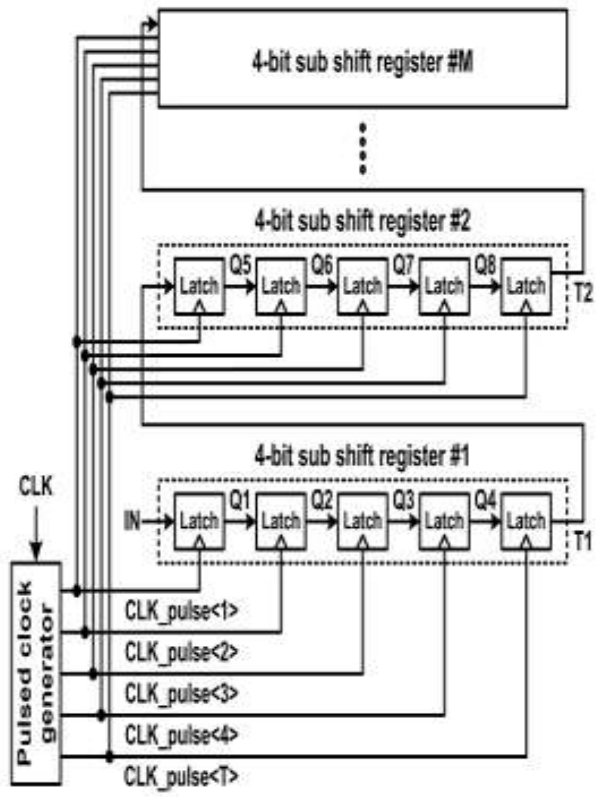
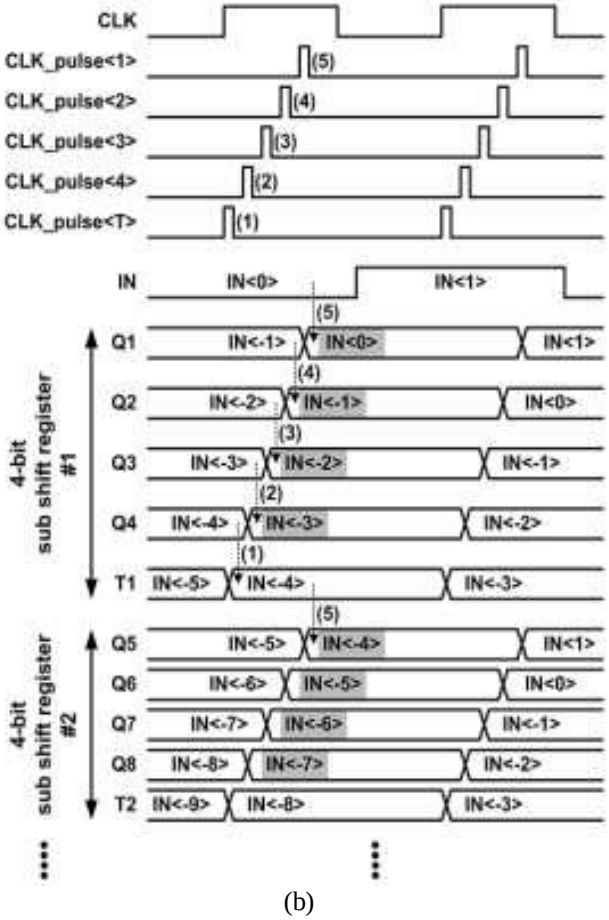


Fig. 3. Shift register with latches, delay circuits, and a pulsed clock signal. (a)Schematic. (b)Waveforms

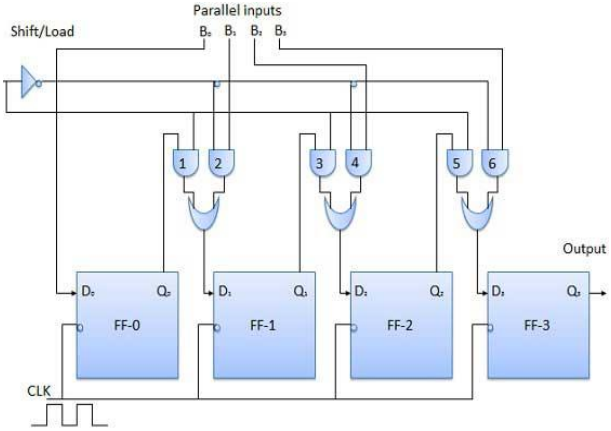
A 4-bitsub shifter register consists of five latches and it performs shift operations with five non overlap delayed pulsed clock signals (CLK_pulse<1:4>and CLK_pulse<T>). In the 4-bit sub shiftregister #1, four latches store 4- bit data (Q1-Q4) and the last latch stores 1-bit temporary data (T1) which will be stored inthe first latch (Q5) of the 4-bit sub shift register #2. Fig. 4(b)shows the operation waveforms in the proposed shift register.Block diagram of Parallel in Serial out(PISO) Shift register is shown in fig 4(c).designing of PISO register is same as that of the SISO shift register,difference is the inputs are in parallel manner and set to the latches using multiplexers.



(a)



(b)



(C)

Fig. 4. Proposed shift register. (a) SISO shift register Schematic. (b)Waveforms.(c) PISO shift register Schematic.

The conventional delayed pulsed clock circuits can be used to save the AND gates in the delayed pulsed clock generator in Fig. 6. In the conventional delayed pulsed clock circuits,the clock pulse width must be larger than the summation of the rising and falling times in all inverters in the delay circuits to keep the shape of the pulsed clock.

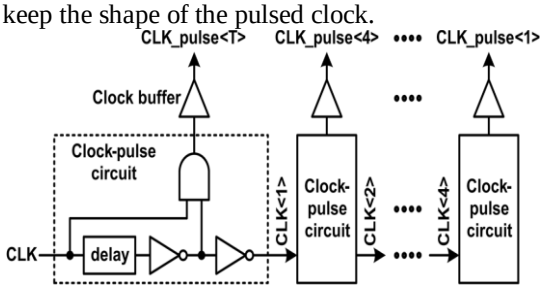


Fig. 5. Delayed pulsed clock generator.

This design implementation the proposed shift register uses the pulsed latch is SSASPL (static differential sense amp shared pulsed latch) it is smallest pulsed latch. By using this SSASPL the design of pulsed latch used in proposed shift register. The below fig .6 shows the circuit diagram of SSASPL with transistors.

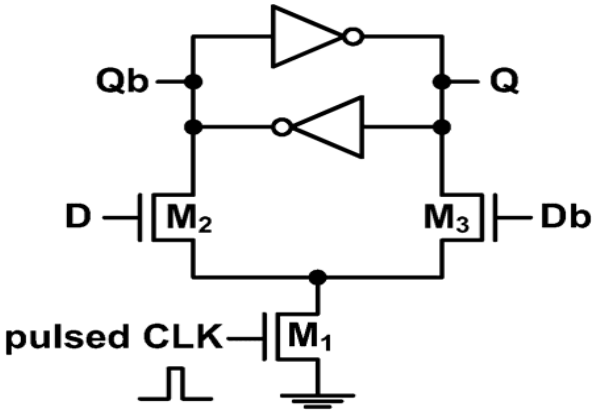
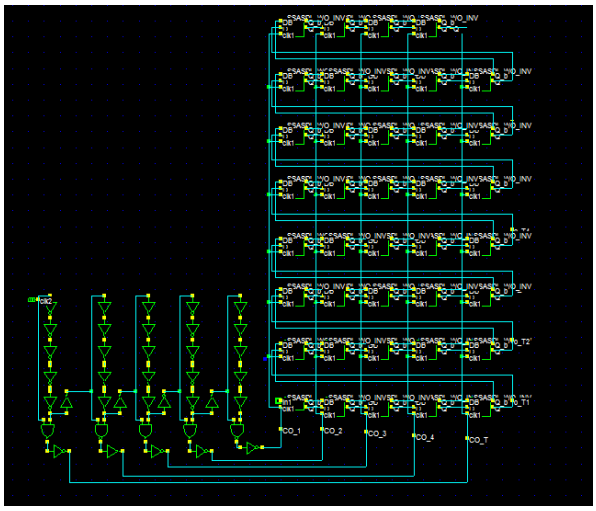


Fig. 6.Schematic of the SSASPL.

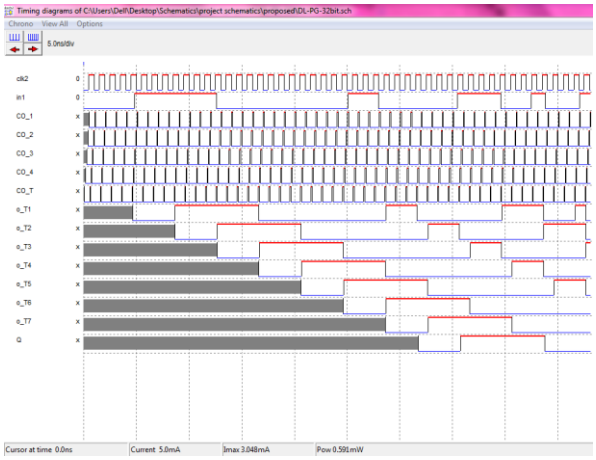
Simulation Results:

The main focus of this work is to meet all challenges faces in designing of shift register circuit with pulsed latch.The simulation results are shown in below figures.

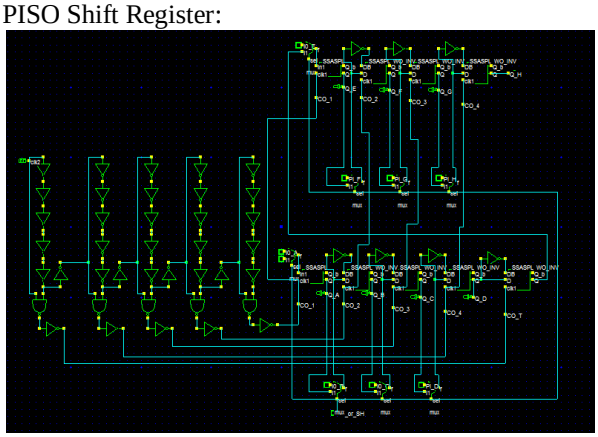
SISO Shift Register:



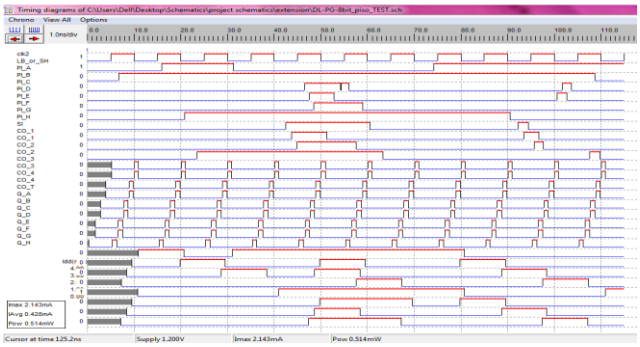
Waveform of SISO:



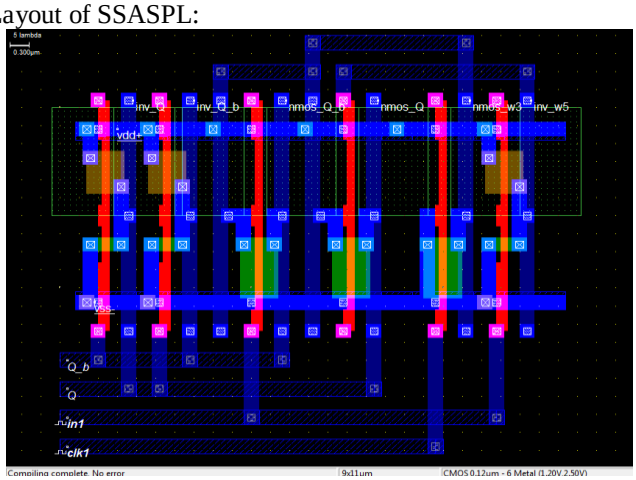
PISO Shift Register:



Waveform of PISO:



Layout of SSASPL:



Comparison:

Shift Register	Power
SISO mode	207.976mW
PISO mode	0.349 mW

III. CONCLUSION

This paper proposed a low-power and area-efficient shift register using pulsed latches. The shift register reduces area and power consumption by substituting flip-flops with pulsed latches in both PISO and SISO modes. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals as an alternative of a single pulsed clock signal.

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